钛地半导体
Tudi Semiconductor

24AA512/24LC512

512K I²C™ CMOS Serial EEPROM

Device Selection Table

Part Number	Vcc Range	Max. Clock Frequency	Temp. Ranges
24AA512	1.8-5.5V	400 kHz(1)	I
24LC512	2.5-5.5V	400 kH	I

- Cascadable for up to eight devices
- Self-timed erase/write cycle
- 128-byte Page Write mode available
- Hardware write-protect for entire array
- Schmitt Trigger inputs for noise suppression
- 1,000,000 erase/write cycles
- Electrostatic discharge protection > 4000V
- Data retention > 200 years
- 8-pin PDIP, SOIC (208 mil), and DFN/TSSOP packages

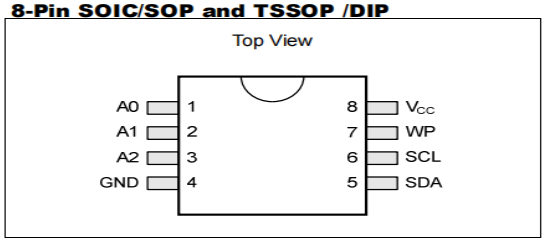
- Standard and Pb-free finishes available
- Temperature ranges:
  - Industrial (I):

Description

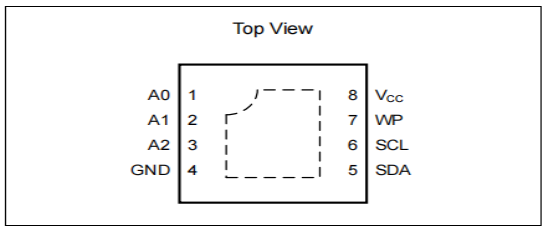
The 24AA512/24LC512(24XX512*) is a 64K x 8 (512 Kbit) Serial Electrically Erasable PROM, capable of operation across a broad voltage range (1.8V to 5.5V). It has been developed for advanced, low-power applications such as personal communications and data acquisi-tion. This device also has a page write capability of up to 128 bytes of data. This device is capable of both random and sequential reads up to the 512K boundary. Functional address lines allow up to eight devices on the same bus, for up to 4 Mbit address space. This device is available in the standard 8-pin plastic DIP, SOIC, DFN and TSSOP packages.

Package Type

8-Pin SOIC/SOP and TSSOP /DIP



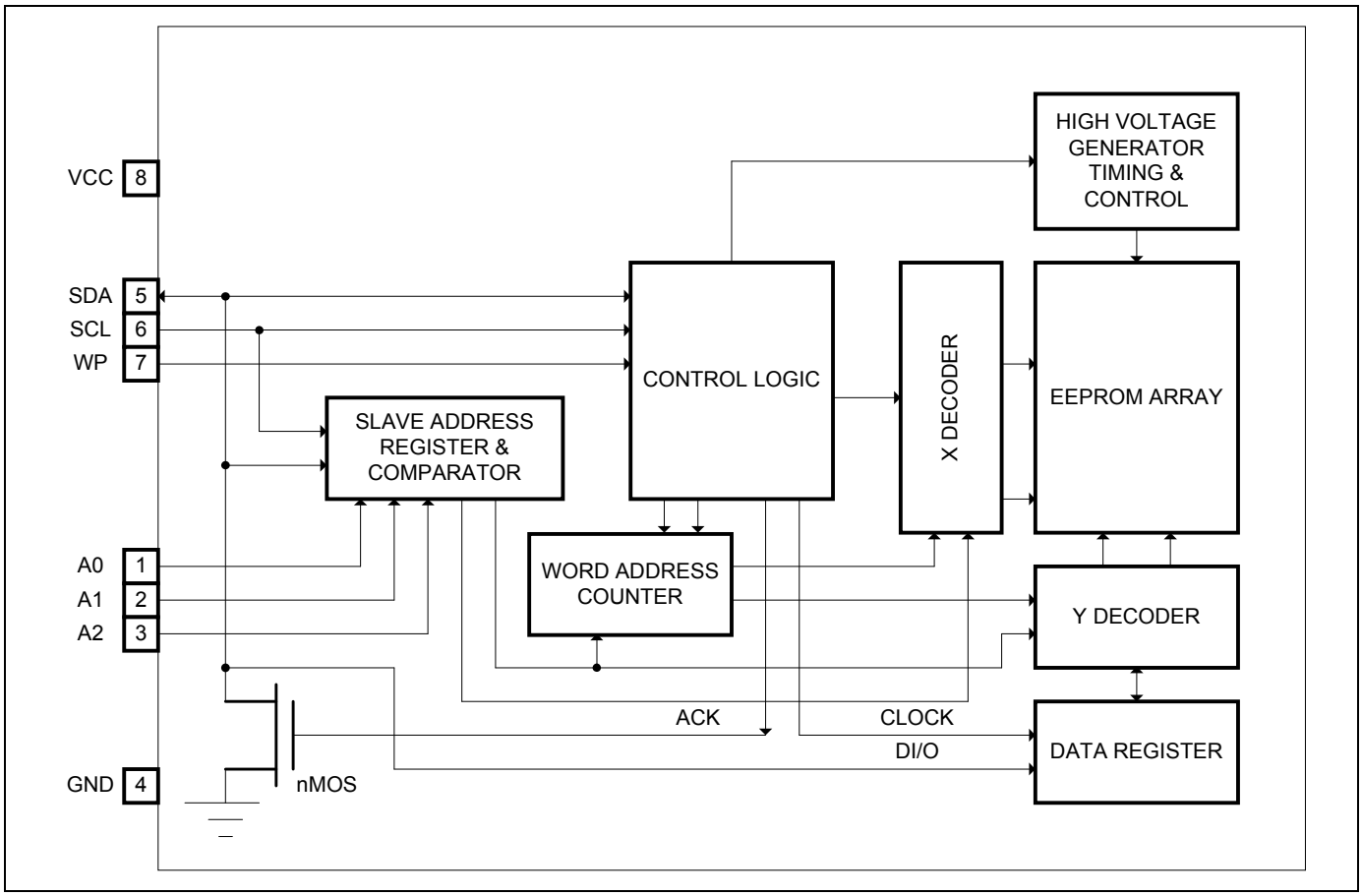
8-Lead DFN



Examples

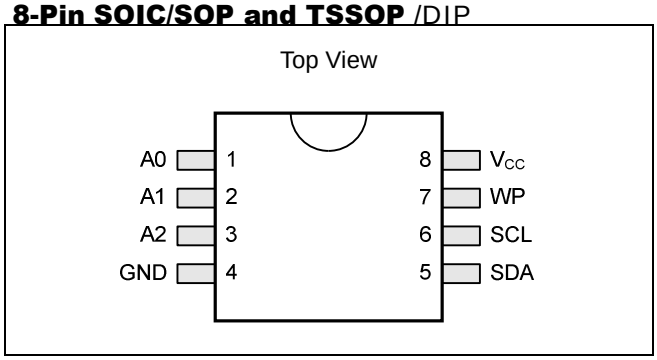
型号	封装	私印	工作电压	兼容电压
24AA512-I/P-TUDI	DIP8	24AA512-I/P	1.8-5.5	2.7V
24AA512T-I/SN-TUDI	SOP8	24AA512I/SN	1.8-5.5	2.7V
24LC512-I/P-TUDI	DIP8	24LC512-I/P	1.8-5.5	
24LC512T-I/SN-TUDI	SOP8	24LC512I/SN	1.8-5.5	

■ Functional Block Diagram

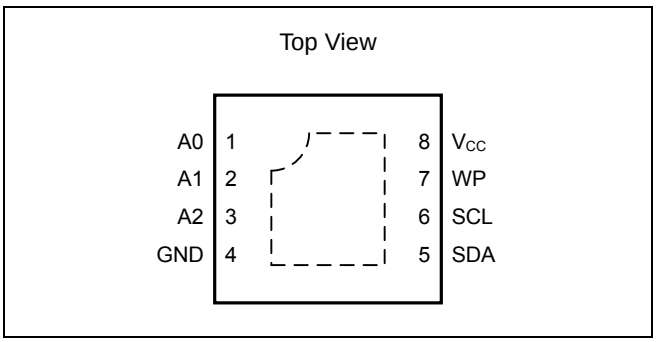


■ Pin Configuration

8-Pin SOIC/SOP and TSSOP /DIP



8-Lead DFN



Pin Definition

Pin No.	Pin Name	I/O	Definition
1	A0	I	Device Address Input
2	A1	I	Device Address Input
3	A2	I	Device Address Input
4	GND	-	Ground
5	SDA	I/O	Serial Address and Data input and Data out put
6	SCL	I	Serial Clock Input
7	WP	I	Write Protect Input
8	V_{CC}	-	Power Supply

Pin Descriptions

SCL

This input clock pin is used to synchronize the data transfer to and from the device.

SDA

The SDA is a bi-directional pin used to transfer addresses and data into and out of the device. The SDA pin is an open drain output and can be wired with other open drain or open collector outputs. However, the SDA pin requires a pull-up resistor connected to the power supply.

A0, A1, A2

The A0, A1 and A2 are the device address inputs.

Typically, the A0, A1, and A2 pins are for hardware addressing and a total of 8 devices can be connected on a single bus system. When A0, A1, and A2 are left floating, the inputs are defaulted to zero.

WP

WP is the Write Protect pin. While the WP pin is connected to the power supply of 24LC512/24AA512 , the entire array becomes Write Protected (i.e. the device becomes Read only). When WP is tied to Ground or left floating, the normal write operations are allowed.

Vcc

Supply voltage

GND

Ground of supply voltage

Device Operation

The 24LC512/24AA512 serial interface supports communications using industrial standard 2-wire bus protocol, such as I^2C.

2-WIRE Bus

The two-wire bus is defined as Serial Data (SDA), and Serial Clock (SCL). The protocol defines any device that sends data onto the SDA bus as a transmitter, and the receiving devices as receivers. The bus is controlled by Master device that generates the SCL, controls the bus access, and generates the Start and Stop conditions. The 24LC512/24AA512 is the Slave device.

The Bus Protocol

Data transfer may be initiated only when the bus is not busy. During a data transfer, the SDA line must remain stable whenever the SCL line is high. Any changes in the SDA line while the SCL line is high will be interpreted as a Start or Stop condition.

The state of the SDA line represents valid data after a Start condition. The SDA line must be stable for the duration of the High period of the clock signal. The data on the SDA line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a Start condition and terminated by a Stop condition.

Start Condition

The Start condition precedes all commands to the device and is defined as a High to Low transition of SDA when SCL is High. The EEPROM monitors the SDA and SCL lines and will not respond until the Start condition is met.

Stop Condition

The Stop condition is defined as a Low to High transition of SDA when SCL is High. All operations must end with a Stop condition.

Acknowledge

After a successful data transfer, each receiving device is required to generate an ACK. The Acknowledging device pulls down the SDA line.

Reset

The 24LC512/24AA512 contains a reset function in case the 2-wire bus transmission on is accidentally interrupted (e. g. a power loss), or needs to be terminated mid-stream. The reset is initiated when the Master device creates a Start condition. To do this, it may be necessary for the Master device to monitor the SDA line while cycling the SCL up to nine times. (For each clock signal transition to High, the Master checks for a High level on SDA.)

Standby Mode

While in standby mode, the power consumption is minimal. The 24LC512/24AA512 enters into standby mode during one of the following conditions: a) After Power-up, while no Op-code is sent; b) After the completion of an operation and followed by the Stop signal, provided that the previous operation is not Write related; or c) After the completion of any internal write operations.

Device Addressing

The Master begins a transmission on by sending a Start condition, then sends the address of the particular Slave devices to be communicated. The Slave device address is 8 bits format as shown in Figure. 1-5.

The four most significant bits of the Slave address are fixed (1010) for 24LC512/24AA512 .

The next three bits, A0, A1 and A2, of the Slave address are specifically related to EEPROM. Up to eight 24LC512/ 24AA512 units can be connected to the 2-wire bus.

The last bit of the Slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, Read operation is selected. While it is set to 0, Write operation is selected.

After the Master transmits the Start condition and Slave address byte appropriately, the associated 2-wire Slave device, 24LC512/24AA512 , will respond with ACK on the SDA line. Then 24LC512/24AA512 will pull down the SDA on the ninth clock cycle, signaling that it received the eight bits of data.

The 24LC512/24AA512 then prepares for a Read or Write operation by monitoring the bus.

Write Operation

Byte Write

In the Byte Write mode, the Master device sends the Start condition and the Slave address information (with the R/W set to Zero) to the Slave device. After the Slave generates an ACK, the Master sends the byte address that is to be written into the address pointer of the 24LC512/ 24AA512 . After receiving another ACK from the Slave, the Master device transmits the data byte to be written into the address

memory location. The 24LC512/24AA512 acknowledges once more and the Master generates the Stop condition, at which time
the device begins its internal programming cycle. While this internal cycle is in progress, the device will not respond to any request from the Master device.

Page Write

The 24LC512/24AA512 is capable of 128-byte Page-Write operation. A Page-Write is initiated in the same manner as a Byte Write, but instead of terminating the internal Write cycle after the first data word is transferred, the Master device can transmit up to 127 more bytes. After the receipt of each data word, the EEPROM responds immediately with an ACK on SDA line, and the seven lower order data word address bits are internally incremented by one, while the higher order bits of the data word address remain constant.
If a byte address is incremented from the last byte of a page, it returns to the first byte of that page. If the Master device should transmit more than 128 bytes prior to issuing the Stop condition, the address counter will “roll over,” and the previously written data will be overwritten. Once all 128 bytes are received and the Stop condition has been sent by the Master, the internal programming cycle begins. At this point, all received data is written to the 24LC512/ 24AA512 in a single Write cycle. All inputs are disabled until completion of
the internal Write cycle.

Acknowledge (ACK) Polling

The disabling of the inputs can be used to take advantage of the typical Write cycle time. Once the Stop condition is issued to indicate the end of the host's Write operation, the 24LC512/24AA512 initiates the internal Write cycle. ACK polling can be initiated immediately. This involves issuing the Start condition followed by the Slave address for a Write operation. If the EEPROM is still busy with the Write operation, no ACK will be returned. If the 24LC512/24AA512 has completed the Write operation, an ACK will be returned and
the host can then proceed with the next Read or Write operation.

Read Operation

Read operations are initiated in the same manner as Write operations, except that the (R/W) bit of the Slave address is set to “1”. There are three Read operation options: current address read, random address read and sequential read.

Current Address Read

The 24LC512/24AA512 contains an internal address counter which maintains the address of the last byte accessed, incremented by one. For example, if the previous operation is either a Read or Write operation addressed to the address location n, the internal address counter would increment to address location n+ 1. When the EEPROM receives the Slave Addressing Byte with a Read operation (R/W bit set to “1”), it will respond an ACK and transmit the 8-bit data byte stored at address location n+1. The Master should not acknowledge the transfer but should generate a Stop condition so the 24LC512/24AA512 discontinues transmission. If 'n' is the last byte of the memory, the data from location '0' will be transmitted. (Refer to Figure 1-8. Current Address Read Diagram.)

Random Address Read

Selective Read operations allow the Master device to select at random any memory location for a Read operation. The Master device first performs a 'dummy' Write operation by sending the Start condition, Slave address and byte address of the location it wishes to read. After the 24LC512/24AA512 acknowledges the byte address, the Master device resends the Start condition and the Slave address, this time with the R/W bit set to one. The EEPROM then responds with its ACK and sends the data requested. The Master device does not send an ACK but will generate a Stop condition. (Refer to Figure 1-9. Random Address Read Diagram.)

Sequential Read

Sequential Reads can be initiated as either a Current Address Read or Random Address Read. After the 24LC512/24AA512 sends the initial byte sequence, the Master device now responds with an ACK indicating it requires additional data from the 24LC512/ 24AA512 . The EEPROM continues to output data for each ACK received. The Master device terminates the sequential Read operation by pulling SDA High (no ACK) indicating the last data word to be read, followed by a Stop condition. The data output is sequential, with the data from address n followed by the data from address n+1,n +2 ... etc. The address counter increments by one automatically, allowing the entire memory contents to be serially read during sequential Read operation. When the memory address boundary of the array is reached, the

address counter “rolls over” to address 0, and the device continues to output data. (Refer to Figure 1-10. Sequential Read Diagram).

Diagrams

Figure 1-1. Typical System Bus Configuration

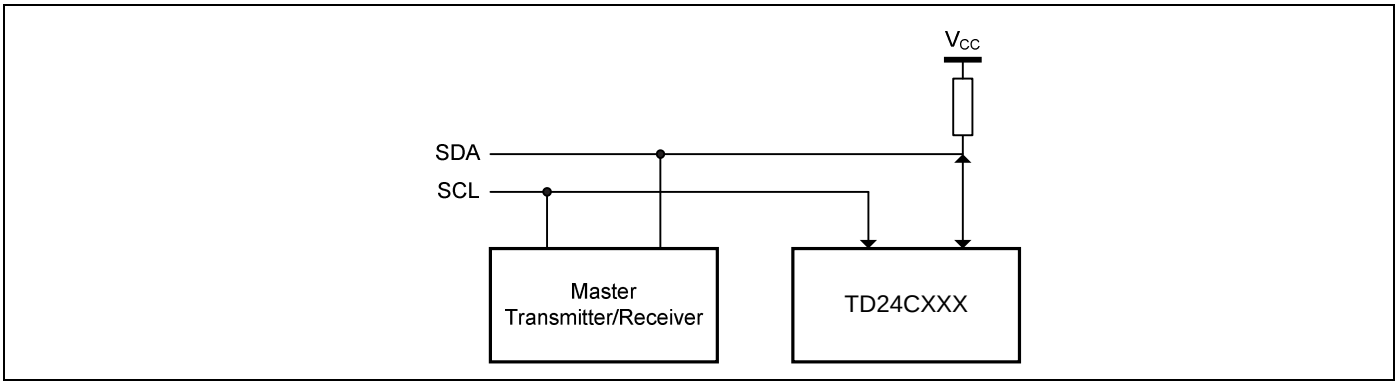


Figure 1-2. output Acknowledge

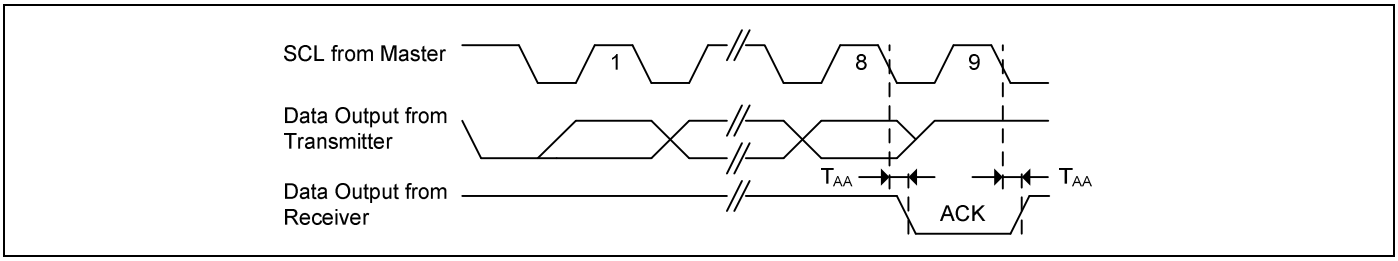


Figure 1-3. Start and Stop Conditions

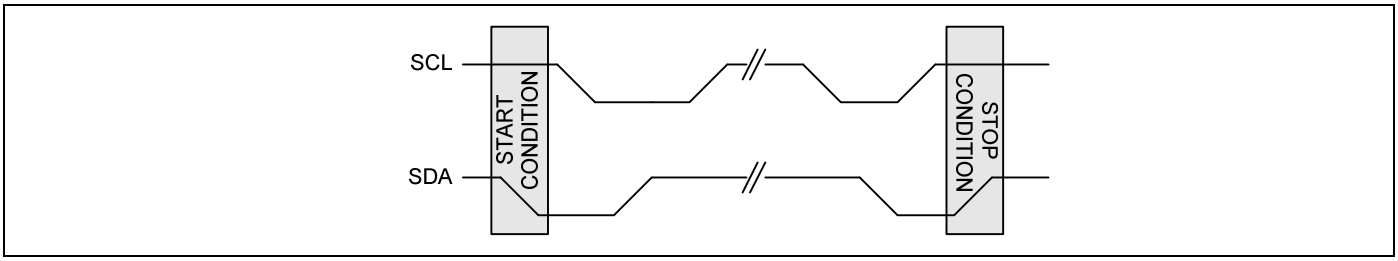


Figure 1-4. Data Validity Protocol

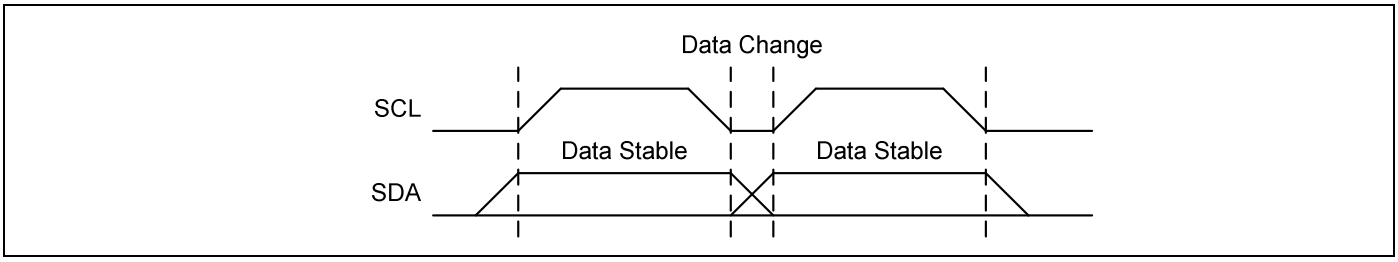


Figure 1-5. Slave Address

Bit	7	6	5	4	3	2	1	0
	1	0	1	0	A2	A1	A0	R/$\overline{W}$

Figure 1-6. Byte Write

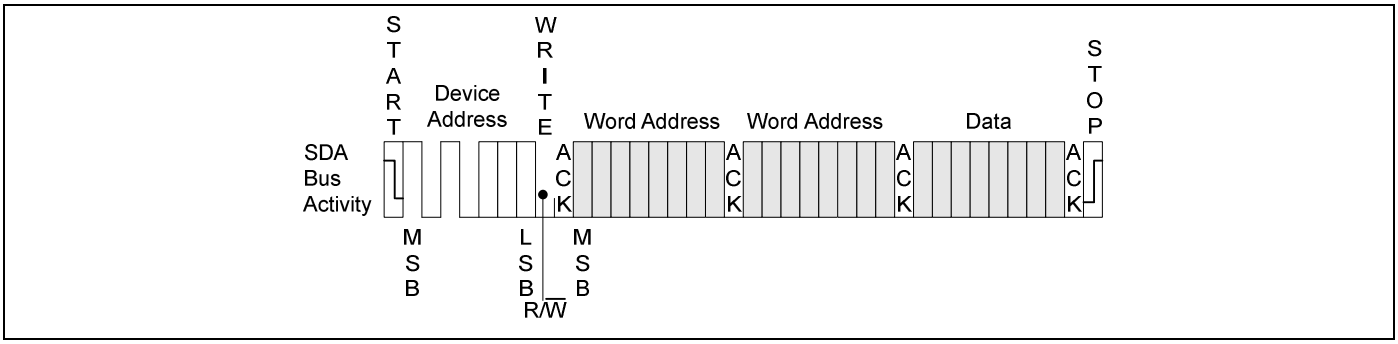


Figure 1-7. Page Write

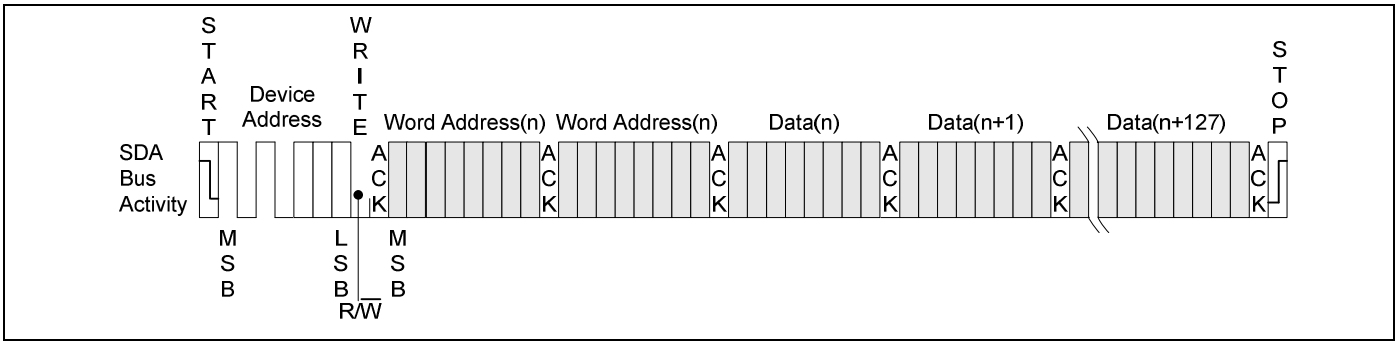


Figure 1-8. Current Address Read

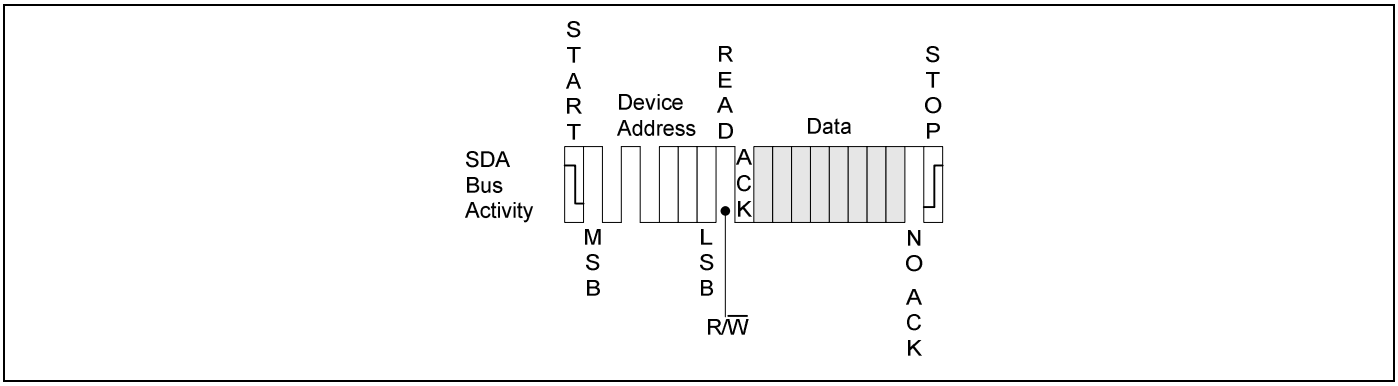


Figure 1-9. Random Address Read

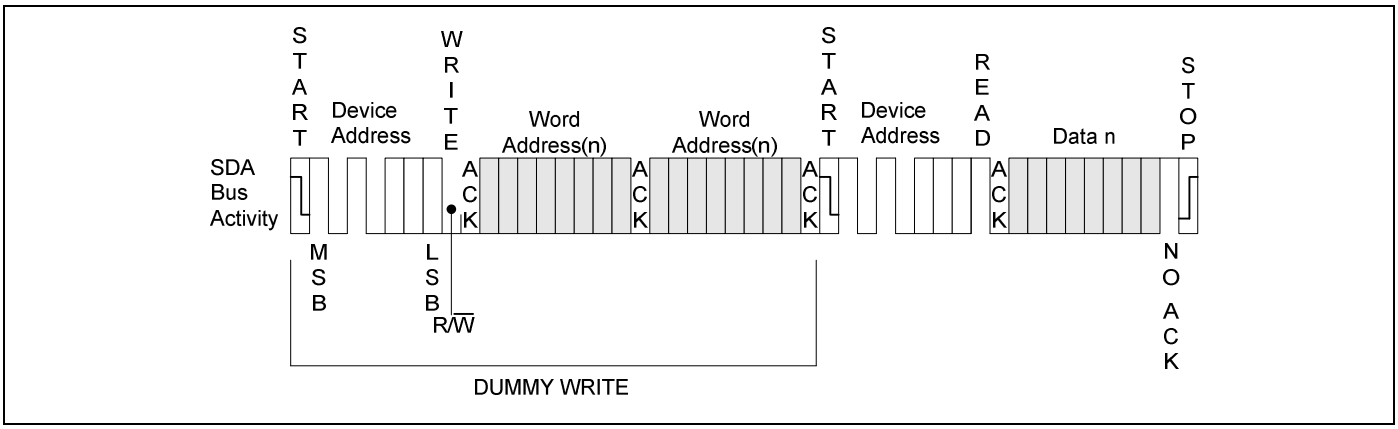
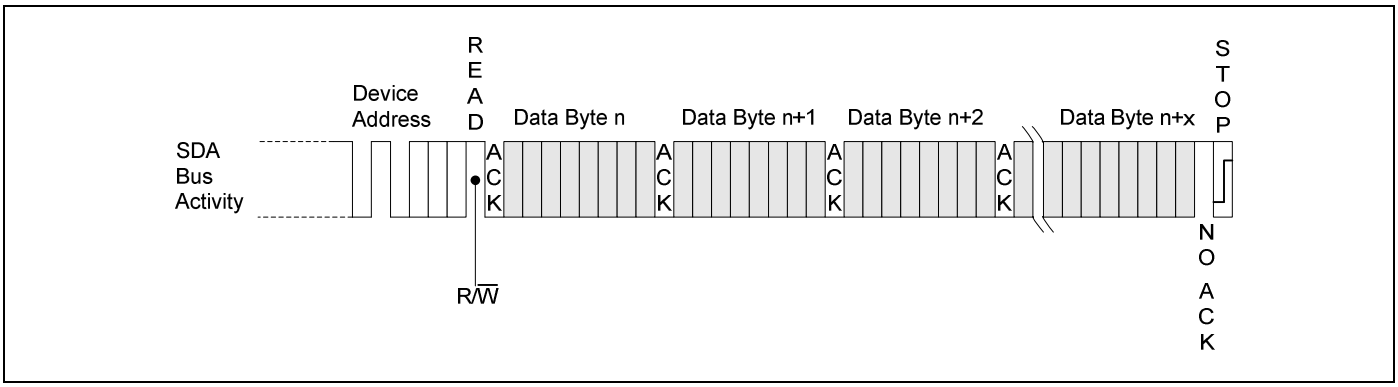


Figure 1-10. Sequential Read



Timing Diagrams

Figure 1-11. Bus Timing

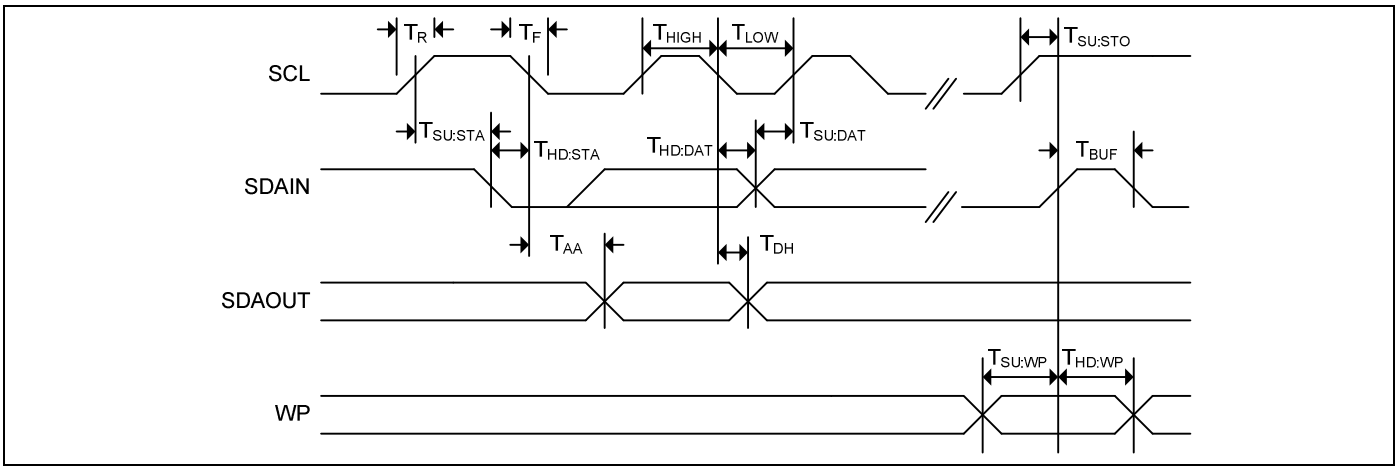
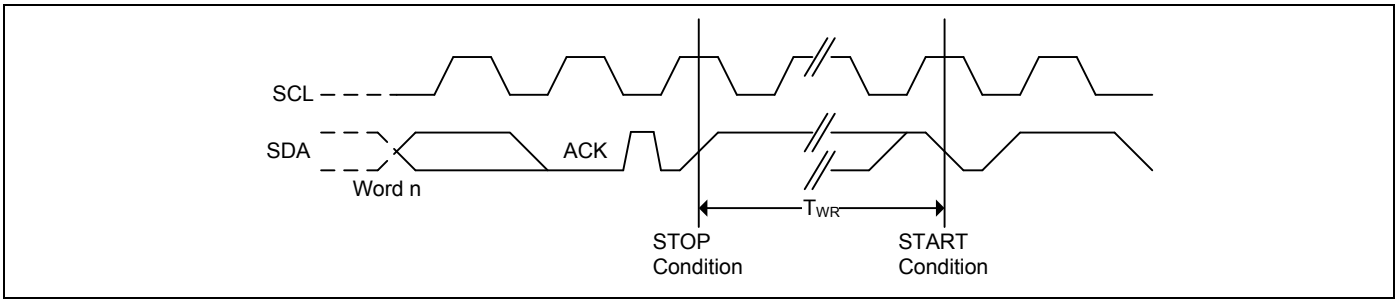


Figure 1-12. Write Cycle Timing



■ Electrical Characteristics

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	-0.5 to + 6.5	V
V_P	Voltage on Any Pin	–0.5 to V_{CC} + 0.5	V
T_{BIAS}	Temperature Under Bias	–55 to +125	℃
T_{STG}	Storage Temperature	–65 to +150	℃
I_{OUT}	Output Current	5	mA

Note: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Range

Range	Ambient Temperature (T_A)	V_{CC}
Industrial	–40℃ to +85℃	1.7V to 5.5V

Note: Industrial grade for Commercial applications (0°C to +70°C).

Capacitance

Symbol	Parameter[1, 2]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input / Output Capacitance	$V_{I/O}$ = 0V	8	pF

Notes: [1] Tested initially and after any design or process changes that may affect these parameters and not 100% tested.
[2] Test conditions: T_A = 25℃, f = 1 MHz, V_{CC} = 5.0V.

DC Electrical Characteristic

Industrial: T_A = –40°C to +85°C, V_{CC} = 1.7V ~ 5.5V

Symbol	Parameter[1]	V_{CC}	Test Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage			1.7	5.5	V
V_{IH}	Input High Voltage			0.7*V_{CC}	V_{CC}+1	V
V_{IL}	Input Low Voltage			-1	0.3* V_{CC}	V
I_{LI}	Input Leakage Current	5 V	V_{IN} = V_{CC} max	--	2	μA
I_{LO}	Output Leakage Current	5V		--	2	μA
V_{OL1}	Output Low Voltage	1.7V	I_{OL} = 0.15 mA	—	0.2	V
V_{OL2}	Output Low Voltage	3V	I_{OL} = 2.1 mA	—	0.4	V
I_{SB1}	Standby Current	1.7V	V_{IN} = V_{CC} or GND	—	1	μA
I_{SB2}	Standby Current	2.5V	V_{IN} = V_{CC} or GND	—	2	μA
I_{SB3}	Standby Current	5V	V_{IN} = V_{CC} or GND	—	3	μA
I_{CC1}	Read Current	1.7V	Read at 400 KHz	—	0.5	mA
		2.5V	Read at 1 MHz		1	mA
		5.5V	Read at 1 MHz		1	mA
I_{CC2}	Write Current	1.7V	Write at 400 KHz	—	2	mA
		2.5V	Write at 1 MHz		3	mA
		5.5V	Write at 1 MHz		3	mA

Note: The parameters are characterized but not 100% tested.

AC Electrical Characteristic

Industrial: T_A = –40°C to +85°C, Supply voltage = 1.7V to 5.5V

Symbol	Parameter [1] [2]	1.7V≤Vcc<2.5V		2.5V≤Vcc<4.5V		4.5V≤Vcc≤5.5V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
F_{SCL}	SCK Clock Frequency		400		1000		1000	KHz
T_{LOW}	Clock Low Period	1200	—	400	—	400	—	ns
T_{HIGH}	Clock High Period	600	—	400	—	400	—	ns
T_R	Rise Time (SCL and SDA)	—	300	—	300	—	300	ns
T_F	Fall Time (SCL and SDA)	—	300	—	100	—	100	ns
$T_{SU:STA}$	Start Condition Setup Time	600	—	200	—	200	—	ns
$T_{SU:STO}$	Stop Condition Setup Time	600	—	200	—	200	—	ns
$T_{HD:STA}$	Start Condition Hold Time	600	—	200	—	200	—	ns
$T_{SU:DAT}$	Data In Setup Time	100	—	40	—	40	—	ns
$T_{HD:DAT}$	Data In Hold Time	0	—	0	—	0	—	ns
T_{AA}	Clock to Output Access time (SCL Low to SDA Data Out Valid)	100	900	50	400	50	400	ns
T_{DH}	Data Out Hold Time (SCL Low to SDA Data Out Change)	100	—	50	—	50	—	ns
T_{WR}	Write Cycle Time	—	5	—	5	—	5	ms
T_{BUF}	Bus Free Time Before New Transmission	1000	—	400	—	400	—	ns
$T_{SU:WP}$	WP pin Setup Time	600	—	400	—	400		ns
$T_{HD:WP}$	WP pin Hold Time	1200	—	1200	—	1200	—	ns
T	Noise Suppression Time	—	100	—	50	—	50	ns

Notes: [1] The parameters are characterized but not 100% tested.

[2] AC measurement conditions:

R_L (connects to V_{CC}): 1.3 kΩ (2.5V, 5.0V), 10 kΩ (1.7V)

C_L = 100 pF

Input pulse voltages: 0.3*V_{CC} to 0.7*V_{CC}

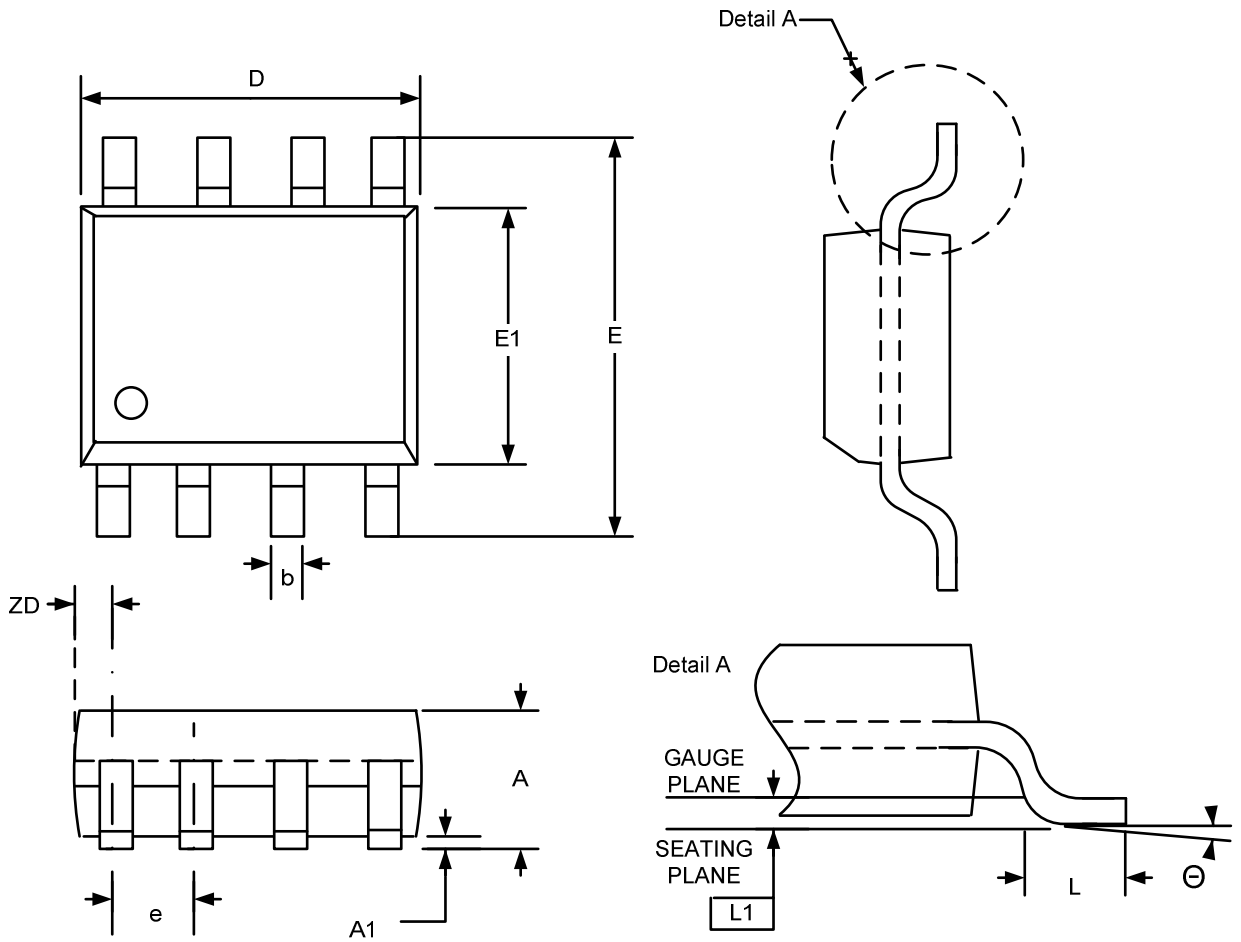
Input rise and fall times: ≤ 50 ns

Timing reference voltages: half V_{CC} level

■ Package Information

SOIC/SOP

8L 150mil SOP Package Outline

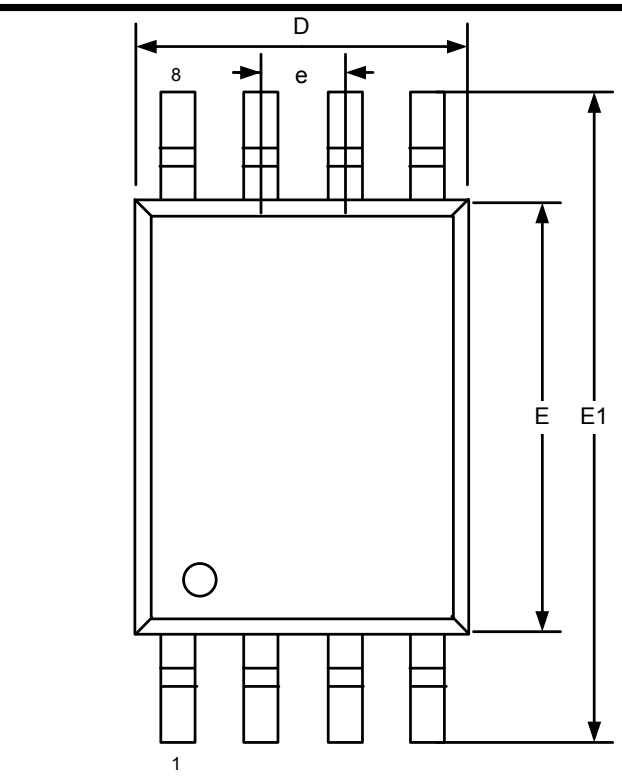


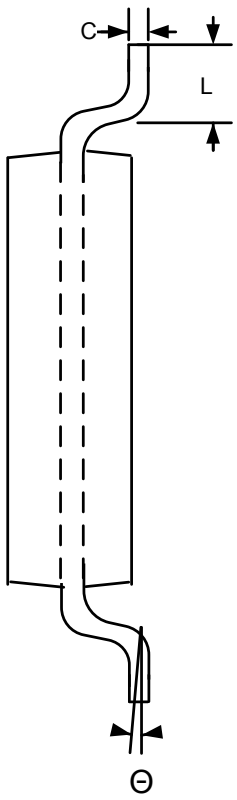
SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	--	1.75	0.053	--	0.069
A1	0.10	--	0.25	0.004	--	0.010
b	0.33	--	0.51	0.013	--	0.020
D	4.80	--	5.00	0.189	--	0.197
E	5.80	--	6.20	0.228	--	0.244
E1	3.80	--	4.00	0.150	--	0.157
e	1.27 BSC.			0.050 BSC.		
L	0.38	--	1.27	0.015		0.050
L1	0.25 BSC.			0.010 BSC.		
ZD	0.545 REF.			0.021 REF.		
Θ	0	--	8°	0	--	8°

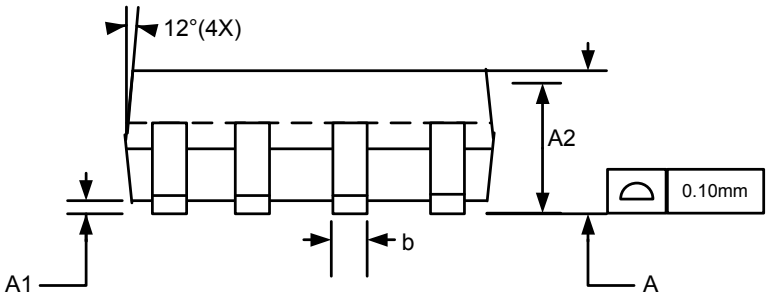
Note:
1. Controlling Dimension:MM
2. Dimension D and E1 do not include Mold protrusion
3. Dimension b does not include dambar protrusion/intrusion.
4. Refer to Jedec standard MS-012
5. Drawing is not to scale

TSSOP

8L 3x4.4mm TSSOP Package Outline





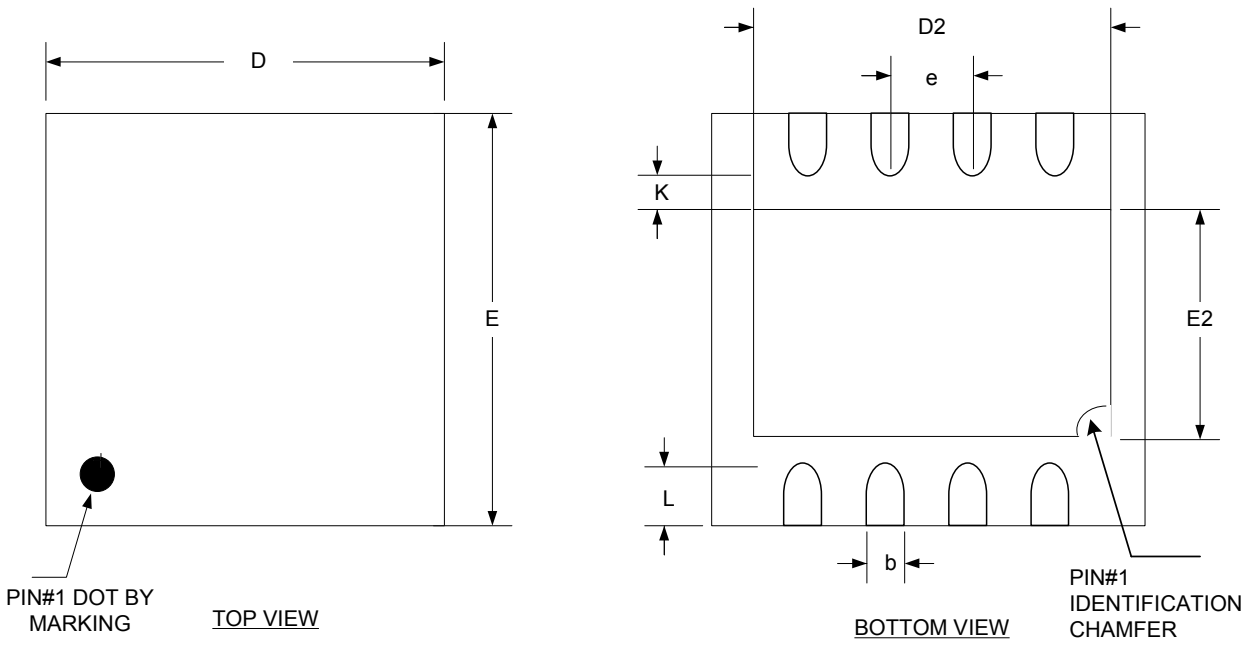


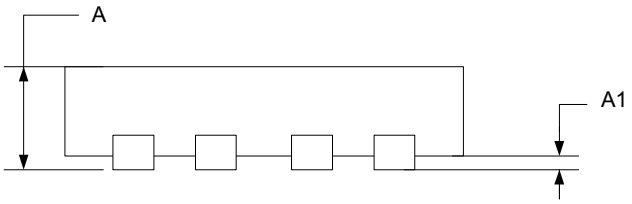
Note:
1. Controlling Dimension:MM
2. Dimension D and E1 do not include Mold protrusion
3. Dimension b does not include dambar protrusion/intrusion
4. Refer to Jedec standard MO-153 AA
5. Drawing is not to scale
6. Package may have exposed tie bar.

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	--	--	1.20	--	--	0.047
A1	0.05	--	0.15	0.002	--	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	--	0.30	0.007	--	0.012
c	0.09	--	0.20	0.004	--	0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.30	4.40	4.50	0.169	0.173	0.177
E1	6.4 BSC			0.252 BSC		
e	0.65 BSC			0.026 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
Θ	0	--	8°	0	--	8°

DFN

8L 3x3mm DFN Package Outline





SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	--	0.05	0.000	--	0.002
b	0.17	0.22	0.27	0.007	0.009	0.011
D	3.00 BSC			0.118 BSC		
D2	2.375	2.385	2.395	0.094	0.094	0.094
E	3.00 BSC			0.118 BSC		
E2	1.635	1.645	1.655	0.064	0.065	0.065
e	0.50BSC.			0.020BSC		
K	0.23	0.28	0.33	0.009	0.011	0.013
L	0.35	0.40	0.45	0.014	0.016	0.018

Note:

1. Controlling Dimension:MM
2. Drawing is not to scale