High PSRR, 600mA LDO Regulator

FEATURES

- Wide Input Voltage Range, 1.65V to 5.5V
- Available in Adjustable/Fixed Output Voltage
- Fast Transient Response
- Typical 360mV Dropout Voltage at 600mA Output Current
- Small Output Capacitor, 1uF
- Typical 50uA Quiescent Current
- Less Than 1uA Shutdown Current
- Dedicated Chip Enable Pin
- Soft Start 100us
- Over Current Limitation
- Thermal Protection
- RoHS Compliant and Halogen Free

APPLICATIONS

- Battery-Powered Equipment's
- Hand-Held Electrical Appliances
- Portable Communication Equipment's

ORDERING INFORMATION

PART	PACKAGE	RoHS	Ship, Quantity
ZTP7001T-00	TSOT23-5L	Yes	Tape and Reel
ZTP7001DA	TDFN2×2-6L	Yes	Tape and Reel
ZTP7001Dxx	TDFN2×2-6L	Yes	Tape and Reel

The last letter(s) of PART No. denote the Output Voltage: -00 = adjustable;A = adjustable; xx = 12: 1.2V; xx = 15: 1.5V;xx = 18: 1.8V; xx = 25: 2.5V; xx = 28: 2.8V; xx = 30: 3.0V;xx = 33: 3.3V.

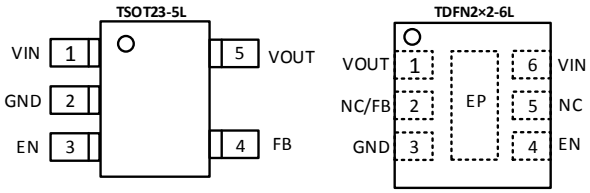
DESCRIPTION

The ZTP7001 is a high performance LDO regulator specifically designed to deliver adjustable output voltage with high PSRR and fast transient response. Internal 700mohm PMOS pass transistor yields typical 360mV dropout voltage at 600mA output current.

Typical quiescent current is only 50uA. A logic low on the enable input, EN, shuts down the output and reduces the supply current to less than 1uA. The ZTP7001 works stably with as low as 1uF ceramic output capacitor, minimizing board space requirement.

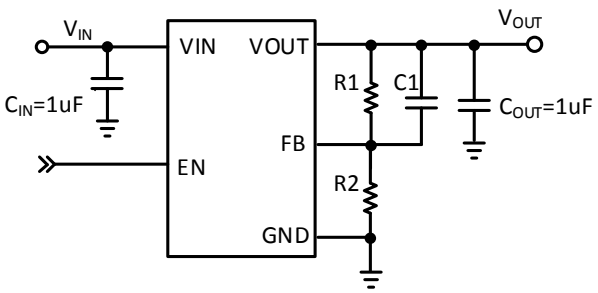
Other features include soft start, high output accuracy, output current limiting, and thermal protection. The ZTP7001 is available in the TSOT23-5L and TDFN2×2-6L package.

Pins Configuration

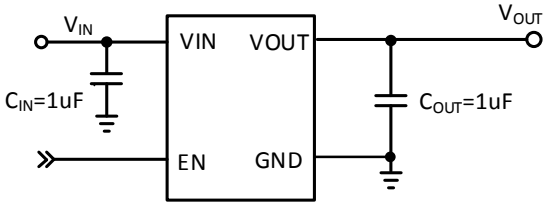


Typical Application Circuits

Adjustable Voltage Regulator



Fixed Voltage Regulator



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Absolute Maximum Ratings

Input Supply Voltage V_{IN} ..... –0.3V to +6.0V
Voltage at EN ..... –0.3V to +6.0V
Others ..... –0.3V to (V_{IN} + 0.3V)
Maximum Power Dissipation P_D@T_A = 25°C 0.4W
Junction Temperature..... 150°C
ESD (Human Body Mode) 2kV
ESD (Machine Mode) 200V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Package Thermal Characteristics

Thermal Resistance, θ_{JA} ..... 250°C /W
Thermal Resistance, θ_{JC} ..... 25°C/W

Electro-Static Discharge Sensitivity

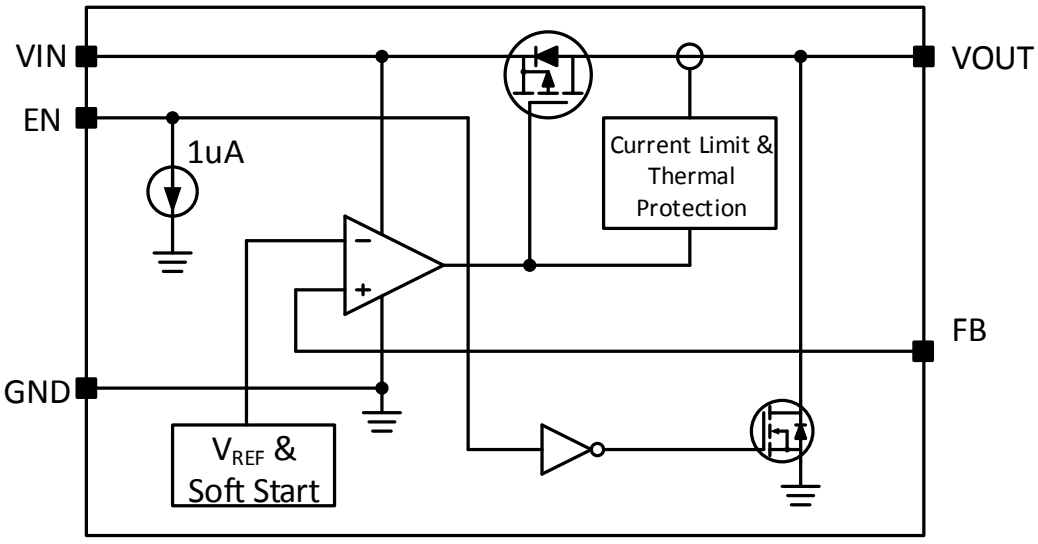
This integrated circuit can be damaged by ESD. It is recommended that all integrated circuits be handled with proper precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure.

Pins Description

TSOT23-5L	Symbol	Description
1	VIN	Input Voltage.
2	GND	Ground.
3	EN	Active High Chip Enable.
4	FB	Output Voltage Feedback.
5	VOUT	Output Voltage.

TDFN2×2-6L	Symbol	Description
1	VOUT	Output Voltage.
2	NC/FB	Not Connected. /Output Voltage Feedback.
3	GND	Ground.
4	EN	Active High Chip Enable.
5	NC	Not Connected.
6	VIN	Input Voltage.

Functional Block Diagram



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Recommended Operation Conditions

PARAMETER	MIN	TYP	Max	Unit
Continuous Junction Temperature	–40	--	125	°C
Ambient Temperature Range	–40	--	85	°C
Input Voltage Range	1.65	--	5.5	V

Electrical Specifications

V_{IN} = V_{EN} = 3.3V and T_A = 25°C unless otherwise specified

PARAMETER	Symbol	TEST CONDITIONS	MIN	TYP	Max	Unit
Input Supply Voltage	V_{IN}		1.65	--	5.5	V
VIN Under Voltage Lockout	V_{UVLO}		--	1.5	1.6	V
Shutdown Current	I_{SD}	V_{EN} = 0V	--	--	1	uA
Quiescent Current	I_Q	I_{OUT} = 0mA	--	50	--	uA
FB Pin Voltage	V_{FB}	I_{OUT} = 10mA	784	800	816	mV
Maximum Output Current	I_{OUT}		600	800	--	mA
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	1mA < I_{OUT} < 600mA	--	30	50	mV
On-Resistance of Pass Element	$R_{DS(ON)}$		--	700	--	mΩ
Dropout Voltage	V_{DP}	I_{OUT} = 600mA	--	360	--	mV
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{OUT} + 0.42V < V_{IN} < 5.5V	--	0.02	--	%/V
Output Noise		BW = 10Hz to 100kHz, I_{OUT} = 10mA	--	70	--	uVrms
Power Supply Ripple Rejection	PSRR	I_{OUT} = 10mA, f = 1kHz	--	70	--	dB
		I_{OUT} = 10mA, f = 10kHz	--	60	--	dB
Short Circuit Limit		V_{OUT} = 0V	--	100	--	mA
EN Pull-Down Constant Current	I_{EN}	V_{EN} = 3.3V	--	1	--	uA
EN Input High Threshold	V_{IH}		1.6	--	--	V
EN Input Low Threshold	V_{IL}		--	--	0.4	V
Soft Start Time	t_{SS}		--	100	--	uS
Thermal Shutdown Temperature	T_{SD}		--	160	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	30	--	°C

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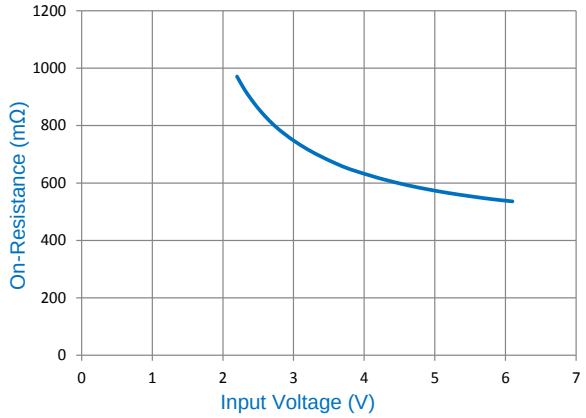
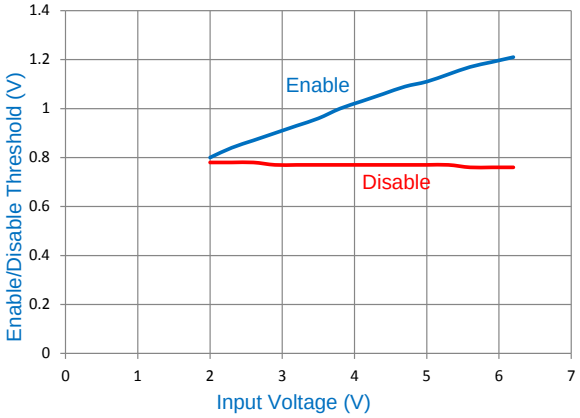
Typical Characteristics

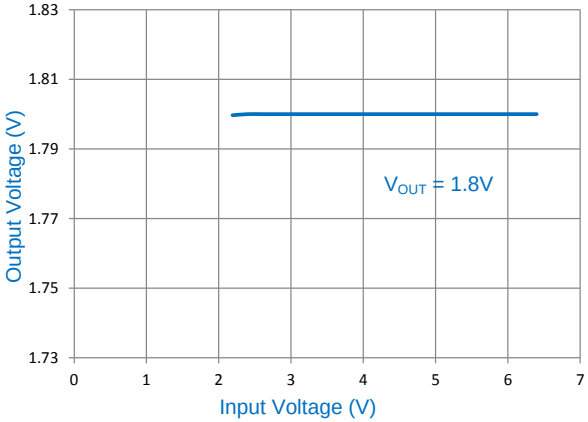
On-Resistance vs. Input Voltage



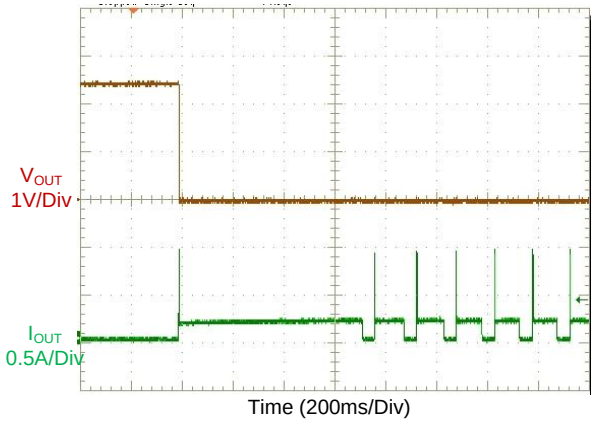
Enable Disable Threshold vs. Input Voltage



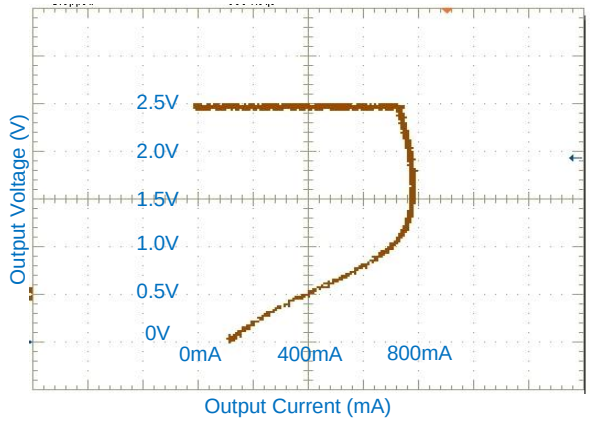
Line Regulation



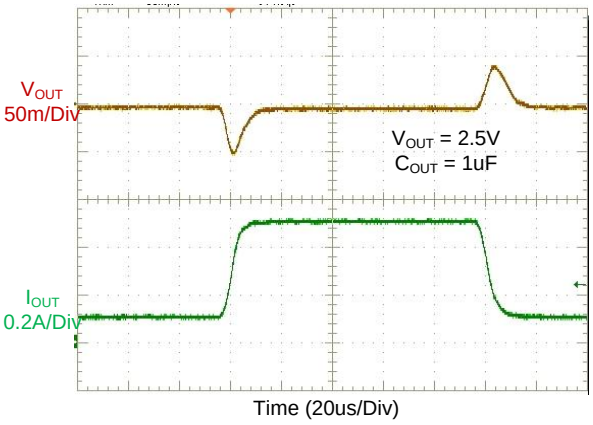
Output Short Circuit Response



Output Current Limit



Load Transient Response



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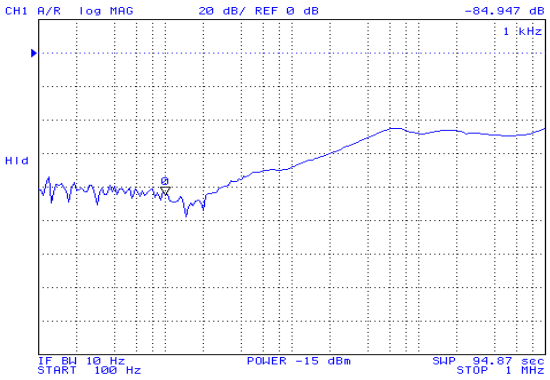
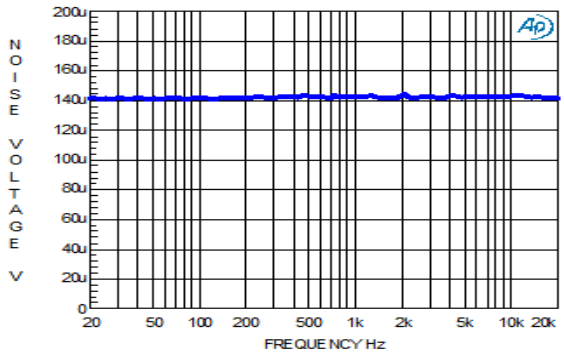
PSRR



V_{IN} = 3.3V, V_{OUT} = 1.6V, I_{OUT} = 100mA

Noise Level



V_{IN} = 3.3V, V_{OUT} = 1.6V, I_{OUT} = 100mA

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Functional Pin Description

VIN: Input Voltage. Connect a minimum 1uF ceramic capacitor to this pin for stable operation.

GND: Ground.

EN: Active High Chip Enable. This pin is internally pulled down by a 1uA current source.

FB: Output Voltage Feedback. The FB voltage is regulated to 0.8V. Connect a resistive voltage divider to set the output voltage.

VOUT: Output Voltage. Connect a minimum 1uF ceramic capacitor to this pin for stable operation.

OPERATION PRINCIPLES

The ZTP7001 low dropout regulator (LDO) operates with a very low input voltage (>1.65V). The ZTP7001 can operate at low input voltage due to low voltage circuit design techniques and a PMOS pass element that exhibits low dropout. The dropout voltage is typically 360mV at 600mA output current.

Chip Enable

Typical quiescent current is only 50uA. A logic low on the enable input, EN, shuts down the output and reduces the supply current to less than 1uA. The EN pin is internally pulled down by a 1uA current source and may be tied to VIN in applications where the shutdown feature is not used.

Output Discharging Resistor

An internal 100Ω MOSFET is connected to VOUT pin and discharges the output voltage to ground when the chip is disabled or thermal protection is triggered.

Soft Start

The ZTP7001 features soft start and the soft start time is fixed as 100us.

Output Voltage Programming

The output voltage of the ZTP7001 adjustable regulator is programmed using an external resistive divider as shown in the typical application circuit. The output voltage is calculated as:

$$V_{OUT} = V_{REF} \times \frac{R1 + R2}{R2}$$

Where V_{REF} = 0.8V typ (the internal reference voltage.)

Resistors R1 and R2 should be chosen for approximately 10uA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error.

Current Limit and Thermal Protection

Current limiting and thermal protection prevent damage by excessive output current and/or power dissipation. The device switches into a constant-current mode at approximately 800mA. Further load reduces the output voltage instead of increasing the output current. The thermal protection shuts the regulator off if the junction temperature rises above 160°C. Recovery is automatic when the junction temperature drops approximately 30°C below the high temperature trip point.

Pass Element

The ZTP7001 integrates a 700mΩ PMOS pass element that enables very low dropout voltage. The PMOS pass element includes a back diode that safely conducts reverse current when the input voltage level drops below the output voltage level.

Application Information

Capacitors Selection

Select carefully the external capacitors carefully to ensure stability and performance. Place the externally capacitors close to the IC with a distance no longer than 0.5 inches.

The input capacitor C_{IN} with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response.

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The ZTP7001 is specifically designed to work with low ESR ceramic output capacitor in space-saving and performance consideration. A 1uF ceramic capacitor is adequate for stable operation. However, for best load and line transient response, output capacitor larger than 4.7uF is recommended.

Power Supply Rejection Ration (PSRR)

PSRR is a measure of how well a circuit rejects ripple coming from the input power supply at various frequencies and is very critical in many RF and wireless applications. PSRR is defined as the gain from the input ripple to output ripple over a wide frequency range (10Hz to 10MHz), Note that at heavy load measuring, ΔV_{IN} will cause temperature deviation. Temperature will cause ΔV_{OUT} voltage. So the heavy load PSRR measuring includes temperature effect.

Thermal Consideration

The maximum power dissipation is specified as:

$$P_{D(MAX)} = \frac{(125°C - TA)}{\theta_{JA}}$$

where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and θ_{JA} is the junction to ambient thermal resistance.

The ZTP7001 features thermal protection that shuts down the IC if the junction temperature is higher than 160°C. However, the power dissipation should be well designed to keep the continuous junction temperature below 125°C for maximum reliability.

θ_{JA} depends on the thermal resistance of the package, PCB layout, surrounding airflow. For SOT-23-5 package, the thermal resistance θ_{JA} is 250°C /W on the standard JEDEC 51-3 single layer thermal test board. The maximum power dissipation at TA = 25°C can be calculated as:

$$P_{D(MAX)} = \frac{(125°C - 25°C)}{250°C/W} = 0.4W$$

Because of the small size of the TSOT23-5 package, it is very important to use a good thermal PC board layout to maximize the allowable power dissipation. The thermal path for the heat generated by the IC is from the die to the copper lead frame, through the package (especially the ground lead), to the PCB board cooper. The PC board copper. The PCB board copper is the heat sink. The footprint copper pads should be as wide as possible and expand out to larger copper areas to spread and dissipate the heat to the surrounding ambient. Feed through via to inner or backside copper layer are also useful in improving the overall thermal performance of the LDO regulator. Other heat sources on the board, not related to the LDO regulator, must also be considered when designing a PC board layout because they will affect overall temperature rise and the maximum allowable power dissipation. The following table lists thermal resistance for several different board sizes and copper areas. All measurements were taken in still air on 3/32" FR-4 board with the device mounted on topside.

Table 1. Measured Thermal Resistance (2-Layer Board)

Copper Area(mm2)		Board Area (mm2)	θ_{JA} (°C/W)
Top Side	Back Side		
2500	2500	2500, 2-Layer	125
1000	2500	2500, 2-Layer	125
225	2500	2500, 2-Layer	130
100	2500	2500, 2-Layer	135
50	2500	2500, 2-Layer	150

Layout Considerations

Careful PCB Layout is necessary for better performance. The following guidelines should be followed for good PCB layout.

- Place the input and output capacitors as close as possible to the IC.
- Keep V_{IN} and V_{OUT} trace as possible as short and wide.
- Use a large PCB ground plane for maximum thermal dissipation.

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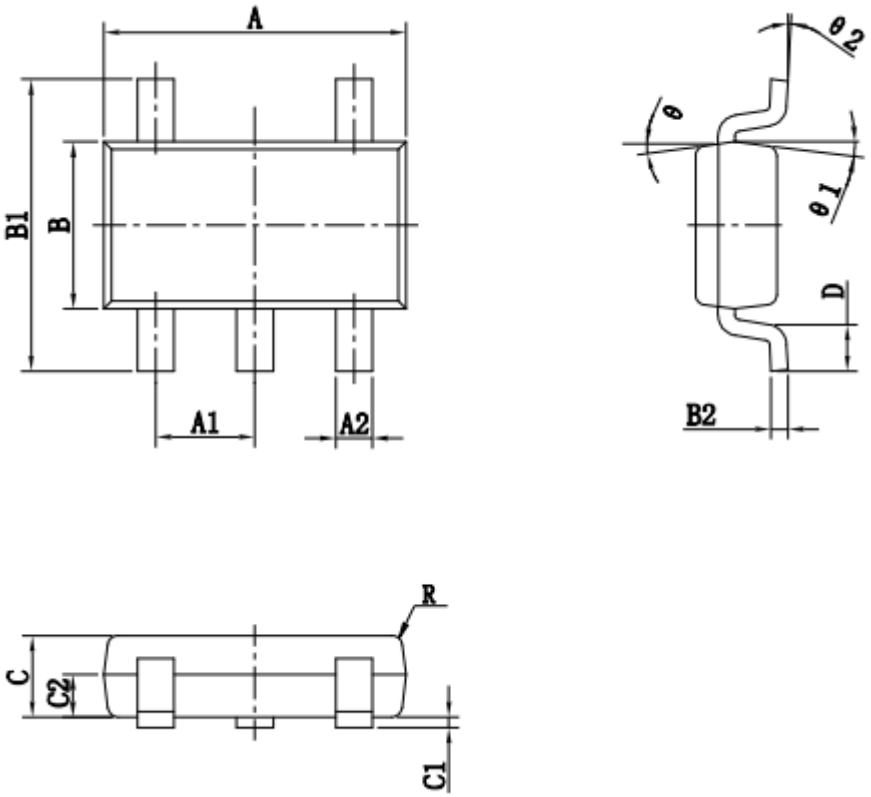
PACKAGE DIMENSIONS TSOT23-5L



Symbol	Dimensions in mm	
	Min	Max
A	2.820	3.020
A1	0.950 BSC	
A2	0.350	0.500
B	1.600	1.700
B1	2.650	2.950
B2	0.080	0.200
C	0.700	0.800
C1	0.000	0.100
C2	0.378	0.438
D	0.300	0.600
θ	9° TYP4	
θ 1	10° TYP4	
θ 2	0~8°	

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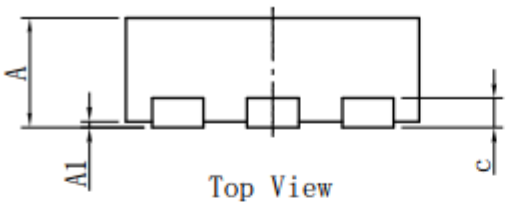
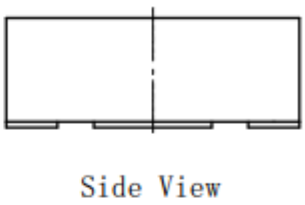
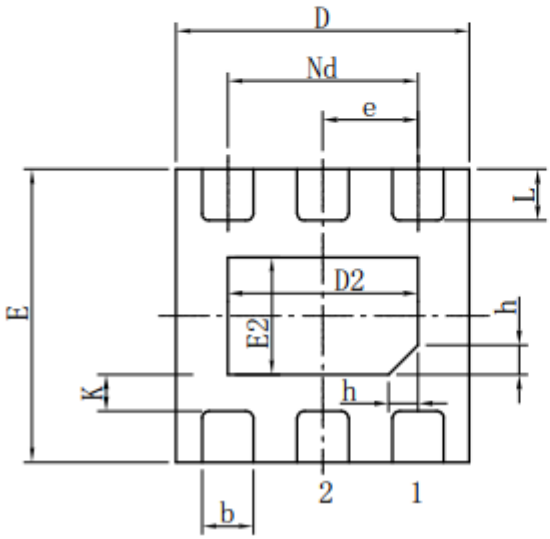
PACKAGE DIMENSIONS TDFN2x2-6L







Symbol	Dimensions in mm	
	Min	Max
A	0.70	0.80
A1	0.00	0.05
b	0.30	0.40
c	0.18	0.25
D	1.95	2.05
D2	1.25	1.35
E	1.95	2.05
E2	0.75	0.85
e	0.650BSC	
Nd	1.300BSC	
K	0.20	-
L	0.28	0.38
h	0.15	0.25

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