24LC01/24AA01 1K

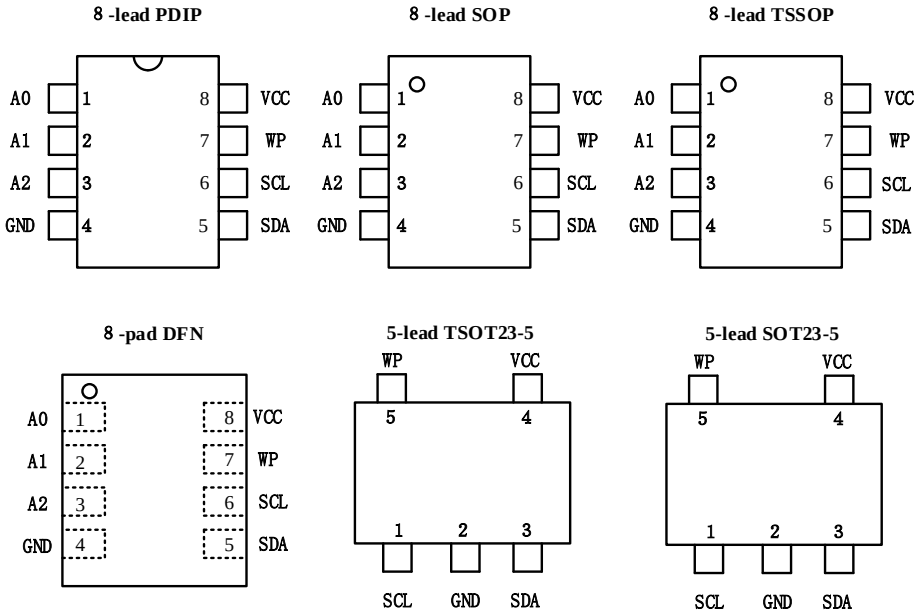
bits (128×8)**Features**

- Compatible with all I²C bidirectional data transfer protocol
- Memory array:
  - 1 Kbits (256bytes) of EEPROM
  - Page size: 16 bytes
- Single supply voltage and high speed:
  - 1MHz
  - Random and sequential Read modes
- Write:
  - Byte Write within 3 ms
  - Page Write within 3 ms
  - Partial Page Writes Allowed
- Write Protect Pin for Hardware Data Protection
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- High-reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
- Enhanced ESD/Latch-up protection
  - HBM 6000V
- 8-lead PDIP/SOP/TSSOP/ UDFN/TSOT23-5 and SOT23-5 packages

Description

- The24LC01/24AA01 provides 2048 bits of serial electrically erasable and programmable read-only memory (EEPROM), organized as 256 words of 8 bits each.
- The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential.

Pin Configuration



Examples

型号	封装	私印	工作电压	兼容电压
24LC01B-I/P-TUDI	DIP8	24LC01B-I/P	1.8-5.5	
24LC01BT-I/SN-TUDI	SOP8	24LC01BI/SN	1.8-5.5	
24LC01BT-I/ST-TUDI	TSSOP8	24LC01B	1.8-5.5	
24LC01BT-I/OT-TUDI	SOT23-5	M1QU	1.8-5.5	
24AA01T-I/SN-TUDI	SOP8	24AA01I/SN	1.8-5.5	1.7V
24AA01T-I/ST-TUDI	TSSOP8	24AA01	1.8-5.5	1.7V
24AA01T-I/OT-TUDI	SOT23-5	B1QA	1.8-5.5	1.7V

Pin Descriptions

Pin Name	Type	Functions
A0-A2	I	Address Inputs
SDA	I/O	Serial Data
SCL	I	Serial Clock Input
WP	I	Write Protect
GND	P	Ground
Vcc	P	Power Supply

Table 1

Block Diagram

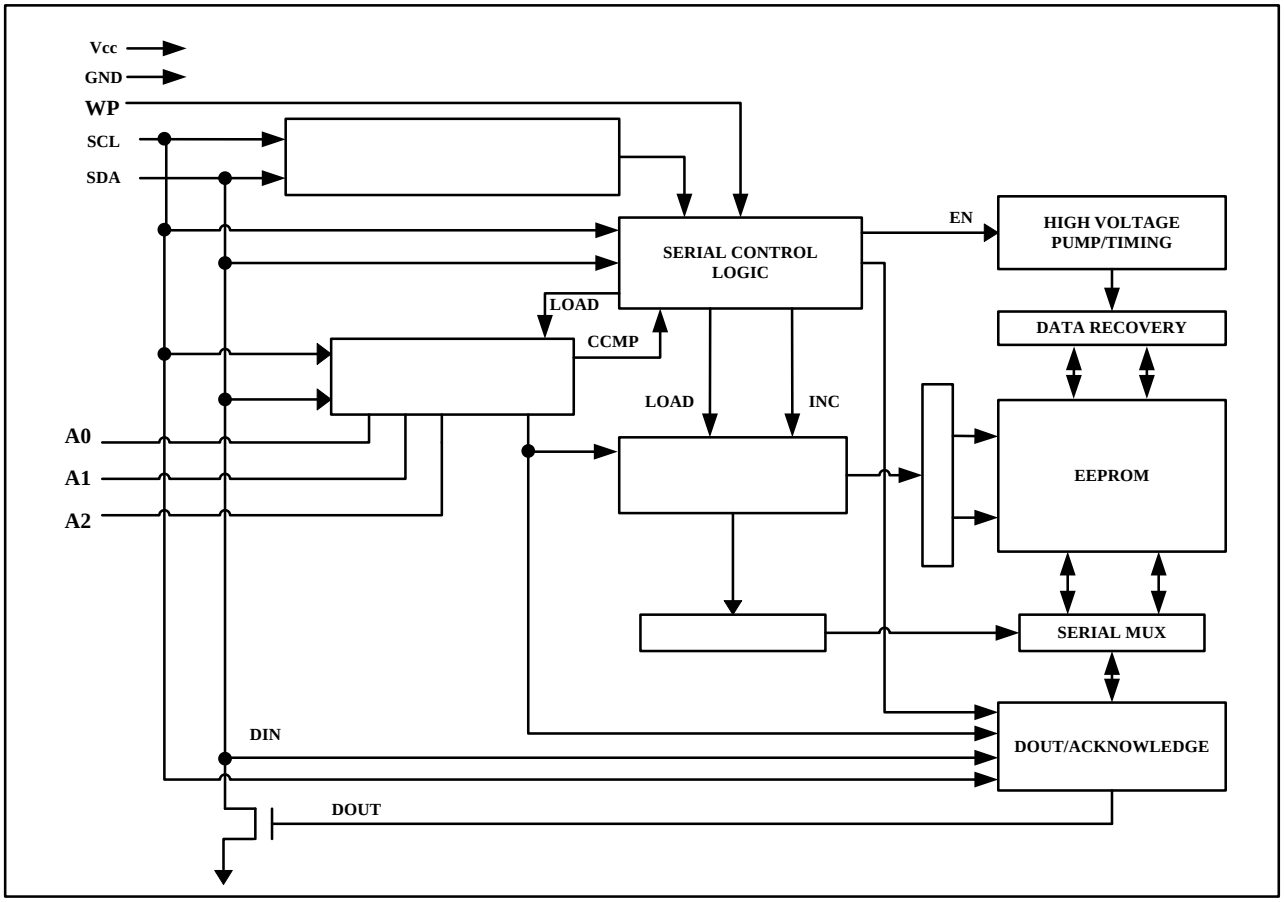


Figure 1

DEVICE/PAGE ADDRESSES (A2, A1 and A0): The A2, A1 and A0 pins are device address inputs that are hard wire for the 24LC01/24AA01 . Eight 2K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open- collector devices.

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

WRITE PROTECT (WP): The 24LC01/24AA01 has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protection pin is connected to Vcc,
the write protection feature is enabled and operates as shown in the following **Table 2**.

WP Pin Status	24LC01/24AA01
At VCC	Full(2K) Array
At GND	Normal Read/Write Operations

Table 2

Functional Description

1. Memory Organization

24LC01/24AA01 , 2K SERIAL EEPROM: Internally organized with 16 pages of 16 bytes each, the 2K requires a 8-bit data word address for random word addressing.

2. Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see **Figure 2**). Data changes during SCL high periods will indicate a start or stop condition as defined below.

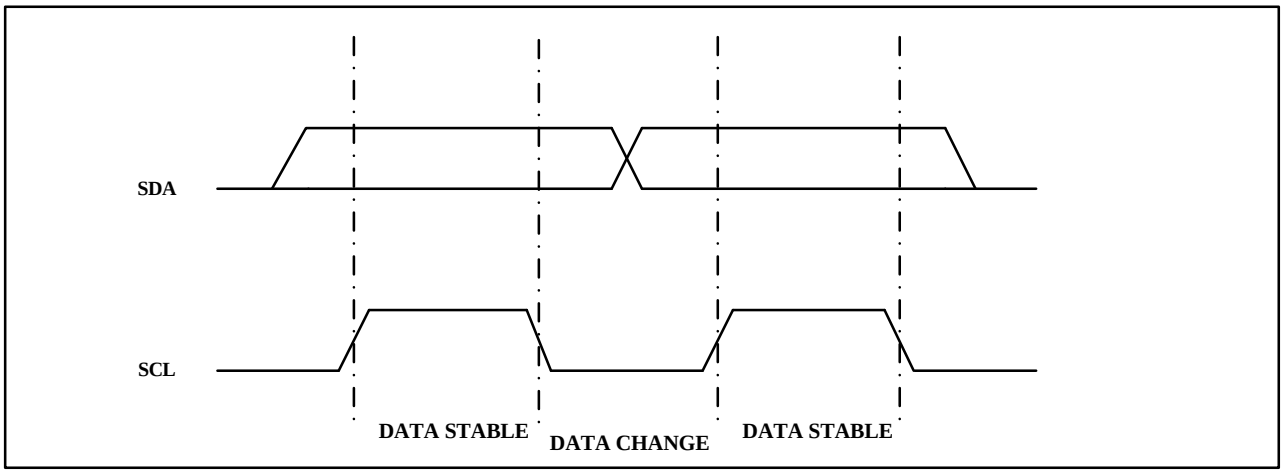


Figure 2. Data Validity

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see **Figure 3**).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see **Figure 3**).

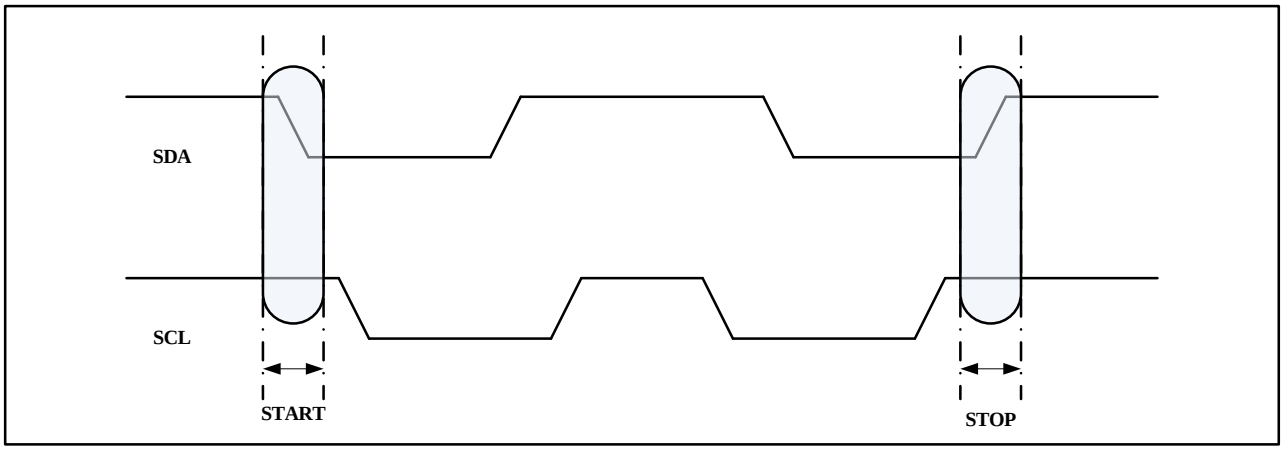


Figure 3. Start and Stop Definition

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a "0" to acknowledge that it has received each word. This happens during the ninth clock cycle.

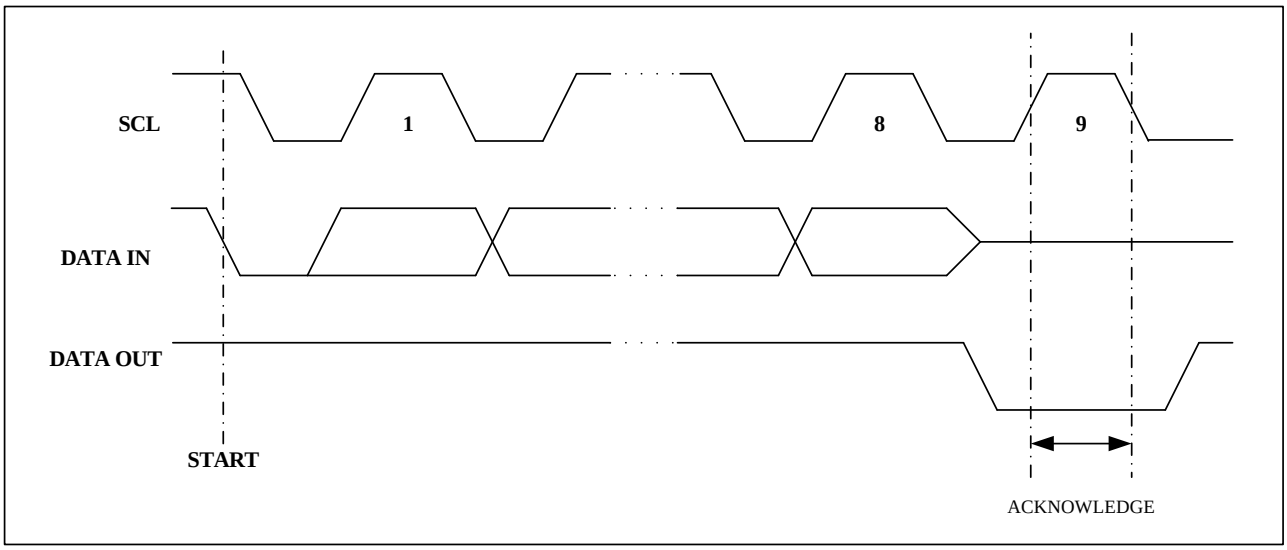


Figure 4. Output Acknowledge

STANDBY MODE: The 24LC01/24AA01 features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

MEMORY RESET: After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps:

1. Clock up to 9 cycles.
2. Lock SDA high in each cycle while SCL is high.
3. Create a start condition.

3. Device Addressing

The 2K EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation (see **Figure 5**)

MSB							LSB
1	0	1	0	A2	A1	A0	R/W

Figure 5. Device Address

The device address word consists of a mandatory "1", "0" sequence for the first four most significant bits as shown. This is common to all the Serial EEPROM devices.

The 2K EEPROM uses A2, A1 and A0 device address bits to allow as much as eight devices on the same bus. These 3 bits must be compared to their corresponding hardwired input pins. The A2, A1 and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a "0". If a compare is not made, the chip will return to a standby state.

DATA SECURITY: The 24LC01/24AA01 has a hardware data protection scheme that allows the user to

write
protect the entire memory when the WP pin is at VCC.

4. Write Operations

BYTE WRITE: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, tWR, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see **Figure 7**).

B7	B6	B5	B4	B3	B2	B1	B0

Figure 6. ADDRESS

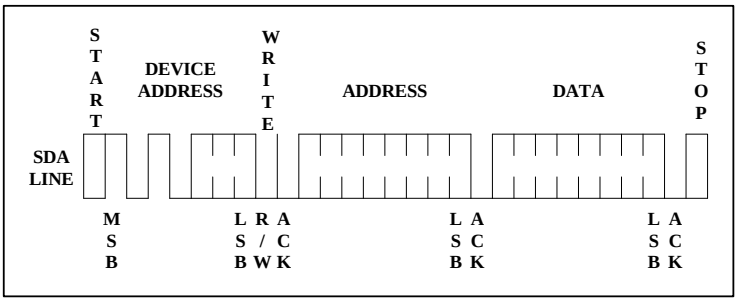


Figure 7. Byte Write

PAGE WRITE: The 2K EEPROM is capable of a 16-byte page write. A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to fifteen more data words. The EEPROM will respond with a "0" after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see **Figure 8**).

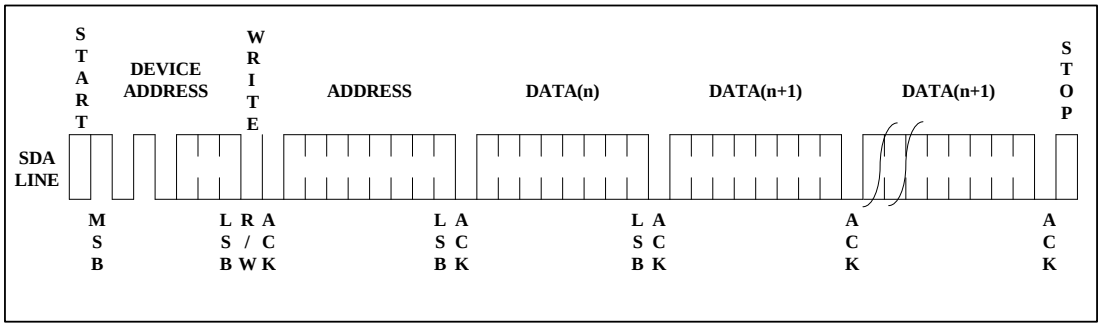


Figure 8. Page Write

The data word address lower four bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than sixteen data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a "0", allowing the read or write sequence to continue.

5. Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page. Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see **Figure 9**).

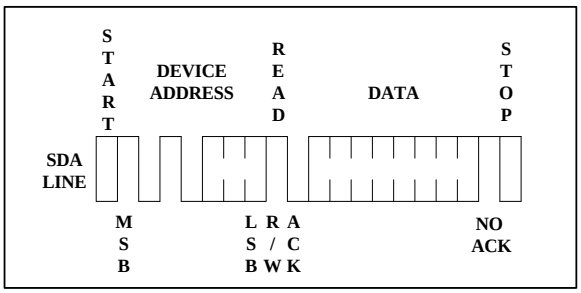


Figure 9. Current Address Read

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition (see **Figure 10**)

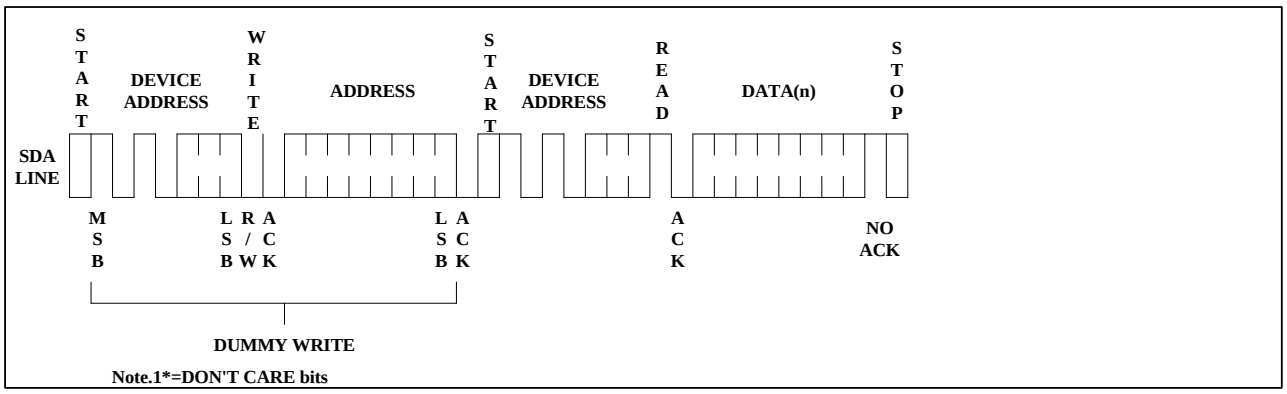


Figure 10. Random Read

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a "0" but does generate a following stop condition (see **Figure 11**).

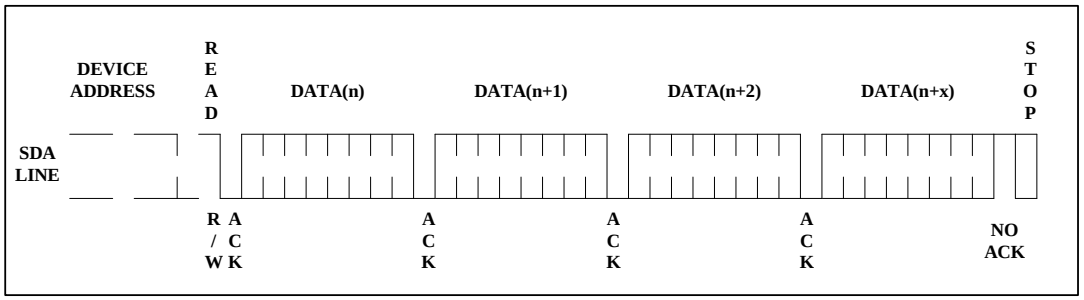


Figure 11. Sequential Read

Electrical Characteristics

Absolute Maximum Stress Ratings:

- DC Supply Voltage . . . . . -0.3V to +6.5V
- Input / Output Voltage . . . . . GND-0.3V to VCC+0.3V
- Storage Temperature . . . . . .-65℃ to +150℃
- Electrostatic pulse (Human Body model) 6000V

Comments:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

24LC01/24AA01	T_A =-40℃ to +85℃	V_{CC} = +1.7V to +5.5V@400kHz V_{CC} = +2.5V to +5.5V@1MHz C_L=100 pF
24LC01/24AA01 E1	T_A =-40℃ to +105℃	
24LC01/24AA01 E0	T_A =-40℃ to +125℃	

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Supply Voltage	V_{CC1}	1.7	-	5.5	V	@400kHz
Supply Voltage	V_{CC2}	2.5	-	5.5	V	@1MHz
Supply Current V_{CC}=5.0V	I_R	-	0.14	0.3	mA	READ @ 400kHz
Supply Current V_{CC}=5.0V	I_W	-	0.28	0.5	mA	WRITE @ 400kHz
Supply Current V_{CC}=5.0V	I_{SB}	-	0.03	0.5	μA	V_{IN}=V_{CC} or V_{SS}
Input Leakage Current	I_{LI}	-	0.10	1.0	μA	V_{IN}=V_{CC} or V_{SS}
Output Leakage Current	I_{LO}	-	0.05	1.0	μA	V_{OUT}=V_{CC} or V_{SS}
Input Low Level	V_{IL}	-0.3	-	V_{CC}×0.3	V	V_{CC}=1.7V to 5.5V
Input High Level	V_{IH}	V_{CC}×0.7	-	V_{CC}+0.3	V	V_{CC}=1.7V to 5.5V
Output Low Level V_{CC}=1.7V	V_{OL1}	-	-	0.2	V	I_{OL}=0.15mA
Output Low Level V_{CC}=5.0V	V_{OL2}	-	-	0.4	V	I_{OL}=3.0mA

Table 3

Pin Capacitance

Applicable over recommended operating range from T_A = 25℃, f_{SCL} = 1.0 MHz, V_{CC} = +2.5V

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Input/Output Capacitance(SDA)	$C_{I/O}$	-	-	8	pF	V_{IO}=0V
Input Capacitance(A0,A1,A2,SCL)	C_{IN}	-	-	6	pF	V_{IN}=0V

Table 4

AC Electrical Characteristics

Applicable over recommended operating range from (unless otherwise noted):

24LC01/24AA01	T_A =-40℃ to +85℃	V_{CC} = +1.7V to +5.5V@400kHz V_{CC} = +2.5V to +5.5V@1MHz C_L=100 pF
24LC01/24AA01 E1	T_A =-40℃ to +105℃	
24LC01/24AA01 E0	T_A =-40℃ to +125℃	

Parameter	Symbol	Min.	Max.	Units
Clock Frequency, SCL	f_{SCL}	-	1000	kHz
Clock Pulse Width Low	t_{LOW}	0.5	-	μs
Clock Pulse Width High	t_{HIGH}	0.26	-	μs
Noise Suppression Time	t_I	-	50	ns
Clock Low to Data Out Valid	t_{AA}	-	0.45	μs
Time the bus must be free before a new transmission can start	t_{BUF}	0.5	-	μs
Start Hold Time	$t_{HD:STA}$	0.26	-	μs
Start Setup Time	$t_{SU:STA}$	0.26	-	μs
Data In Hold Time	$t_{HD:DAT}$	0	-	μs
Data In Setup Time	$t_{SU:DAT}$	50	-	ns
Input Rise Time(1) (2)	t_R	-	-	ns
Input Fall Time(1) (2)	t_F	-	-	ns
Stop Setup Time	$t_{SU:STO}$	0.26	-	μs
Data Out Hold Time	t_{DH}	50	-	ns
Write Cycle Time	t_{WR}	-	3	ms
5.0V,25℃,Byte Mode(1)	Endurance	1M	-	Write Cycle

Table 5

Notes:

1. This parameter is ensured by characterization only.
2. There is no min. or max. values for the input signal rise and fall times. It is however recommended by the I²C specification that the input signal rise and fall times be less than 120 ns when f_{SCL} < 1 MHz, more than 20 ns and less than 300 ns when f_{SCL} < 400 kHz.
3. AC measurement conditions:

   R_L (connects to V_{CC}): 1.3 kΩ

   Input pulse voltages: 0.3 V_{CC} to 0.7 V_{CC}
   Input rise and fall time: 50 ns
   Input and output timing reference voltages: 0.5 V_{CC}
   The value of R_L should be concerned according to the actual loading on the user's system.

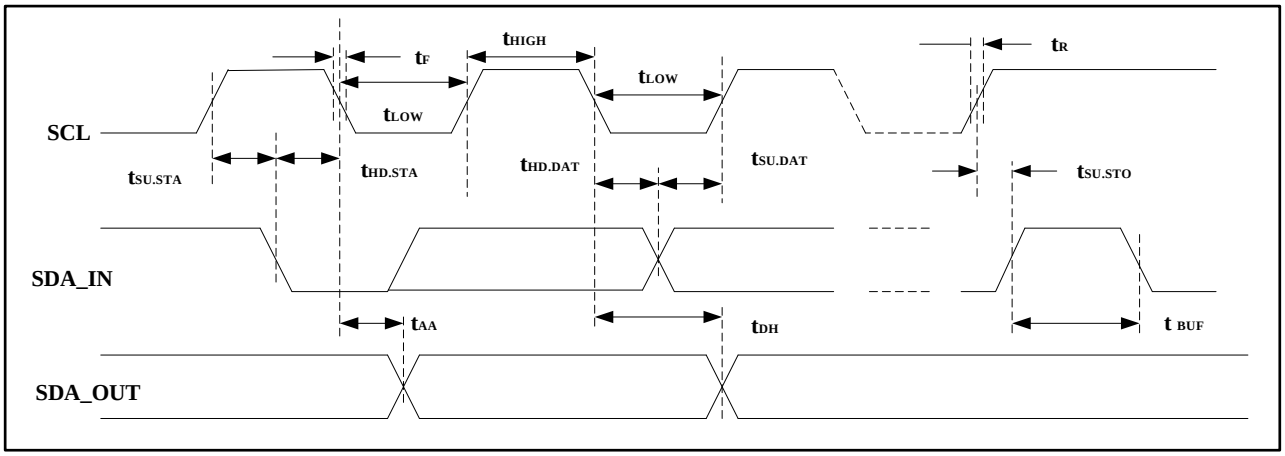


Figure 12. SCL: Serial Clock, SDA: Serial Data I/O

Write Cycle Timing

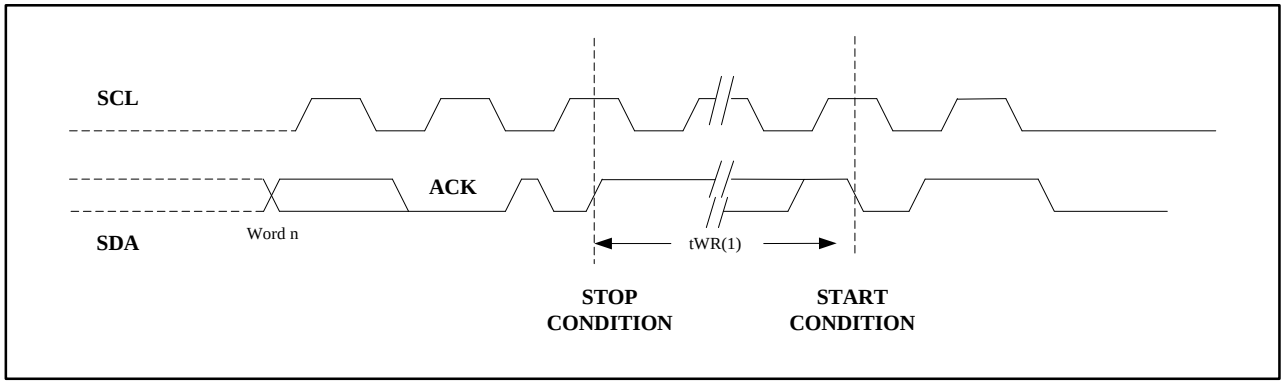
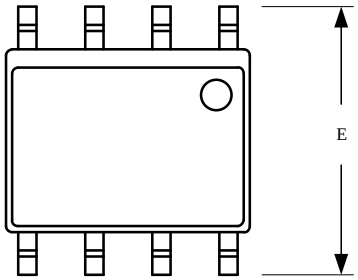
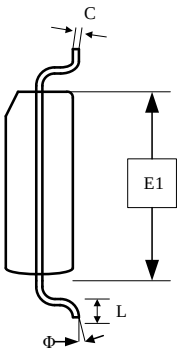


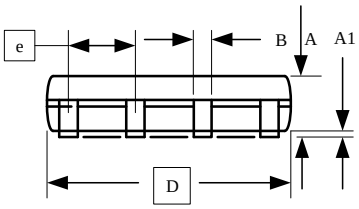
Figure 13. SCL: Serial Clock, SDA: Serial Data I/O

24LC01/24AA01

Package Information SOP



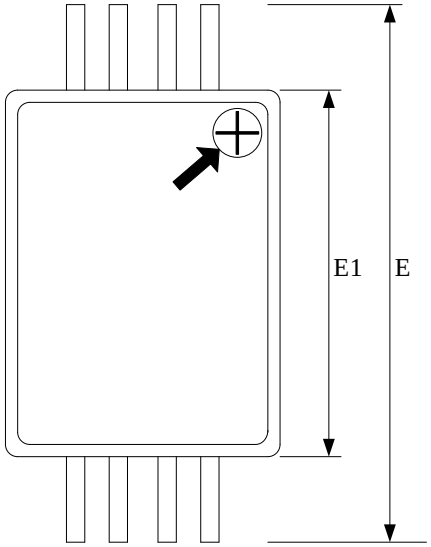




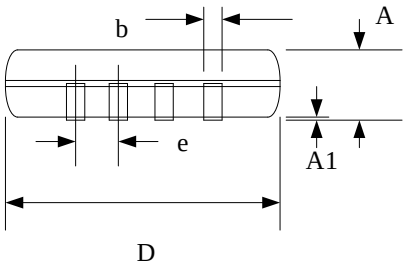
COMMON DIMENSIONS
(Unit of Measure=mm)

SYMBOL	MIN	NOM	MAX
A	1.35	-	1.75
A1	0.10	-	0.23
B	0.39	-	0.48
C	0.21	-	0.26
D	4.70	4.90	5.10
E1	3.70	3.90	4.10
E	5.80	6.00	6.20
e	1.27BSC		
L	0.50	-	0.80
Φ	0°	-	8°

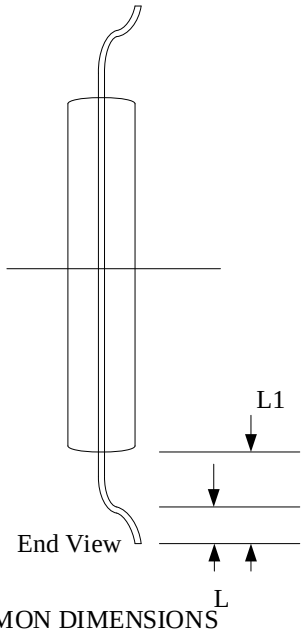
TSSOP



Top View



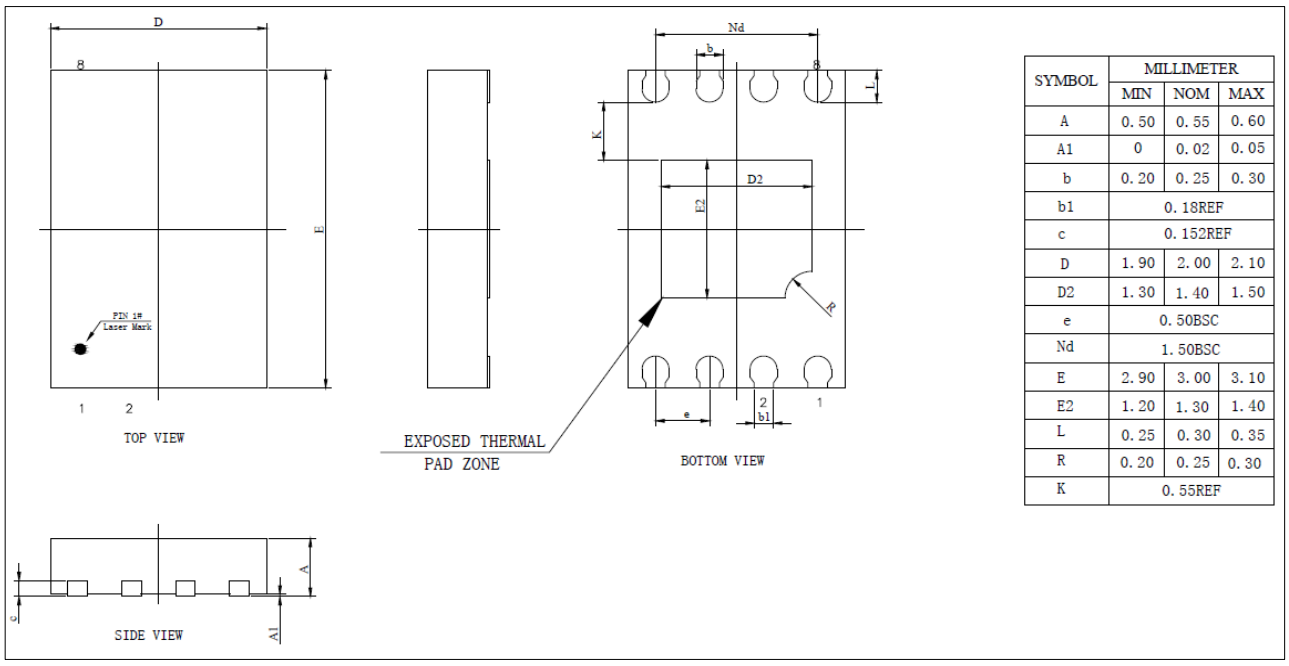
Side View



COMMON DIMENSIONS
Unit of Measure=mm

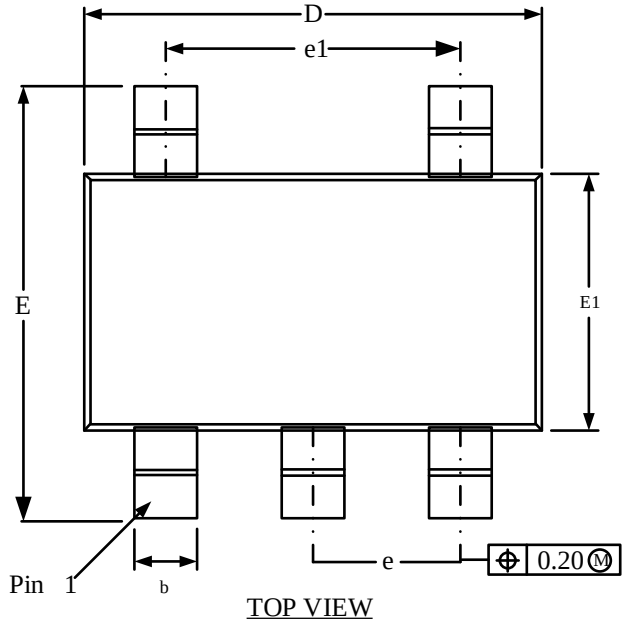
SYMBOL	MIN	NOM	MAX
D	2.90	3.00	3.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
A	-	-	1.20
A1	0.05	-	0.15
b	0.21	-	0.30
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		

UDFN

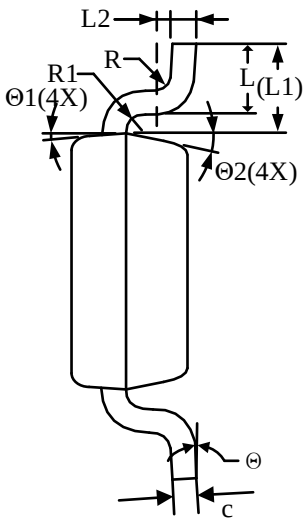


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1		0.18REF	
c		0.152REF	
D	1.90	2.00	2.10
D2	1.30	1.40	1.50
e		0.50BSC	
Nd		1.50BSC	
E	2.90	3.00	3.10
E2	1.20	1.30	1.40
L	0.25	0.30	0.35
R	0.20	0.25	0.30
K		0.55REF	

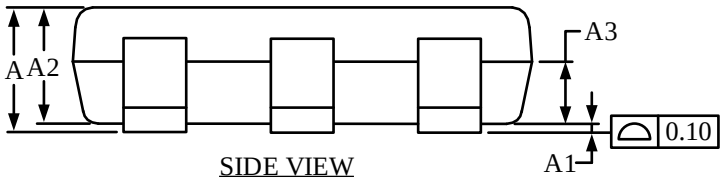
TSOT23-5



TOP VIEW



SIDE VIEW

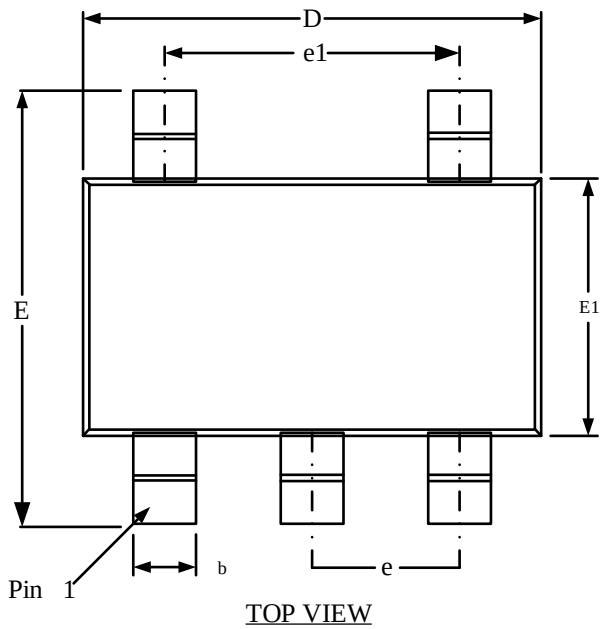


SIDE VIEW

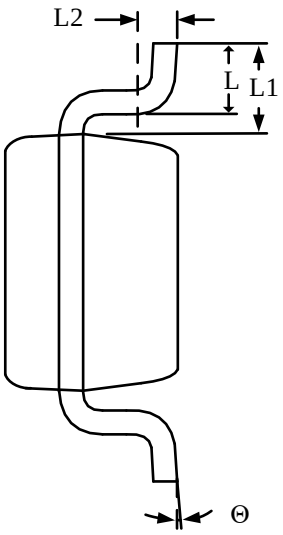
COMMON DIMENSIONS
(UNITS OF MEASURE = MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	-	-	0.90
A1	0.00	-	0.10
A2	0.65	0.75	0.85
A3	0.35	0.40	0.45
b	0.30	0.44	0.50
c	0.14	-	0.20
D	2.85	2.95	3.05
E	2.65	2.80	2.95
E1	1.60	1.65	1.70
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
L	0.30	0.45	0.60
L1	0.575REF		
L2	0.258BSC		
R	-	-	0.25
R1	-	-	0.25
Θ	0°	-	8°
Θ1	3°	5°	7°
Θ2	10°	12°	14°

SOT23-5



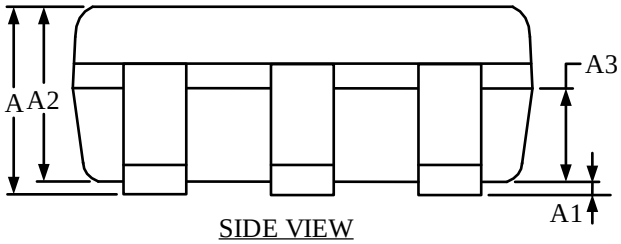
TOP VIEW



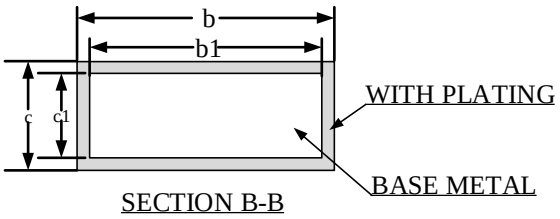
SIDE VIEW

COMMON DIMENSIONS
(UNITS OF MEASURE = MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	-	-	1.35
A1	0.04	-	0.15
A2	1.00	1.10	1.20
A3	0.55	0.65	0.75
b	0.38	-	0.48
b1	0.37	0.40	0.43
c	0.11	-	0.21
c1	0.10	0.13	0.16
D	2.72	2.92	3.12
E	2.60	2.80	3.00
E1	1.40	1.60	1.80
e	0.95BSC		
e1	1.90BSC		
L	0.30	-	0.60
L1	0.575REF		
L2	0.258BSC		
Θ	0°	-	8°



SIDE VIEW



SECTION B-B

Revision

.

history

重要通知与免责声明
深圳市钍地半导体有限公司将准确可靠地提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、WEB工具、安全信息和其他资源，但不保证任何缺陷，一切以实物测试为准，并且不作任何明示或暗示的保证，包括但不限于对适销性的暗示保证、对特定目的适用的暗示保证或不侵犯任何第三方知识产权的暗示保证。
这些资源旨在为使用钍地产品的熟练开发人员提供支持： (1) 为您的应用程序选择合适的产品；(2) 设计、验证和测试您的应用程序； (3) 确保您的应用程序符合适用的标准和任何其他安全、安保或其他要求； (4) 钍地和钍地标志是钍地半导体的注册商标。所有商标均为其各自所有者的财产； (5) 有关更改详情，请查阅任何修订文件中包含的修订历史记录。资源可能会在不通知的情况下更改。我公司将不对使用此产品及其使用而导致的专利或第三方知识产权的侵权负责。