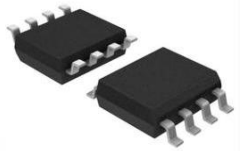
LM-LM61089B

Dual Programmable Thyristor Transient Voltage Suppressor

Features

- Dual programmable transient suppressor.
- Wide negative firing voltage range: V_{GKRM}=-167V max.
- Low dynamic switching voltage: V_{FRM} and $V_{GK(BO)}$.
- Low gate triggering current: I_{GT}=5mA max.
- Peak pulse current: I_{PP}=30A for 10/1000μs surge.
- Holding current: I_H=150mA min.



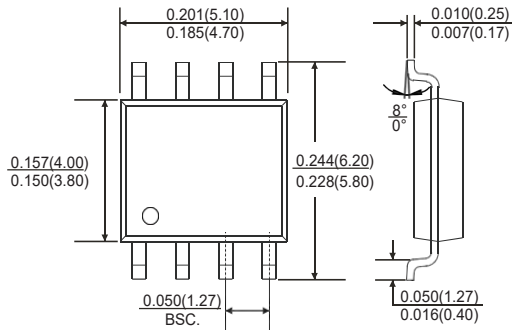
Applications

■ LM-LM61089B is designed to protect communication equipment such as SPC exchanger from being damaged by transient overvoltages at the second level.

Testing Standards

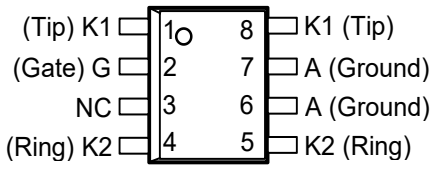
Type	Wave Sharp		V_{PP}/I_{PP}
ITU-T K.20,21 and K.45	Voltage	10/700μs	3000V
	Current	5/310μs	70A

SOP-8



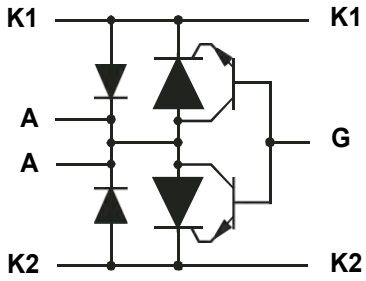
Dimensions in inches and (millimeter)

SOP Package Top View



NC - No internal connection
Terminal typical application names shown in parenthesis

Device Symbol



Terminals K1, K2 and A correspond to the alternative line designators of T, R and G or A, B and C. The negative protection voltage is controlled by the voltage, V_{GG},applied to the G terminal.

Description

This device is especially designed to protect subscriber line card interfaces (SLIC) against transient overvoltages. Positive overloads are clipped with 2 diodes. Negative surges are suppressed by 2 thyristors, their breakdown voltage being referenced to $-V_{BAT}$ through the gate. This component presents a very low gate triggering current (I_{GT}) in order to reduce the current consumption on printed circuit board during the firing phase. A particular attention has been given to the internal wire bonding. The “4-point” configuration ensures reliable protection, eliminating the overvoltage introduced by the parasitic inductances of the wiring (Ldi/dt), especially for very fast transients.

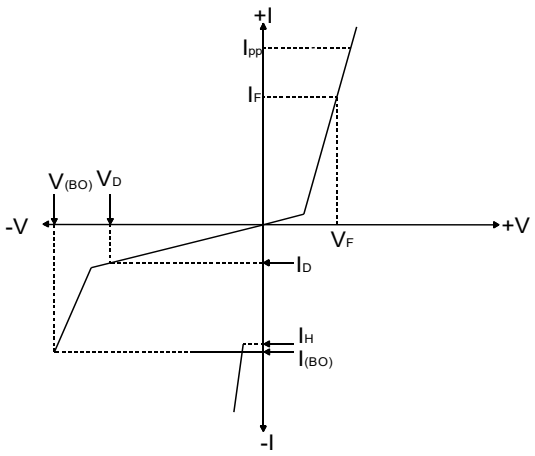
Absolute Maximum Ratings (T_A = 25 °C , RH=45%-75%,unless otherwise noted)

Parameter		Symbol	Value	Unit
Non-repetitive peak on-state pulse current				
10/1000μs	(Telcordia (Bellcore) GR-1089-CORE,Issue 2, February 1999, Section 4)	I_{TSP}	30	A
5/310μs	(ITU-T K.20/21& K.45/44 open-circuit voltage 10/700μs)		70	
1.2/50μs	(Telcordia (Bellcore) GR-1089-CORE, Issue 2, February 1999, Section 4)		120	
Non-repetitive peak pulse voltage(10/700μs)		V_{PP}	3000	V
Non repetitive surge peak on-state current (sinusoidal) 60Hz	0.1s	I_{TSM}	11	A
	1s		4.5	
	5s		2.4	
	300s		0.95	
	900s		0.93	
Maximum voltage LINE/GROUND		V_{DRM}	-170	V
Maximum voltage GATE/LINE		V_{GKRM}	-167	V
Storage temperature range		T_{STG}	-40 to +150	°C
Junction temperature		T_J	-40 to +150	°C
Operating free-air temperature range		T_A	-40 to +85	°C

Note：5/310μs means current wave, and its rise time is 5μs, fall time is 310μs.
10/700μs means voltage wave, and its rise time is 10μs, fall time is 700μs.

Voltage -Current Characteristic

Symbol	Parameters
I_D	Off-state current
I_H	Holding current
$V_{(BO)}$	Break-over voltage
V_F	Forward voltage
V_{FRM}	Peak forward recovery voltage
$V_{GK(BO)}$	Gate-cathode impulse break-over voltage
I_{GKS}	Gate reverse current
I_{GT}	Gate trigger current
V_{GT}	Gate-cathode trigger voltage
C_{KA}	Cathode-anode off-state capacitance



Electrical Characteristics (T_A = 25 °C , RH=45%-75%,unless otherwise noted)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
Parameters related to the diode						
V_F	Forward voltage	I_F=5A, t_W=200μs	-	-	3	V
V_{FRM}	Peak forward recovery voltage	2/10μs,I_F=100A,Rs=50Ω, di/dt=80A/μs	-	-	10	V
Parameters related to the protection thyristor						
I_D	Off-state current	V_{DRM}=-170V, V_{GK}=0V	-	-	-5	μA
$V_{(BO)}$	Break-over voltage	2/10μs, I_{TM}=-100A,Rs=50Ω, di/dt=-80A/μs, V_{GG}=-100V	-	-	-112	V
I_H	Holding current	I_T=-1A, di/dt=1A/ms, V_{GG}=-100V	-150	-	-	mA
I_{GKS}	Gate reverse current	V_{GG}=V_{GK}=-167V, V_{KA}=0,T_J=25°C	-	-	-5	μA
I_{GT}	Gate trigger current	I_T=-3A, $t_{P(g)}$≥20μs, V_{GG}=-48V	-	-	5	mA
V_{GT}	Gate trigger voltage	I_T=-3A, $t_{P(g)}$≥20μs, V_{GG}=-48V	-	-	2.5	V
C_{AK}	Anode-cathode off-state capacitance	f=1MHz,V_d=1V,I_G=0A, V_D=-3V	-	-	100	pF

Note：5/310μs means current wave, and its rise time is 5μs, fall time is 310μs.
10/700μs means voltage wave, and its rise time is 10μs, fall time is 700μs.

Applications Information

☐ Operation of Ringing SLICs using Multiple Negative Voltage Supply Rails

Figure 1 shows a typical powering arrangement for a multi-supply rail SLIC. V_{BATL} is a lower (smaller) voltage supply than V_{BATH}. With supply switch S1 in the position shown, the line driver amplifiers are powered between 0 V and V_{BATL}. This mode minimizes the power consumption for short loop transmission. For long loops and to generate ringing, the driver voltage is increased by operating S1 to connect V_{BATH}. These conditions are shown in Figure 2.

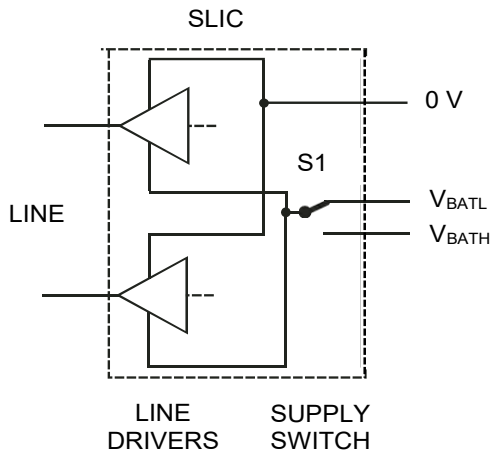


Figure 1. SLIC with Voltage Supply Switching

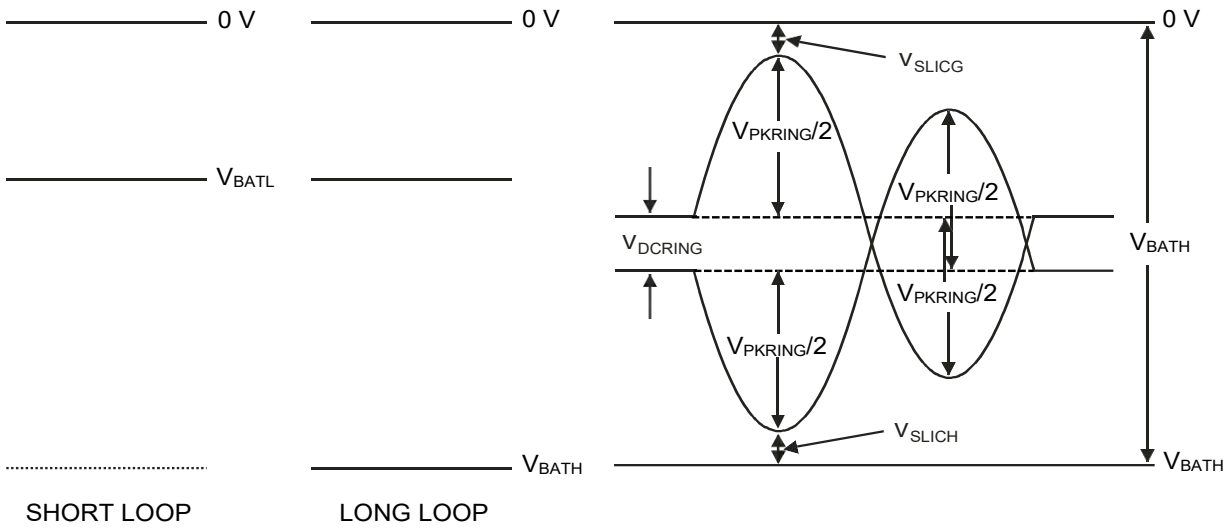


Figure 2. Driver Supply Voltage Levels

Conventional ringing is typically unbalanced ground or battery backed. To minimize the supply voltage required, most multi-rail SLICs use balanced ringing as shown in Figure 2. The ringing has d.c., V_{DCRING}, and a.c., V_{PKRING}, components. A 70 V r.m.s. a.c. sinusoidal ring signal has a peak value, V_{PKRING}, of 99 V. If the d.c. component was 20 V, then the total voltage swing needed would be 99 + 20 = 119 V. There are internal losses in the SLIC from ground, V_{SLICG}, and the negative supply, V_{SLICH}. The sum of these two losses generally amounts to a total of 10 V. This makes a total, V_{BATH}, supply rail value of 119 + 10 = 129 V.

In some cases a trapezoidal a.c. ring signal is used. This would have a peak to r.m.s ratio (crest factor) of about 1.25, increasing the r.m.s. a.c. ring level by 13 %. The d.c. ring voltage may be lowered for short loop applications.

☐ SLIC Parameter Values

The table below shows some details of HV SLICs using multiple negative supply rails.

Manufacturer	INFINEON		LEGERITY						Unit
SLIC Series	SLIC-P		ISLIC						
SLIC #	PEB 4266		79R241		79R101		79R100		
Data Sheet Issue	14/02/2001		-/08/2000		-/07/2000		-/07/2000		
Short Circuit Current	110		150		150		150		mA
V_{BATH} max.	-155		-104		-104		-104		V
V_{BATL} max.	-150		-104		V_{BATH}		V_{BATH}		V
AC Ringing for:	85		45 [1]		50 [1]		55 [1]		V rms
Crest Factor	1.4		1.4		1.4		1.25		
V_{BATH}	-70		-90		-99		-99		V
V_{BATR}	-150		-36		-24		-24		V
R or T Power Max. < 10 ms	10								W
R or T Overshoot < 10 ms	TBD	TBD	-5	5	-10	5	-10	5	V
R or T Overshoot < 1 ms	-10	+10							V
R or T Overshoot < 1 µs	-10	+30	-10	10	-15	8	-15	8	V
R or T Overshoot < 250 ns			-15	15	-20	12	-20	12	V
Line Feed Resistance	20 + 30		50		50		50		Ω

Note：1. Assumes -20 V battery voltage during ringing.

From the table, the maximum supply voltage, V_{BATH}, is -155 V. In terms of minimum voltage overshoot limits, -10 V and +8 V are needed for 1 µs and -15 V, +12 V are needed for 250 ns. To maintain these voltage limits over the temperature range, 25 ℃ values of -12 V, +10 V are needed for 250 ns.

It is important to define the protector overshoot under the actual circuit current conditions. For example, if the series line feed resistor was 40 Ω, R1 in Figure 9, and Telcordia GR-1089-CORE 2/10 and 10/1000 first-level impulses were applied, the peak protector currents would be 56 A and 20 A. At the second-level, the 2/10 impulse current would be 100 A. Therefore, the protector voltage overshoot should be guaranteed to not exceed the SLIC voltage ratings at 100 A, 2/10 and 20 A, 10/1000. In practice, as the 2/10 waveshape has the highest current (100 A) and fastest di/dt (80 A/µs) the overshoot level testing can restricted to the be 2/10 waveshape.

Using the table values for maximum battery voltage and minimum overshoot gives a protection device requirement of -170 V and +12 V from the output to ground. There needs to be temperature guard banding for the change in protector characteristics with temperature. To cover down to -40 ℃ , the 25℃ protector minimum values become -185 V (V_{DRM}) on the cathode and -182 V (V_{GKS}) on the gate.

☐Gated Protectors

This section covers four topics. First, it is explained why gated protectors are needed. Second, the voltage limiting action of the protector is described. Third, how the withstand voltages of the LM-LM61089B junctions are set. Fourth, an example application circuit is described.

Purpose of Gated Protectors

Fixed voltage thyristor overvoltage protectors have been used since the early 1980s to protect monolithic SLICs (Subscriber Line Interface Circuits) against overvoltages on the telephone line caused by lightning, a.c. power contact and induction. As the SLIC was usually powered from a fixed voltage negative supply rail, the limiting voltage of the protector

could also be a fixed value.

SLICs have become more sophisticated. To minimize power consumption, some designs automatically adjust the drivere supply voltage to a value that is just sufficient to drive the required line current. For short lines, the supply voltage would b set low, but for long lines, a higher supply voltage would be generated to drive sufficient line current. The optimum protection for this type of SLIC would be given by a protection voltage which tracks the SLIC supply voltage. This can be achieved by connecting the protection thyristor gate to the SLIC V_{BATH} supply,

Figure 3. This gated (programmable) protection arrangement minimizes the voltage stress on the SLIC, no matter what value of supply voltage.

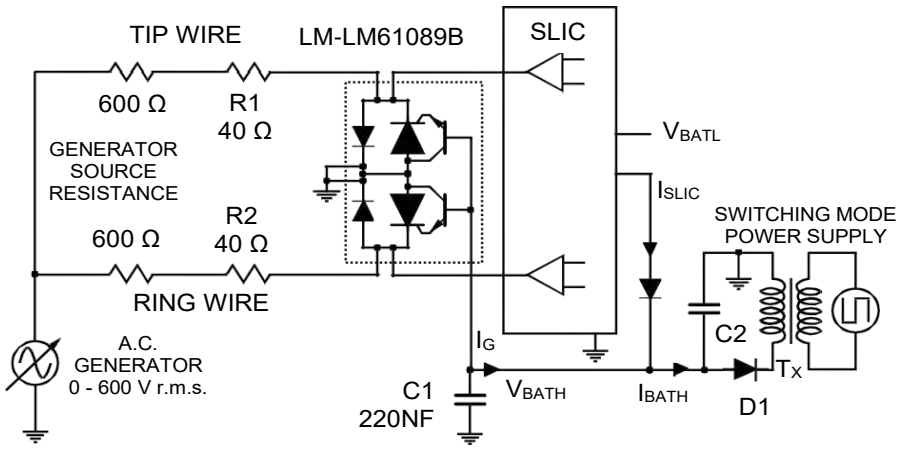


Figure 3. LM-LM61089B Buffered Gate Protector

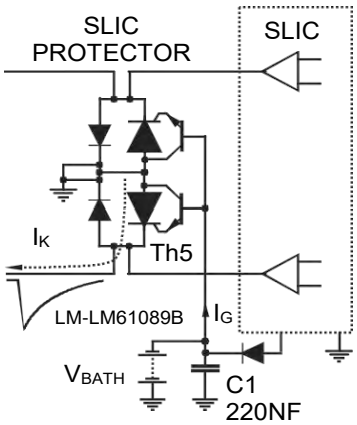


Figure 4. Negative Overvoltage Condition

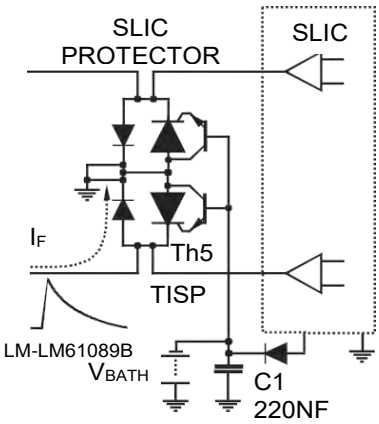


Figure 5. Positive Overvoltage Condition

Operation of Gated Protectors

Figure 4 and Figure 5 show how the LM-LM61089B limits negative and positive overvoltages. Positive overvoltages (Figure 5) are clipped by the antiparallel diode of Th5 and the resulting current is diverted to ground. Negative overvoltages (Figure 4) are initially clipped close to the SLIC negative supply rail value (V_{BATH}). If sufficient current is available from the overvoltage, then Th5 will switch into a low voltage on-state condition. As the overvoltage subsides the high holding current of Th5 prevents d.c. latchup. The protection voltage will be the sum of the gate supply (V_{BATH}) and the peak gate-cathode voltage ($V_{GK(BO)}$). The protection voltage will be increased if there is a long connection between the gate decoupling capacitor, C1, and the gate terminal. During the initial rise of a fast impulse, the gate current (I_G) is the same as

the cathode current (I_K). Rates of 80 A/µs can cause inductive voltages of 0.8 V in 2.5 cm of printed wiring track. To minimize this inductive voltage increase of protection voltage, the length of the capacitor to gate terminal tracking should be minimized. Inductive voltages in the protector cathode wiring will also increase the protection voltage. These voltages can be minimized by routing the SLIC connection through the protector as shown in Figure 3.

Figure 6, which has a 10 A/µs rate of impulse current rise, shows a positive gate charge (Q_{GS}) of about 0.1 µC. With the 0.1 µF gate decoupling capacitor used, the increase in gate supply is about 1 V (= Q_{GS}/C1). This change is just visible on the -72 V gate voltage, V_{BATH}. But, the voltage increase does not directly add to the protection voltage as the supply voltage change reaches a maximum at 0.4 µs, when the gate current reverses polarity, and the protection voltage peaks earlier at 0.3 µs. In Figure 6, the peak clamping voltage ($V_{(BO)}$) is -77.5 V, an increase of 5.5 V on the nominal gate supply voltage. This 5.5 V increase is the sum of the supply rail increase at that time, (0.5 V), and the protection circuit's cathode diode to supply rail breakover voltage (5 V). In practice, use of the recommended 220 nF gate decoupling capacitor would give a supply rail increase of about 0.3 V and a $V_{(BO)}$ value of about -77.3 V.

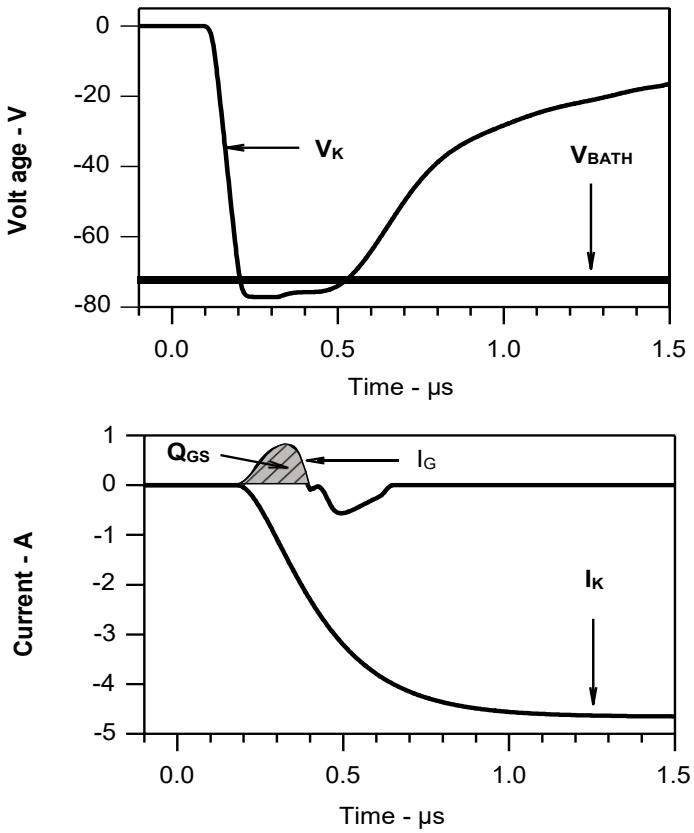


Figure 6. Protector Fast Impulse Clamping and Switching Waveforms

Voltage Stress Levels on the LM-LM61089B

Figure 7 shows the protector electrodes. The package terminal designated gate, G, is the transistor base, B, electrode connection and so is marked as B (G). The following junctions are subject to voltage stress: Transistor EB and CB, SCR AK (off state) and the antiparallel diode (reverse blocking). This clause covers the necessary testing to ensure the junctions are good.

Testing transistor CB and EB: The maximum voltage stress level for the LM-LM61089B is V_{BATH} with the addition of the short

term antiparallel diode voltage overshoot, V_{FRM}. The current flowing out of the G terminal is measured at V_{BATH} plus V_{FRM}. The SCR K terminal is shorted to the common (0 V) for this test (see Figure 7). The measured current, I_{GKS}, is the sum of the junction currents I_{CB} and I_{EB}.

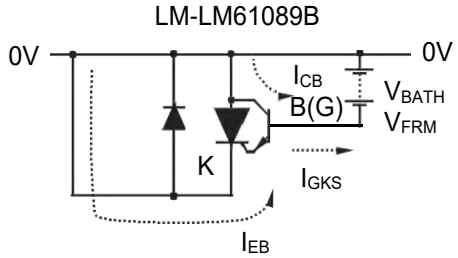
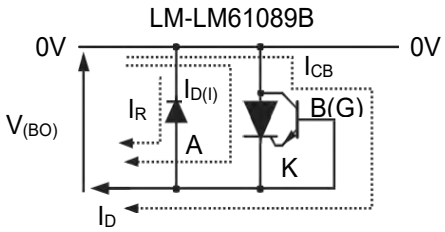


Figure 7. Transistor CB and EB Verification

Testing transistor CB, SCR AK off state and diode reverse blocking: The highest AK voltage occurs during the overshoot period of the protector. To make sure that the SCR and diode blocking junctions do not break down during this period, a d.c. test for off-state current, I_D, can be applied at the overshoot voltage value. To avoid transistor CB current amplification by the transistor gain, the transistor base-emitter is shorted during this test (see Figure 8).



$I_{D(I)}$ is the internal SCR value of I_D

Figure 8. Off-State Current Verification

Summary: Two tests are needed to verify the protector junctions. Maximum current values for I_{GKS} and I_D are required at the specified applied voltage conditions.

Application Circuit

Figure 9 shows a typical LM-LM61089B SLIC card protection circuit. The incoming line conductors, Ring (R) and Tip (T), connect to the relay matrix via the series overcurrent protection. Fusible resistors, fuses and positive temperature coefficient (PTC) resistors can be used for overcurrent protection. Resistors will reduce the prospective current from the surge generator for both the LM-LM61089B and the ring/test protector.

Relay contacts 3a and 3b connect the line conductors to the SLIC via the LM-LM61089B protector. The protector gate reference voltage comes from the SLIC negative supply (V_{BATH}). A 220 nF gate capacitor sources the high gate current pulses caused by fast rising impulses.

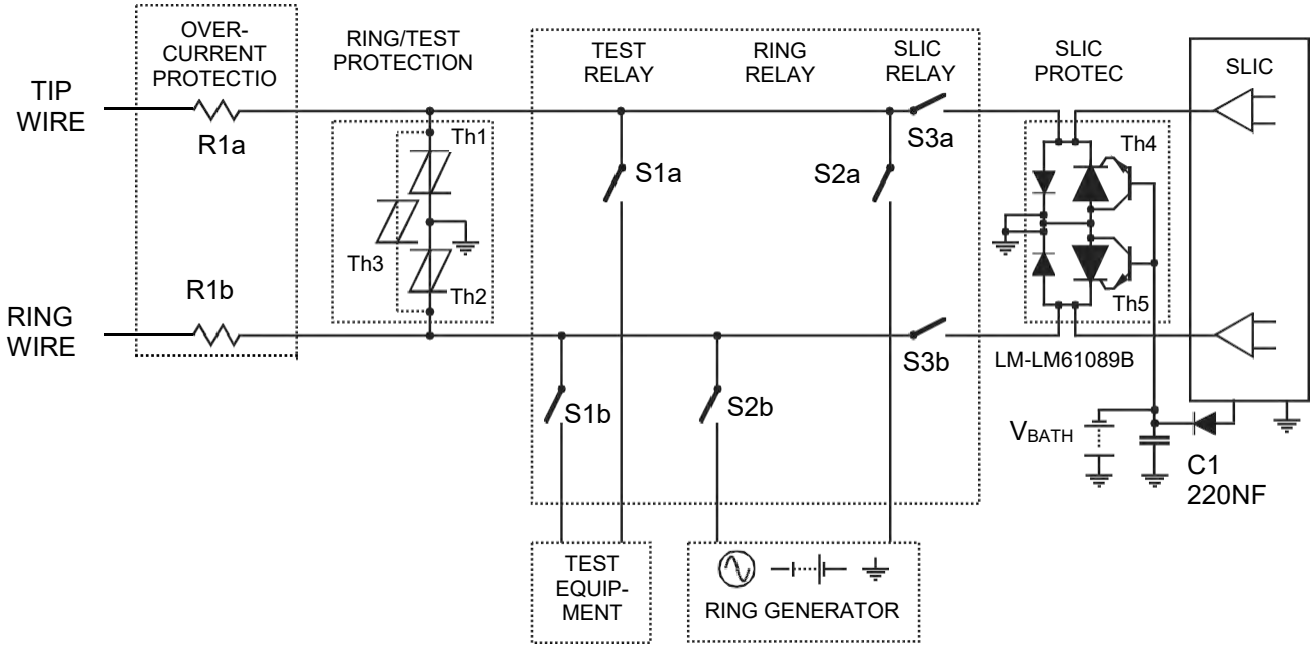
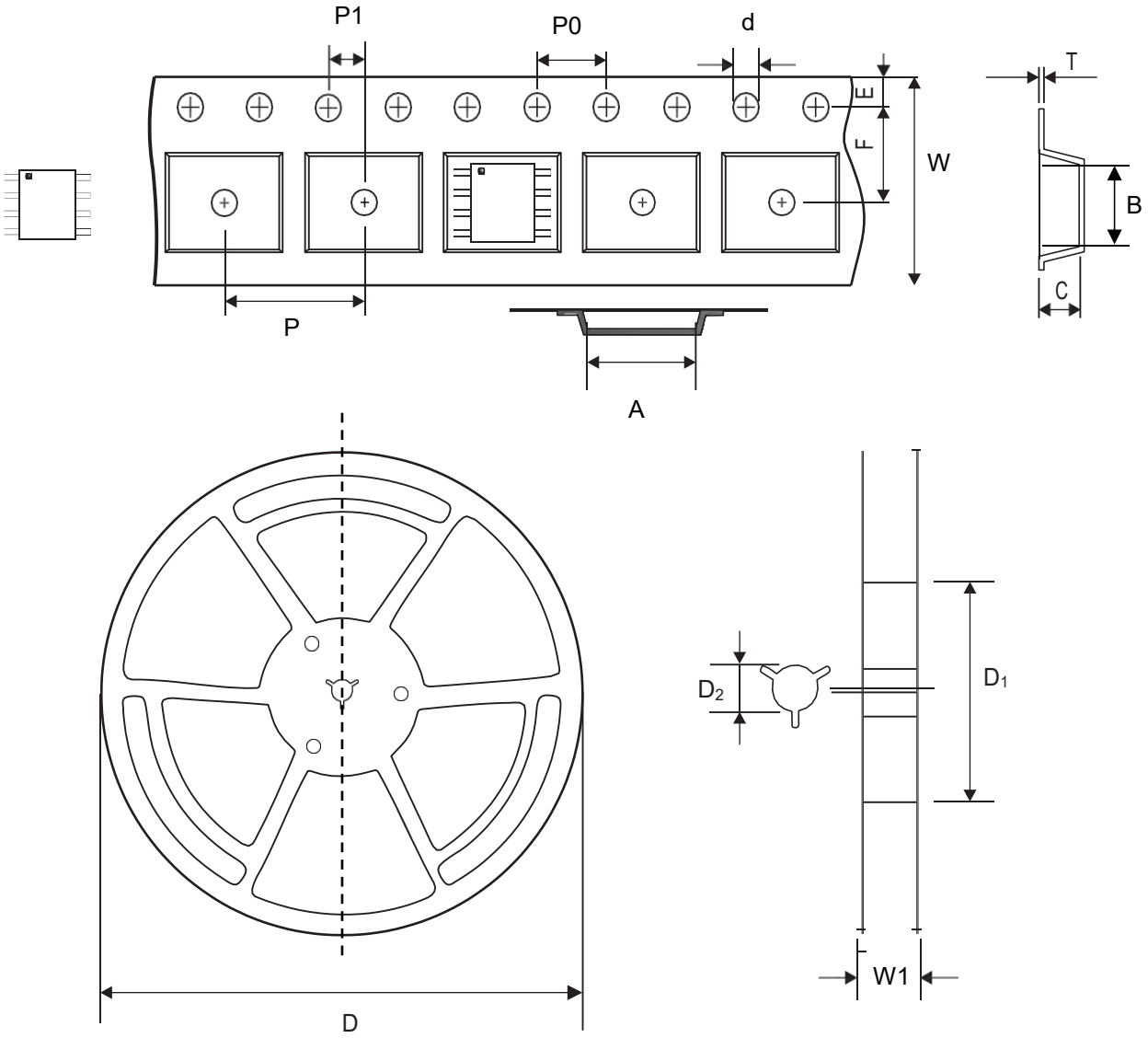


Figure 9. Typical Application Circuit

Reel Taping Specification

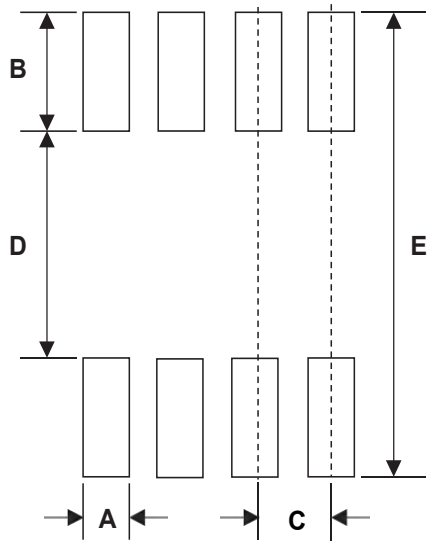


	SYMBOL	A	B	C	d	D	D1	D2
SOP-8	(mm)	6.40 ± 0.10	5.20 ± 0.10	2.10 ± 0.10	1.50 + 0.10 - 0.00	330.00 ± 1.00	100.00 ± 0.50	13.00 ± 1.00
	(inch)	0.252 ± 0.004	0.205 ± 0.004	0.083 ± 0.004	0.059 + 0.004 - 0.000	12.992 ± 0.039	3.937 ± 0.020	0.512 ± 0.039

	SYMBOL	E	F	P	P0	P1	T	W	W1
SOP-8	(mm)	1.75 ± 0.10	5.50 ± 0.05	8.00 ± 0.10	4.00 ± 0.10	2.00 ± 0.05	0.25 ± 0.02	12.00 + 0.30 - 0.10	17.60 + 1.00 - 0.00
	(inch)	0.069 ± 0.004	0.217 ± 0.002	0.315 ± 0.004	0.157 ± 0.004	0.079 ± 0.002	0.010± 0.001	0.472 + 0.012 - 0.004	0.693 + 0.039 - 0.000

Suggested PAD Layout

SIZE	SOP-8	
	(mm)	(inch)
A	0.60	0.024
B	1.52	0.060
C	1.27	0.050
D	4.00	0.157
E	7.00	0.276



Marking Code

Part Number	Marking Code
LM-LM61089B	61089B
61089B= Product type marking code XXXXX = Date Code Dot denotes Pin1	

Ordering Information

Part Number	Package	Weight	Base qty	Reel Size	Delivery mode
		grams(approx.)	(pcs)	(inch)	
LM-LM61089B	SOP-8	0.077	4000	13	Tape and reel

NOTICE

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