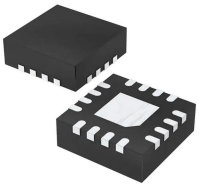
D4202

Single LNB-Complete Bias And Power Managemenr Solution

General Description



QFN16(3*3)

The D4202 is a single chip power management and control solution for LNB's. The highly integrated solution provides all the required FET and mixer bias, control detection and decoding, local oscillator switching and a stable power supply for the IF amplifier and additional support functions. Packaged in a small 16 pin package the D4202 only requires 3 external components providing a very small compact solution. Being at the heart of the LNB monitoring the control, power management and environmental conditions, the D4202 is able to provide reliable solution eliminating effects such as false switching and over loading.

The D4202 provides a highly integrated single chip power management solution to meet the demands of single output and mono-block satellite receiver Low Noise Block's (LNB's). The D4202 includes bias circuits to drive up to three GaAs or HEMT FET's and an additional active mixer. To minimize the pin count and external components the D4202 Vcc pin is combined with the IC's control pin for both voltage and tone signals. A reliable voltage detector allows the device to enable the required polarization channel by selecting either one of two FETs using 0V gate switching methodology. The third FET is permanently active to provide bias for an extra LNA gain stage. Specific to Universal type LNB's a 22kHz tone is used to switch between low and high band oscillators. The internal tone detection circuitry has been designed so that no external filtering is required whist still providing a tone detector which rejects all unwanted signals including DiSEqC tone bursts. The D4202 has integrated logic control and has been optimized to drive bipolar type oscillators directly. To provide the complete LNB power management solution the IC is self powering and provides a temperature compensated output voltage to power the remaining parts of the LNB such as the Zetex IF amplifiers.To provide system flexibility the drain current of the FETs is user selectable over the range of 0-15mA and the mixer current can be set from 0-10mA. This is achieved with the addition of a single reference resistor for both the FET stages and the mixer.

These devices are unconditionally stable over the full working temperature with the FETs in place, subject to the inclusion of the recommended gate and drain capacitors. These

ensure RF stability and minimal injected noise.It is possible to use less than the full complement of FET and mixer bias controls, unused drain and gate connections can be left open circuit without affecting operation of the remaining bias control.

The D4202 has over temperature and over current protection, if the IC temperature or input current exceeds safe limits the LNB will shut down and restart when operating conditions return to normal. To protect the external FETs the bias circuits have been designed to ensure that under any condition including power up/down transients, the gate drive from the bias circuits cannot exceed the range -3.0 to 1V. Further more if the negative rail experiences a fault condition, such as overload or short circuit, the drain supply to the FETs will limit, avoiding excessive current flow.

Features

- Single chip LNB bias, control and power management
- Integrated regulated supply for LNB
- Zero volt gate FET switching topology
- Voltage detection for polarization switching
- 22kHz tone detector with unwanted signal rejection for band switching
- No external control signal filtering required
- Programmable mixer and FET bias
- Temperature compensated protected FET bias
- Full power management protection

Package Information

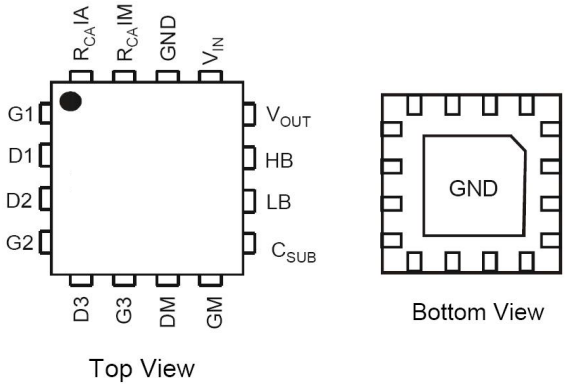
Part NO.	Package Description	Package Marking	Package Option
D4202	QFN16(3*3)	CHMC D4202 SXXXX ○	3000/Reel

CHMC:Trademark D4202:Part NO. SXXXX:Lot NO.

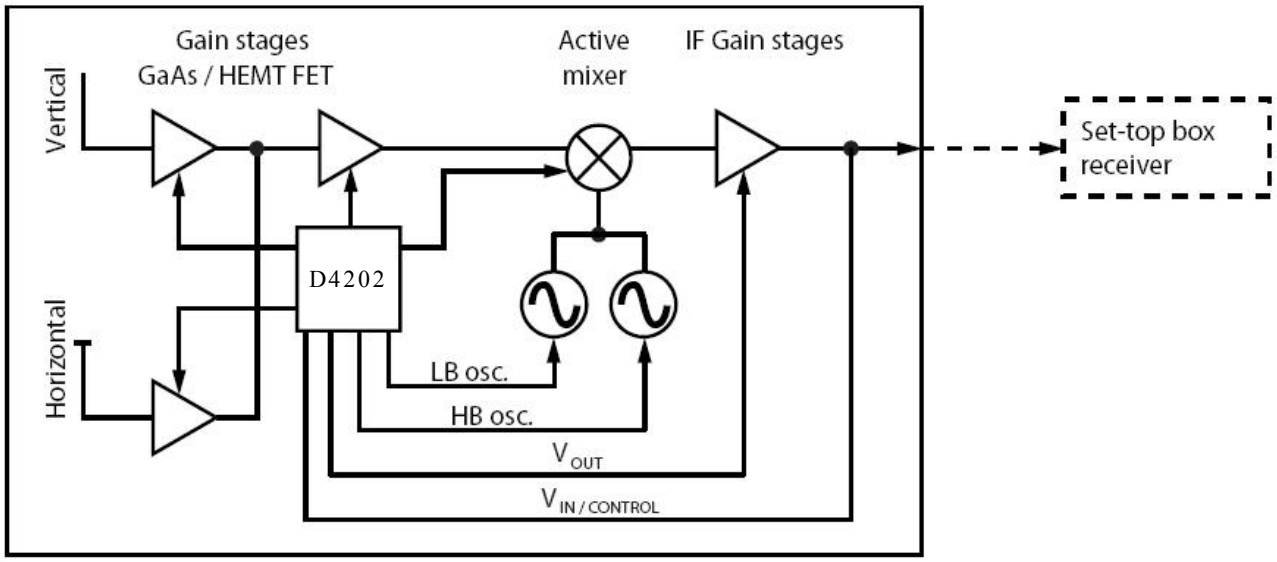
Applications

- Single and Single Universal LNBs
- Mono-block LNB's
- C-band LNB's

Pin Configuration



Block Diagram



Absolute Maximum Ratings

Characteristic		Limit	Unit
Supply voltage		-0.6～+25	V
Supply current		120	mA
Power dissipation	QFN16(3*3)	2	W
Operating temperature range		-40～+85	℃
Operating junction temperature range		-40～+125	℃
Storage temperature range		-40～+125	℃

Electrical Characteristics

All measurements at T_A= 25°C ,V_{IN}=13V,$R_{CAL}A$= $R_{CAL}M$=22k (setting Ids to 10mA) unless otherwise specified.

Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
Supply voltage operating range	QFN16(3*3)	8		22	V
Supply current					
No load supply current	Id1=Id2=Id3=Idm=I_{OUT}=0mA		2	3	mA
Max. total load current	QFN16(3*3)			80	mA
Max. bias load current	Id1 or Id2+Id3+Idm			40	mA
Max.osc load current	LB or HB			50	mA
Max.V_{OUT} load current	QFN16(3*3)			80	mA
V_{OUT}	V_{IN}=10.5V to 21V,I_{OUT}=30mA	4.75	5	5.25	V
Delta V_{OUT} vs V_{IN}	V_{LL}=10.5 to 21V		0.1		%/V
Delta V_{OUT} vs T_J	Tamb=-40 to +85°C		50		ppm
Substrate voltage	(Internally generated),I_{SUB}=0mA	-3.0	-2.5	-2.0	V
	I_{SUB}=-20μA			-2.0	V
Vpol threshold	Applied via V_{IN} pin, Tamb=-40 to +85°C	14.1	14.7	15.4	V
Pol switching speed	V_{IN}(low)=13V, V_{IN}(high)=18V			1	ms

Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
Output noise					
Drain voltage	Cgate-gnd=4.7nF, Cgate-gnd=10nF			0.02	Vpk-pk
Gate voltage	Cgate-gnd=4.7nF, Cgate-gnd=10nF			0.005	Vpk-pk
Tone detector					
T detect threshold	22kHz sq. wave, T_{rise}=T_{fall}=7.5mS	100	170	300	mV
Rejection freq.	22kHz sq. wave, 1V pk-pk , T_{rise}=T_{fall}=7.5mS	1.0	7.5		kHz
LO output stage					
LB V_{OUT} low	I_L=0,V_{IN}(tone)=350mV pk-pk 22kHz sq. wave, T_{rise}=T_{fall}=7.5mS	-0.01	0	0.01	V
LB V_{OUT} high	I_L=50mA,V_{IN}(tone)=0	4.5	5.0	5.25	V
HB V_{OUT} low	I_L=0,V_{IN}(tone)=0	-0.01	0	0.01	V
HB V_{OUT} high	I_L=50mA,V_{IN}(tone)=350mV pk-pk.22kHz sq. wave, T_{rise}=T_{fall}=7.5mS	4.5	5.0	5.25	V
Gate characteristics					
G1 output					
Voltage off	Id1=0, V_{IN}=14V,Ig1=0	-0.05	0	0.05	V
Voltage low	Id1≤12mA, V_{IN}=15.5V,Ig1=-10μA	-3.0	-2.5	-2.0	V
Voltage high	Id1≥8mA, V_{IN}=15.5V, Ig1=0	0.4	0.65	1.0	V
G2 output					
Voltage off	Id2=0, V_{IN}=15.5V,Ig2=0	-0.05	0	0.05	V
Voltage low	Id2≤12mA, V_{IN}=14V,Ig2=-10μA	-3.0	-2.5	-2.0	V
Voltage high	Id2≥8mA, V_{IN}=14V, Ig2=0	0.4	0.65	1.0	V

Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
G3 and Gm outputs					
Voltage low	Id3/m≤12mA, Ig3/m=-10μA	-3.0	-2.5	-2.0	V
Voltage high	Id3/m≥8mA, Ig3/m=0	0.4	0.5	1.0	V
Drain characteristics					
D1 output					
Voltage high	Id1=10mA, V_{IN}=15.5V	1.8	2.0	2.2	V
Leakage current	Vd1=0.5, V_{IN}=14V			10	μA
D2 output					
Voltage high	Id2=10mA, V_{IN}=14V	1.8	2.0	2.2	V
Leakage current	Vd2=0.5, V_{IN}=15.5V			10	μA
D3 output					
Voltage high	Id3=10mA, V_{IN}=15.5V	1.8	2.0	2.2	V
Dm output					
Voltage high	Idm=10mA	0.5	0.6	0.7	V
D1,2,3 and m					
Delta V_D vs V_{IN}	V_{IN}=10.5 to 21V	-0.2	0.05	0.2	%/V
Delta V_D vs T_J	Tamb=-40 to +85°C		50		ppm
FET current range	Id1,Id2 and Id3	0		15	mA
Mixer current range	Idm	0		10	mA
Drain current	Id1,Id2,Id3 and Idm, RcalA and RcalM=22k	8	10	12	mA
Delta Id vs V_{IN}	V_{IN}=10.5 to 21V	-0.2	0.05	0.2	%/V
Delta Id vs Tamb	Tamb=-40 to +85°C		0.05		%/°C

* These parameters are related to Rcal values.

* The total combined load currents should not exceed the stated maximum load current.

* The D4202 rejects DiSEqC data streams.

* To ensure RF stability and to guard against ESD damage, a capacitor should be connected between the pins Vin and Gnd. See applications notes.

* To ensure RF stability, a capacitor should be connected between the pins V_{OUT} and Gnd.

Application Summary

Figure 1 is a partial application circuit for the D4202 showing all external components required for appropriate biasing. The bias circuits are unconditionally stable over the full temperature range with the associated FETs and gate and drain capacitors in circuit. Capacitors C1 and C2 ensure that residual power supply and substrate generator noise is not allowed to affect other external circuits which may be sensitive to RF interference. They also serve to suppress any potential RF feed through between stages via the D4202 device. These capacitors are required for all stages used. Values of 10nF and 4.7nF respectively are recommended however this is design dependent and any value between 1nF and 100nF could be used. The capacitor CSUB is an integral part of the D4202's negative supply generator. The negative bias voltage is generated on-chip using an internal oscillator. The required value of capacitor CSUB is 47nF. This generator produces a low current supply of approximately -2.5V.Although this generator is intended purely to bias the external FETs, it can be used to power other external low current circuits via the CSUB pin. Resistor RcalA sets the drain current at which all external amplifier FETs are operated and RcalM sets the mixer bias current. If any bias control circuit is not required, its related drain and gate connections may be left open circuit without affecting the operation of the remaining bias circuits. The D4202 device have been designed to protect the external FETs from adverse operating conditions. With a JFET connected to any bias circuit, the gate output voltage of the bias circuit can not exceed the range -3.0V to 1V under any conditions, including power up and power down transients. Should the negative bias generator be shorted or overloaded so that the drain current of the external FETs can no longer be controlled, the drain supply to FETs is shut down to avoid damage to the FETs by excessive drain current. The D4202 incorporates over-temperature and current protection so if the receiver or installation develops a fault causing excessive power dissipation, the LNB will shut down and restart once operating conditions are back to normal.To ensure RF stability and guard against down-feed cable induced ESD damage, a capacitor CV_{IN} should be connected between the pins V_{IN} and Gnd. A capacitor of value 100nF is expected to perform both these functions. This capacitor needs to maintain its value over the operating range so Y5V types are not recommended. If an alternate form of ESD protection is used (for example a power zener), then a smaller value capacitor can be used (22nF minimum is recommended). To ensure RF stability, a capacitor CV_{OUT} should also be connected between the pins V_{OUT} and Gnd. Values in the range 22nF to 100nF should be adequate to perform this function.

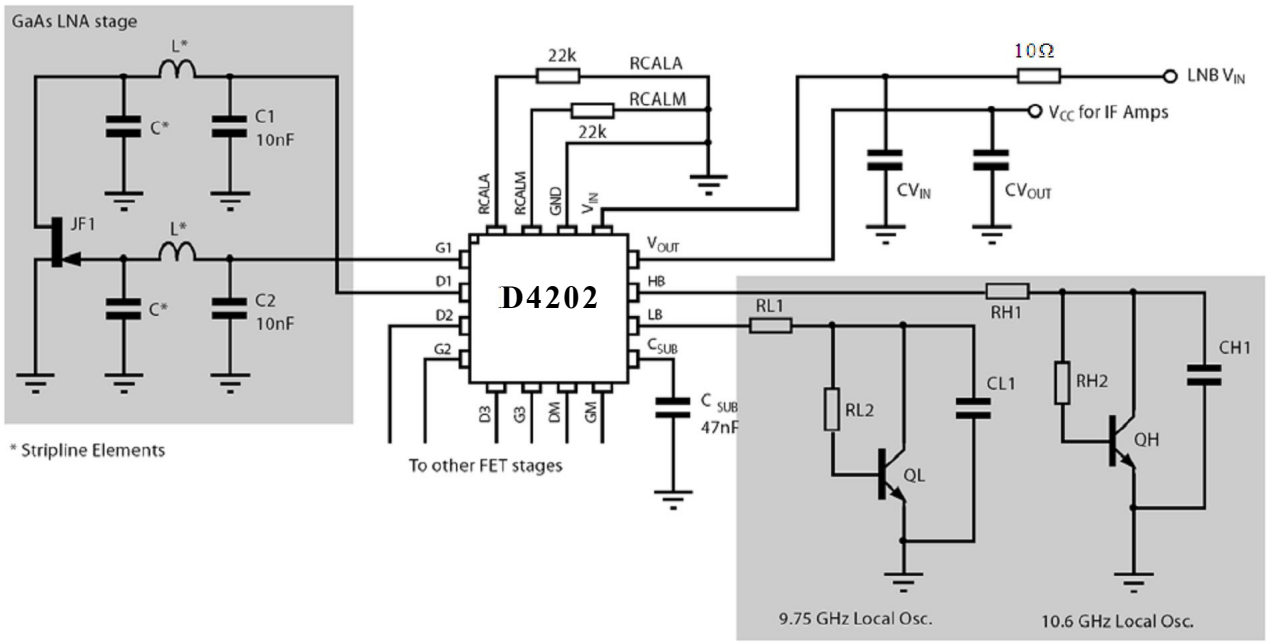


Figure.1 Application circuit for the D4202

Figure 2 shows the main elements of a Single universal LNB. The D4202 is compliant with virtually all markets including the fleet of Astra satellites. A single chip solution provides all the FET and mixer bias, control signal detect for polarization and band selection and all the necessary power management functions required within a Single Universal LNB. Polarization and band switching on the D4202 uses the standard 13V-17V and 22kHz as defined by Astra. The exception is that the devices voltage detector has a much tighter tolerance than required to increase field reliability.

The single V_{IN} pin is used internally for three functions, LNB and IC power supply, voltage detection and tone detection. The IC's is self powering via an internal regulator which utilizes the 13V-17V control voltage from the satellite receiver. This regulated voltage is used both to supply the internal requirements of the IC and is also made available on the VOUT pin to provide a power supply for the remaining elements of the LNB such as IF amplifiers. The voltage of the 13V-17V feed from the receiver is sensed by a tight tolerance detector with integrated filtering which removes all common unwanted signals and interference. The output of this detector is used to select one of two bias circuits, enabling either FET 1 or FET 2. The internal tone detector allows the device to detect the 22kHz tone

which is superimposed on the LNB power line (13V-17V signal). The tone detector rejects all unwanted signals including transients from other parts of the LNB system without the use of any external components. The tone detector controls a drive circuit which powers one of two local oscillators (normally used to switch between low and high band in Universal LNB applications). The functional table below shows the operation of the FET and Mixer bias, oscillator outputs and the LNB power supply.

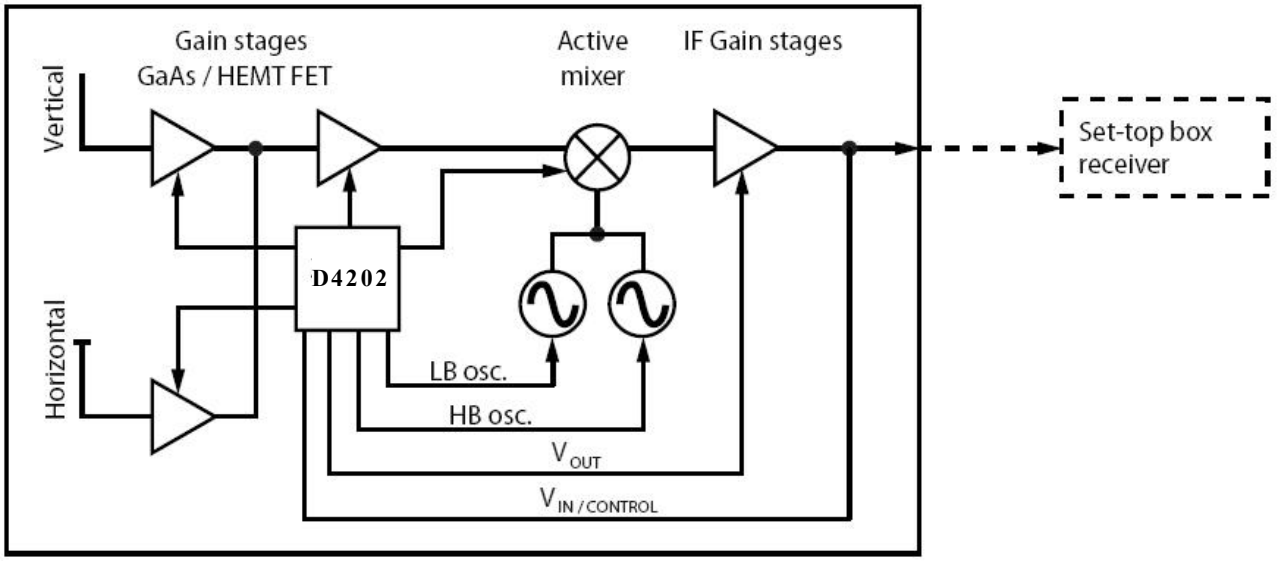
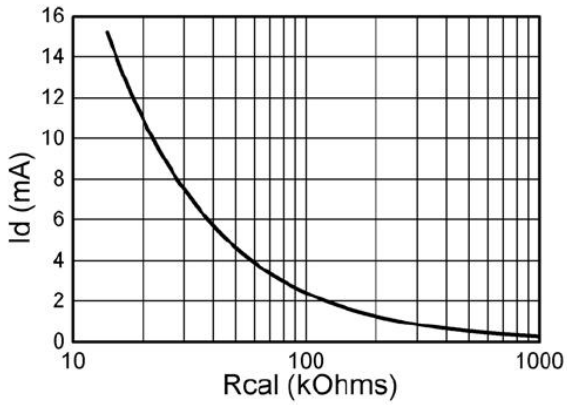


Figure 2 Single Universal LNB System Diagram

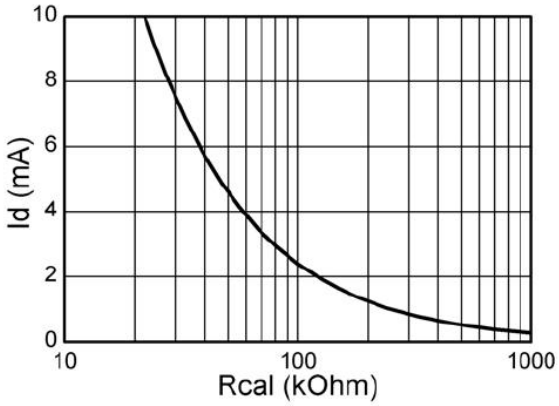
Functional Table

Inputs		Outputs						
V_{IN}(V)	Fin(KhZ)	FET1	FET2	FET3	Mixer	LB(V)	HB(V)	V_{OUT}(V)
＜14.0	0	Disabled	Active	Active	Active	5.0	0	5.0
>15.5	0	Active	Disabled	Active	Active	5.0	0	5.0
＜14.0	22	Disabled	Active	Active	Active	0	5.0	5.0
>15.5	22	Active	Disabled	Active	Active	0	5.0	5.0

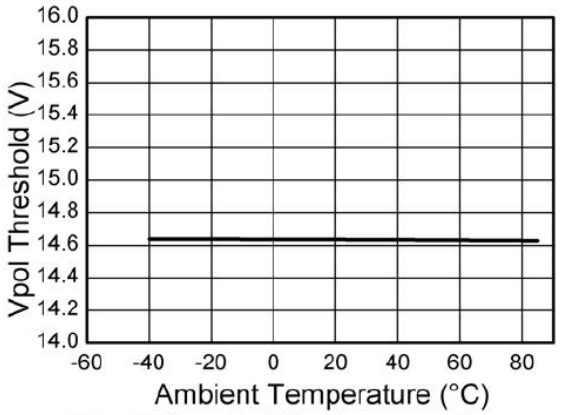
Characteristics Curve



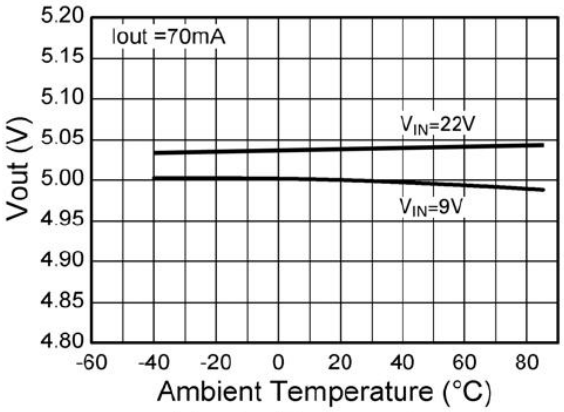
Id1, Id2, Id3 v Rcal



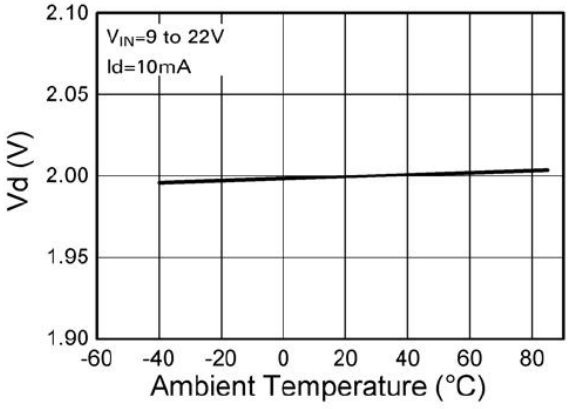
Idm v Rcal



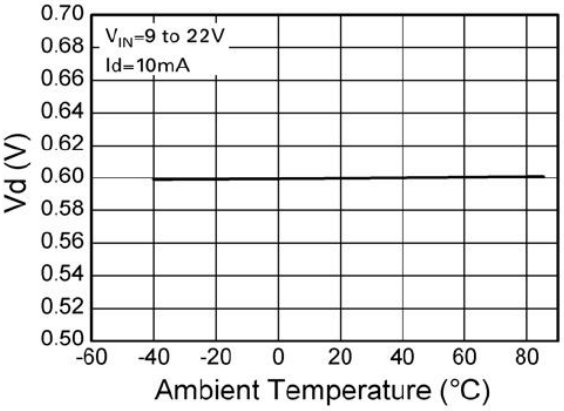
Vpol Threshold v Temperature



Vout v Temperature



Vd1, Vd2, and Vd3 v Temperature



Vdm v Temperature

System Design Considerations – Device Mounting

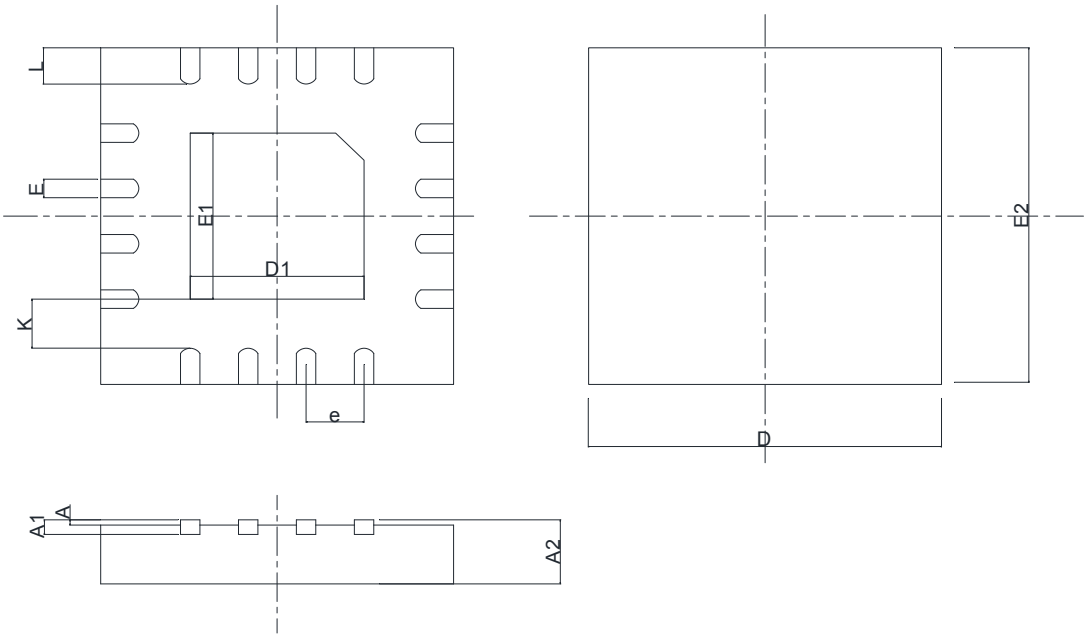
Under normal LNB operation, the regulator function of the D4202 can result in an internal power dissipation of 0.5W to 2W dependant on the LNB design. To help remove the heat generated by the power dissipation the device must be provided with adequate heatsinking. Most of the heat dissipated in the components of the IC flows through the die, die attach and finally the package frame, exiting through the metal tab in the base of the device. It is vital that this tab is soldered to a PCB designed to give a low thermal resistance. This can be achieved by using the following recommendations:

1. Use a double-sided PCB with 1 ounce copper (35mm) or thicker on each side. The back-side of the PCB should have a substantial unbroken area of copper directly underneath the D4202.
2. There should be at least 2, but preferably 4 or more thermal vias in the PCB between the device tab and the back of the board. These should be plated with 0.5 ounce copper (18um) or thicker.
3. The LNB housing must be designed so that the back of the PCB underneath the D4202 is held firmly against a metal surface capable of giving a low thermal resistance path, taking heat away from the PCB. If the metal surface is not smooth, consider using a thermal coupling grease. If the metal housing is assembled inside an enclosure, please consider any effects from thermally insulating materials.
4. Try to minimize LNB power consumption.

The J-C (junction-to-case) thermal resistance of the D4202 is typically 25°C/W for the 3x3 package variants.When designing a PCB for use with the D4202, the user must take into account the likely power dissipation, the recommended maximum die temperature, the maximum ambient temperature and the combined thermal resistance of the D4202 and its PCB mounting arrangement. Zetex has developed a calculator as a guide which can help with this analysis and design considerations.

Outline Dimensions

QFN16(3*3) Unit: mm



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.000	0.050	0.000	0.002
A1	0.203REF.		0.008REF.	
A2	0.700	0.800	0.028	0.031
E	0.180	0.300	0.007	0.012
E1	1.600	1.800	0.063	0.071
E2	2.900	3.100	0.114	0.122
D	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
L	0.300	0.500	0.012	0.020
e	0.500（BSC）		0.020（BSC）	
K	0.200MIN.		0.008MIN.	

Statements

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- The product upgrades without end, Silicore Technology will wholeheartedly provide customers integrated circuits that have better performance and better quality.