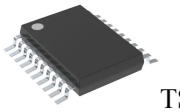
GS75232TSS
Multiple RS-232 Driver and Receiver

General Description


TSSOP20

The GS75232TSS combines three drivers and five receivers. The pinout matches the flow-through design of the SN75C185 to decrease the part count, reduce the board space required, and allow easy interconnection of the UART and serial-port connector of an IBM™PC/AT and compatibles. The bipolar circuits and processing of the GS75232TSS provides a rugged, low-cost solution for this function at the expense of quiescent power and external passive components relative to the SN75C185.

The GS75232TSS complies with the requirements of the TIA/EIA-232-F and ITU (formerly CCITT) V.28 standards. These standards are for data interchange between a host computer and a peripheral at signaling rates up to 20 kbit/s. The switching speeds of these devices are fast enough to support rates up to 120 kbit/s with lower capacitive loads (shorter cables). Interoperability at the higher signaling rates cannot be expected unless the designer has design control of the cable and the interface circuits at both ends. For interoperability at signaling rates up to 120 kbit/s, use of TIA/EIA-423-B (ITU V.10) and TIA/EIA-422-B (ITU V.11) standards is recommended.

The GS75232TSS is available in TSSOP20 package.

Features

- Single chip with easy interface between UART and serial-port connector of IBM™ PC/AT and compatibles
- Meet or exceed the requirements of TIA/EIA-232-F and ITU v.28 standards
- Designed to support data rates up to 120kbit/s
- Pinout compatible with SN75C185 and SN75185

Package Information

Part NO.	Package Description	Package Marking	Package Option
GS75232TSS	TSSOP20	GS75232TSS XXXXX	70/Tube

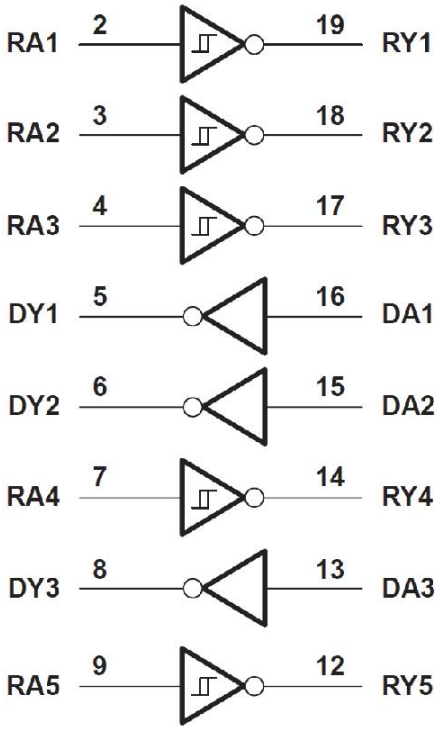
GS75232TSS:Part NO. XXXXX:Lot NO.

Applications

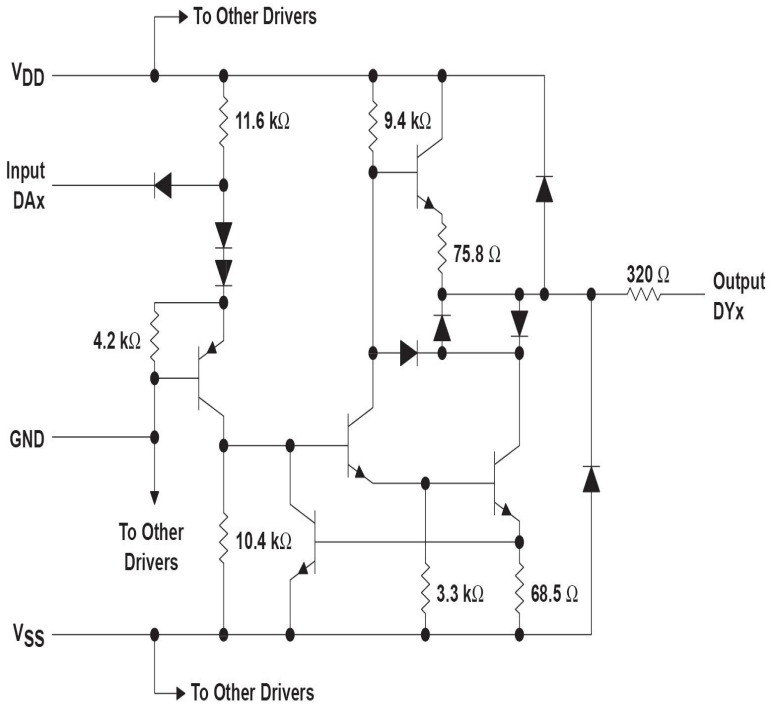
Serial Communication

Functional Block Diagram

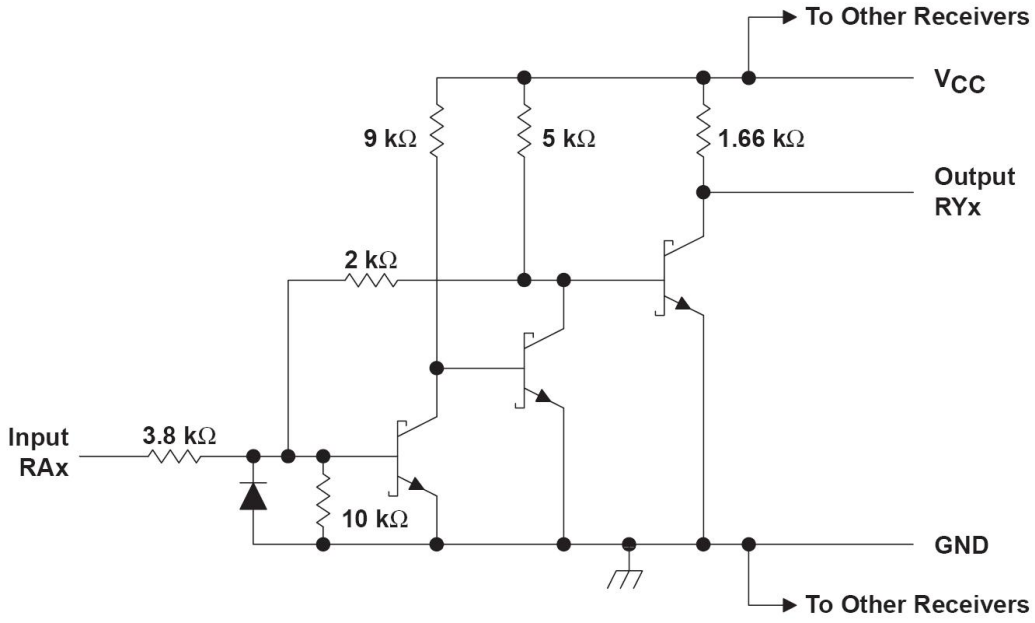
Logic Diagram (Positive Logic)



Schematic (Each Driver)

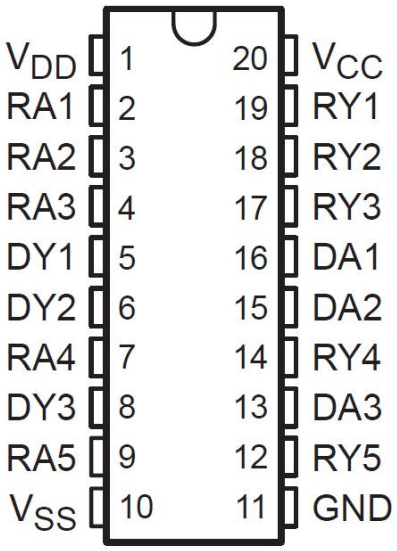


Schematic (Each Receiver)



Resistor Values Shown are Nominal.

Pin Configuration



GS75232TSS(TSSOP20)

Pin Description

Pin Number	Pin Name	Function Description	Pin Number	Pin Name	Function Description
1	V_{DD}	Positive Supply Voltage	11	GND	Ground
2	RA1	Receiver A1 Input	12	RY5	Receiver Y5 Output
3	RA2	Receiver A2 Input	13	DA3	Driver A3 Input
4	RA3	Receiver A3 Input	14	RY4	Receiver Y4 Output
5	DY1	Driver Y1 Output	15	DA2	Driver A2 Input
6	DY2	Driver Y2 Output	16	DA1	Driver A1 Input
7	RA4	Receiver A4 Input	17	RY3	Receiver Y3 Output
8	DY3	Driver Y3 Output	18	RY2	Receiver Y2 Output
9	RA5	Receiver A5 Input	19	RY1	Receiver Y1 Output
10	V_{SS}	Negative Supply voltage	20	V_{CC}	Supply voltage

Absolute Maximum Ratings（Tamb=25℃）

Parameter Name		Symbol	Value	Unit
Supply Voltage (Note 1)		V_{CC}	10	V
		V_{DD}	15	
		V_{SS}	-15	
Input Voltage Range	Driver		-15 ~ +7	V
	Receiver		-30 ~ +30	
Driver Output Voltage Range		Vo	-15 ~ +15	V
Receiver Low-level Output Current		I_{OL}	20	mA
Package Thermal Impedance (Note 2 and 3)	TSSOP20		83	
Operating Virtual Junction Temperature		T_J	150	℃
Storage Temperature Range		Tstg	-65 ~ +150	℃

Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note: 1. All voltages are with respect to the network ground terminal.

Note: 2. Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A)/ \theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

Note: 3. The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

Parameter Name	Symbol		Min	Typ	Max	Unit
Supply Voltage (Note 4)	V_{DD}		7.5	9	15	V
	V_{SS}		-7.5	-9	-15	
	V_{CC}		4.5	5	5.5	
High-Level Input Voltage (driver only)	V_{IH}		1.9			V
Low-Level Input Voltage (driver only)	V_{IH}				0.8	V
High-Level Output Current	I_{OH}	Driver			-6	mA
		Receiver			-0.5	
Low-Level Output Current	I_{OL}	Driver			6	mA
		Receiver			16	
Operating Free-Air Temperature	T_A		0		70	℃

Note4：When powering up the GS75232TSS, the following sequence should be used: 1. VSS 2. VDD 3. VCC 4. I/Os

Applying VCC before VDD may allow large currents to flow, causing damage to the device. When powering down the GS75232TSS,

the reverse sequence should be used.

Supply Currents Over Recommended Operating Free-air Temperature Range

Parameter Name	Symbol	Test Conditions		Min	Typ	Max	Unit
Supply Current from V_{DD}	I_{DD}	All Inputs at 1.9V, No Load	V_{DD}=9V,V_{SS} =−9V			15	mA
			V_{DD}=12V,V_{SS}=−12V			19	
			V_{DD}=15V, V_{SS}=−15V			25	
		All Inputs at 0.8V, No Load	V_{DD}=9V, V_{SS}=−9V			4.5	
			V_{DD}=12V, V_{SS}=−12V			5.5	
			V_{DD}=15V, V_{SS}=−15V			9	
Supply Current from V_{SS}	I_{SS}	All Inputs at 1.9V, No Load	V_{DD}=9V,V_{SS}=−9V			−15	mA
			V_{DD}=12V, V_{SS} =−12V			−19	
			V_{DD}=15V, V_{SS}=−15V			−25	
		All Inputs at 0.8V, No Load	V_{DD}=9V,V_{SS}=−9V			−3.2	
			V_{DD}=12V, V_{SS}=−12V			−3.2	
			V_{DD}=15V,V_{SS}=−15V			−3.2	
Supply Current from V_{CC}	I_{CC}	All Inputs at 5V, No Load, Vcc=5V				30	mA

Driver Section

Electrical Characteristics Over Recommended Operating Free-air Temperature Range

(V_{DD}=9V,V_{SS}=-9V,V_{CC}=5V, Unless otherwise noted)

Parameter Name	Symbol	Test Conditions	Min	Typ	Max	Unit
High-level Output Voltage	V_{OH}	V_{IL}=0.8V,R_L=3k, (See Figure 1)	6.0	7.5		V
Low-level Output Voltage (See Note 5)	V_{OL}	V_{IH}=1.9V,R_L=3k, (See Figure 1)		-7.5	-6.0	V
High-level Input Current	I_{IH}	V_I=5V, (See Figure 2)			10.0	μA
Low-level Input Current	I_{IL}	V_I=0V, (See Figure 2)			-1.6	mA
High-level Short-Circuit Output Current (See Note 6)	$I_{OS(H)}$	V_{IL}=0.8V,V_O=0, (See Figure 1)	-4.5	-12.0	-19.5	mA
Low-level Short-Circuit Output Current	$I_{OS(L)}$	V_{IH}=2V,V_O=0, (See Figure 1)	4.5	12.0	19.5	mA
Output Resistance (See Note 7)	R_O	V_{CC}=V_{DD}=V_{SS}=0, V_O=−2V to 2V	300			Ω

Note 5. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only (e.g, if−10V is maximum, the typical value is a more negative voltage).

Note 6. Output short-circuit conditions must maintain the total power dissipation below absolute maximum ratings.

Note 7. Test conditions are those specified by TIA/EIA-232-F and as listed above.

Switching Characteristics

(V_{DD}=12V,V_{SS}=-12V,V_{CC}=5V,Ta=25℃,Unless otherwise noted)

Parameter Name	Symbol	Test Conditions		Min	Typ	Max	Unit
Propagation Delay Time, Low to High-level Output	t_{PLH}	R_L=3KΩ to 7KΩ,C_L=15pF (See Figure 3)			315	500	ns
Propagation Delay Time, High to Low-level Output	t_{PHL}	R_L=3KΩ to 7KΩ,C_L=15pF (See Figure 3)			75	175	ns
Transition Time, Low to High-level Output	t_{TLH}	R_L=3KΩ to 7KΩ	C_L=15pF (See Figure 3)		60	100	ns
			C_L=2500pF (See Figure 3) (Note 8)		1.7	2.5	μs
Transition Time, High to Low-level Output	t_{THL}	R_L=3KΩ to 7KΩ	C_L=15pF (See Figure 3)		40	75	ns
			C_L=2500pF (See Figure 3) (Note 8)		1.5	2.5	μs

Note 8. Measured between ±3-V and ±3-V points of the output waveform (TIA/EIA-232-F conditions); all unused inputs are tied either high or low.

Receiver Section

Electrical Characteristics Over Recommended Operating Conditions

(ALL Typical Values are at V_{DD}=9V,V_{SS}=-9V,V_{CC}=5V, T_A=25℃, Unless otherwise noted)

Parameter Name	Symbol	Test Conditions		Min	Typ	Max	Unit
Positive-going Input Threshold Voltage	V_{IT+}	T_A=25℃, (See Figure 5)		1.75	1.9	2.3	V
		T_A=0℃ to 70℃, (See Figure 5)		1.55		2.3	
Negative-going Input Threshold	V_{IT-}			0.75	0.97	1.25	V
Input Hysteresis Voltage (V_{IT+} − V_{IT-})	Vhys			0.5			V
High-level Output Voltage	V_{OH}	I_{OH}=−0.5mA	V_{IH}=0.75V	2.6	4	5	V
			Inputs Open	2.6			
Low-level Output Voltage	V_{OL}	I_{OL}=10mA,V_I=3V			0.2	0.45	V
High-level Input Current	I_{IH}	V_I=25V, (See Figure 5)		3.6		8.3	mA
		V_I=3V, (See Figure 5)		0.43			
Low-level Input Current	I_{IL}	V_I=−25V, (See Figure 5)		-3.6		-8.3	mA
		V_I=−3V, (See Figure 5)		-0.43			
Short-circuit OutputCurrent	I_{OS}	(See Figure 4)			-3.4	-12	mA

Switching Characteristics

(V_{DD}=12V,V_{SS}=-12V,V_{CC}=5V,Ta=25℃,unless otherwise noted)

Parameter Name	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time, Low to High-level Output	t_{PLH}	C_L=50pF,R_L=5 k (See Figure 6)		107	250	ns
Propagation Delay Time, High to Low-level Output	t_{PHL}			42	150	ns
Transition Time, Low to High-level Output	t_{TLH}			175	350	ns
Transition Time, High to Low-level Output	t_{THL}			16	60	ns
Propagation Delay Time, Low to High-level Output	t_{PLH}	C_L=15pF, R_L=1.5k (See Figure 6)		100	160	ns
Propagation Delay Time, High to Low-level Output	t_{PHL}			60	100	ns
Transition Time, Low to High-level Output	t_{TLH}			90	175	ns
Transition Time, High to Low-level Output	t_{THL}			15	50	ns

Parameter Measurement Information

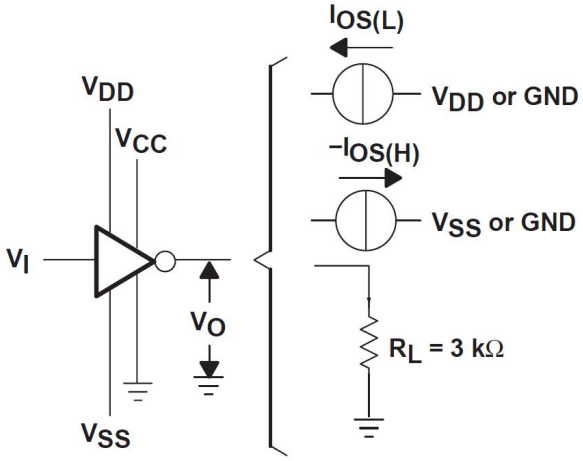


Fig.1 Driver Test Circuit for V_{OH},V_{OL},$I_{OS(H)}$and $I_{OS(L)}$

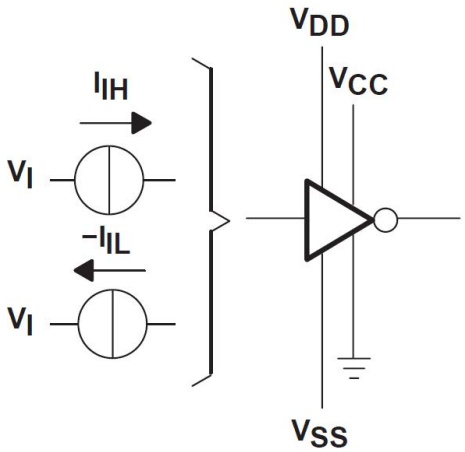
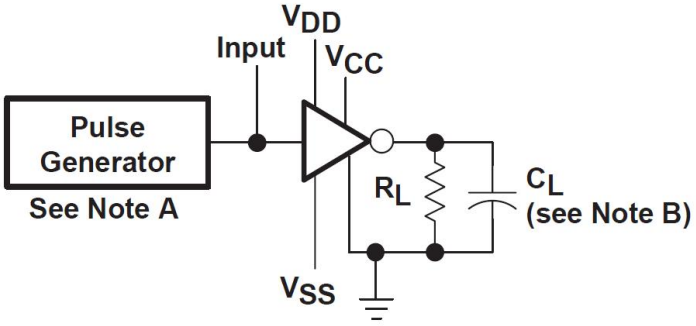


Fig.2 Driver Test Circuit for I_{IH} and I_{IL}



Note: A. The pulse generator has the following characteristics: t_W=25μs,PRR=20kHz,Z_O=50Ω,tr=t_f<50ns

Note B. C_L includes probe and jig capacitance.

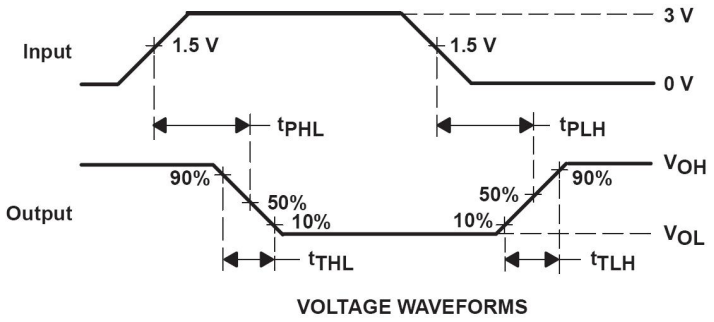


Fig.3 Driver Test Circuit and Voltage Waveforms

Parameter Measurement Information

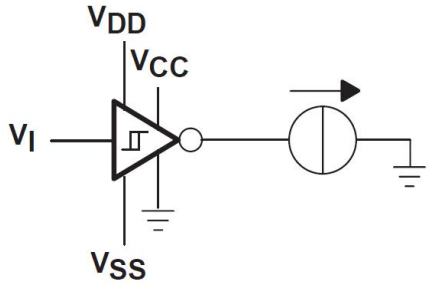


Fig.4 Receiver Test Circuit for I_{OS}

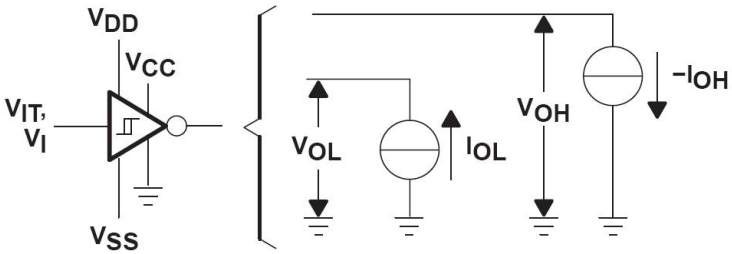
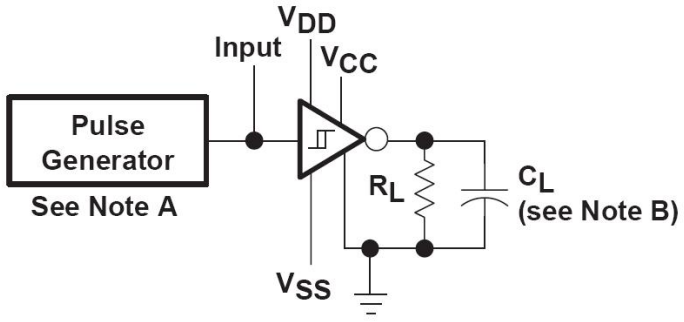


Fig.5 Receiver Test Circuit for V_{IT},V_{OH} and V_{OL}



Note: A. The pulse generator has the following characteristics: t_W=25μs,PRR=20kHz, Z_O=50Ω,tr=t_f<50ns

Note B. C_L includes probe and jig capacitance.

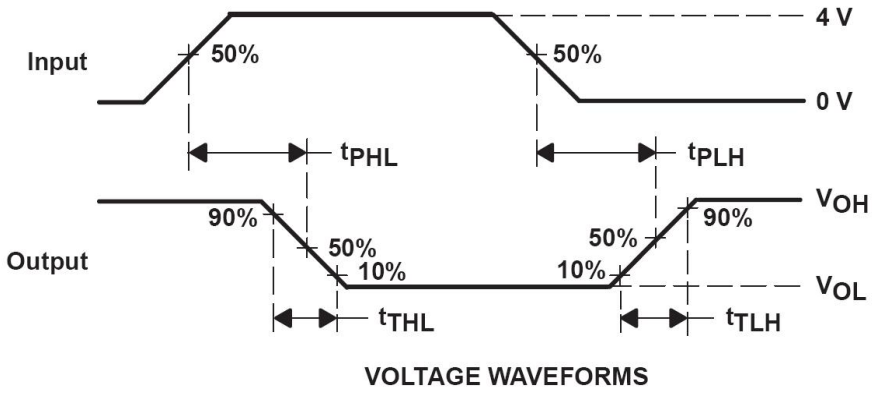


Fig 6. Receiver Propagation and Transition Times

Typical Characteristics Driver Section

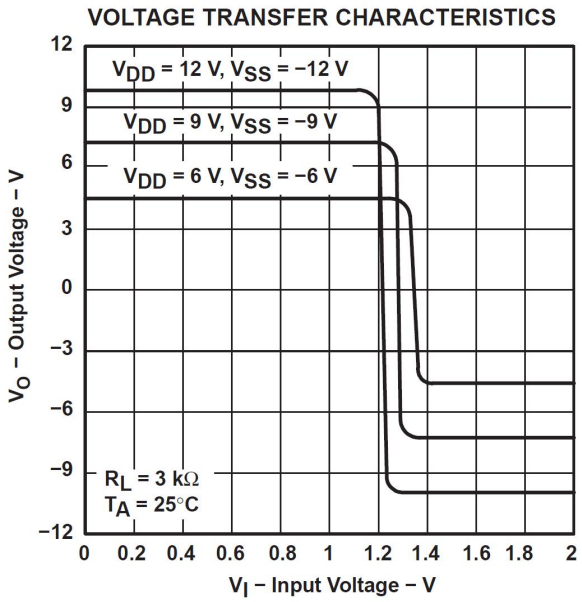


Figure 7

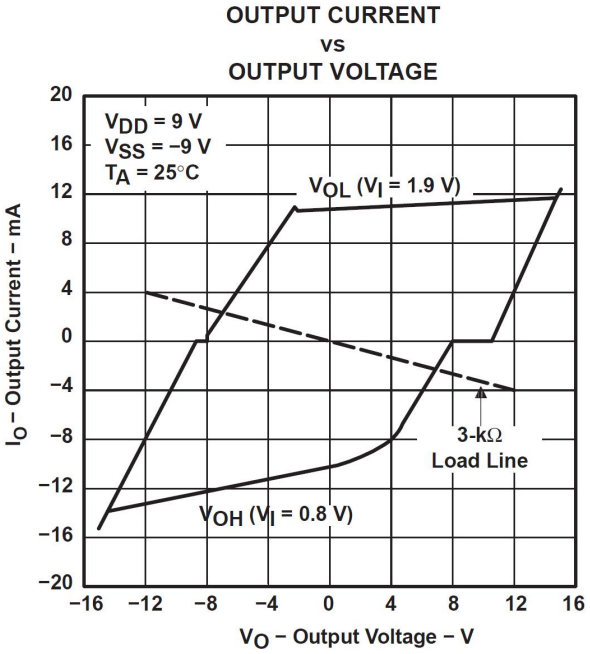


Figure 8

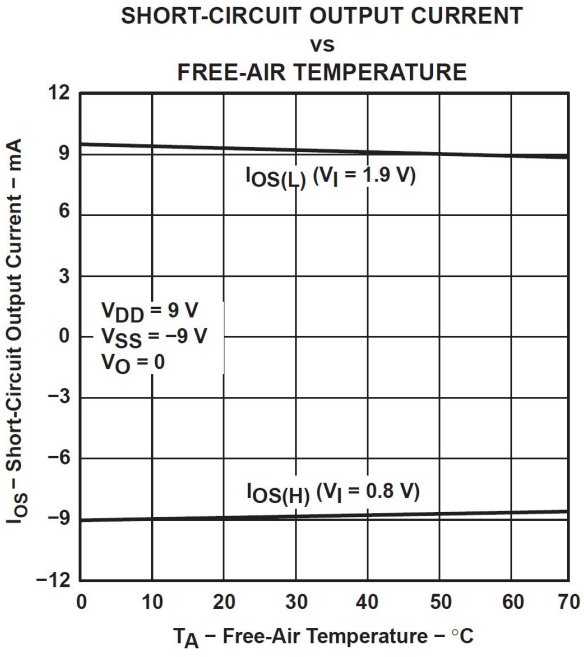


Figure 9

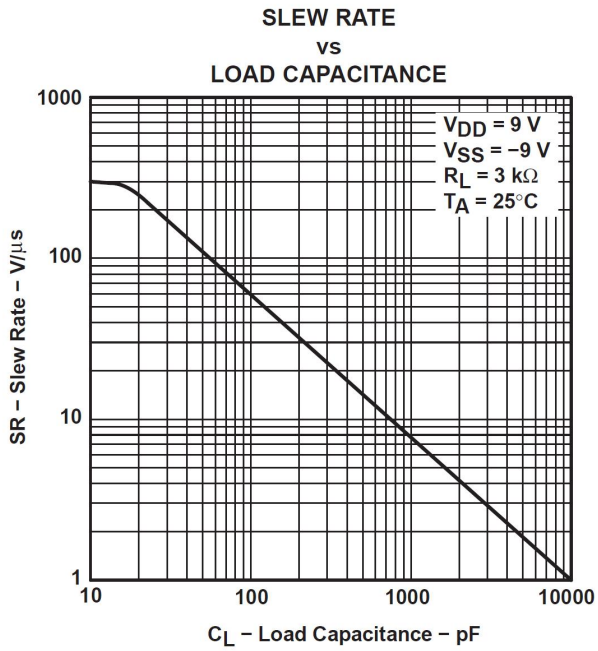


Figure 10

Typical Characteristics Driver Section(Cont.)

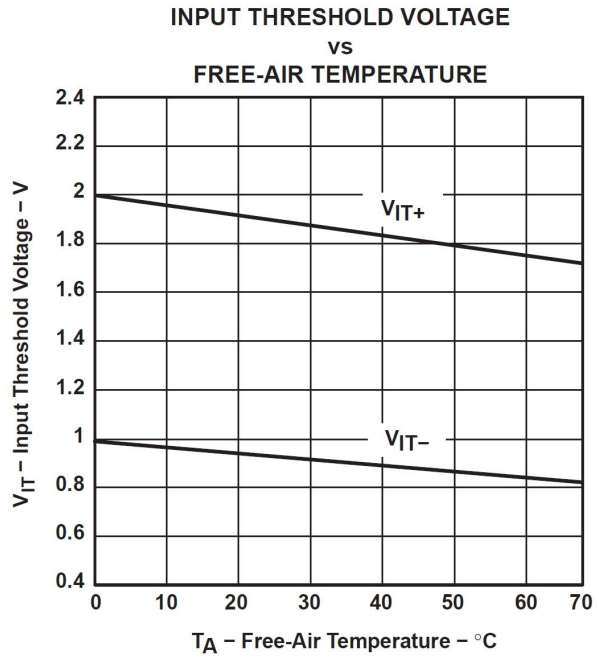


Figure 11

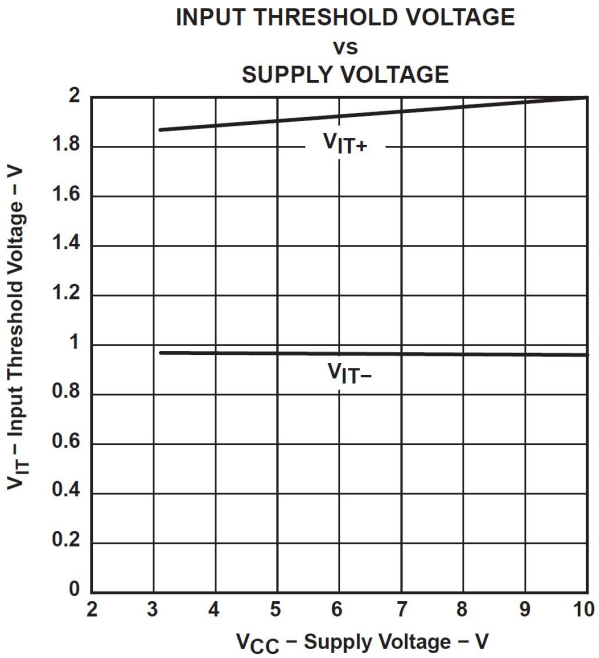
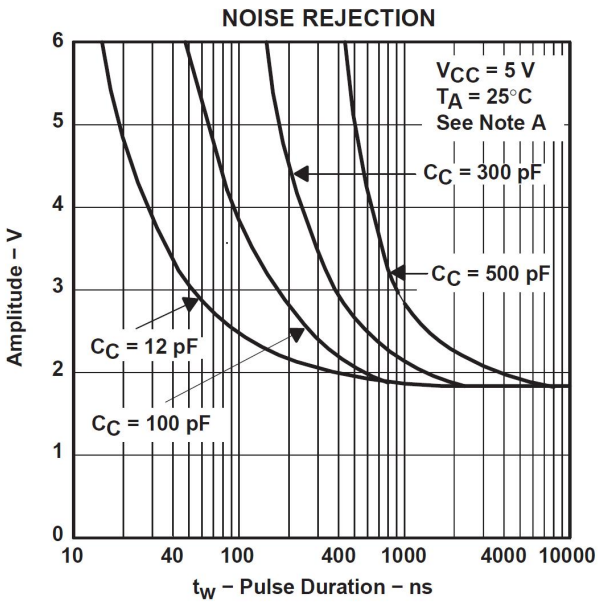


Figure 12



NOTE A: This figure shows the maximum amplitude of a positive-going pulse that, starting from 0 V, does not cause a change of the output level.

Figure 13

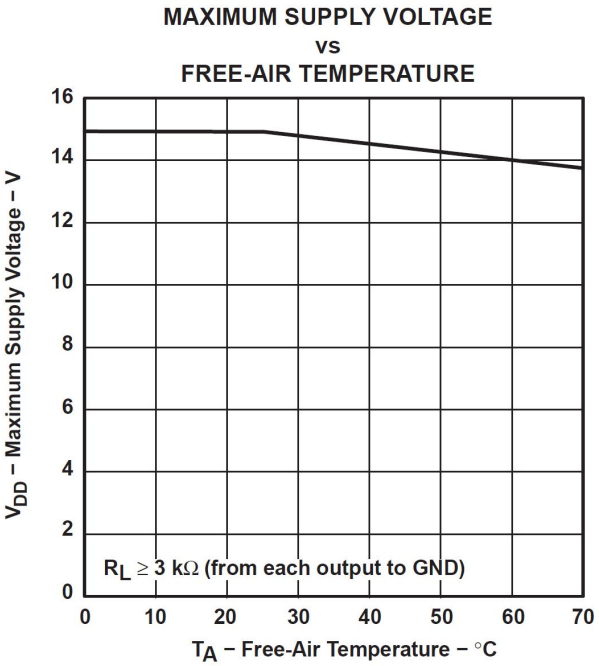


Figure 14

Application Information

Diodes placed in series with the V_{DD} and V_{SS} leads protect the GS75232TSS in the fault condition in which the device outputs are shorted to ±15 V and the power supplies are at low and provide low-impedance paths to ground

(see Figure 15).

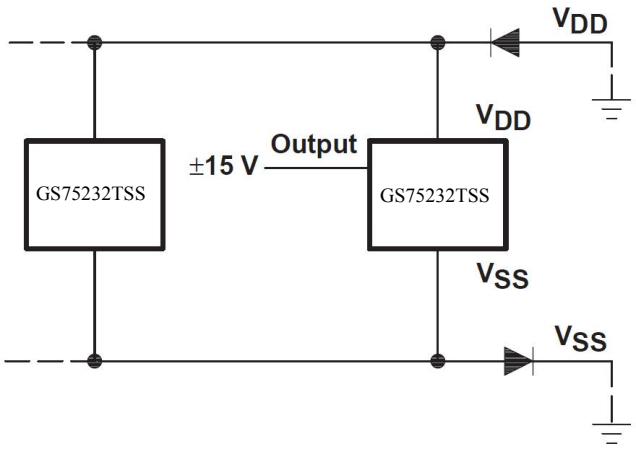


Fig.15 Power-Supply Protection to Meet Power-Off Fault Conditions of TIA/EIA-232-F

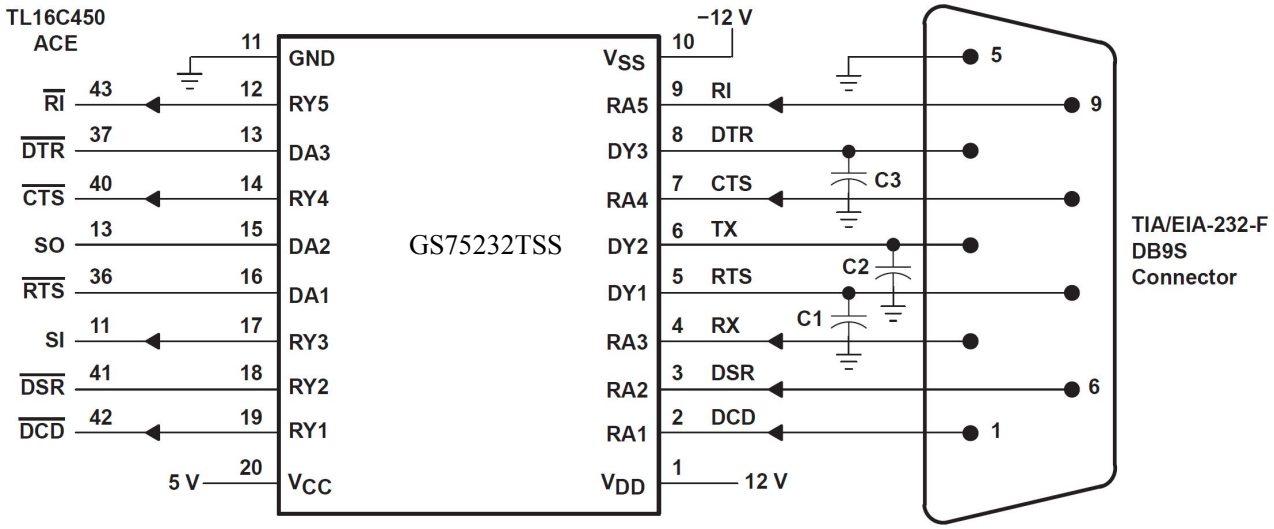
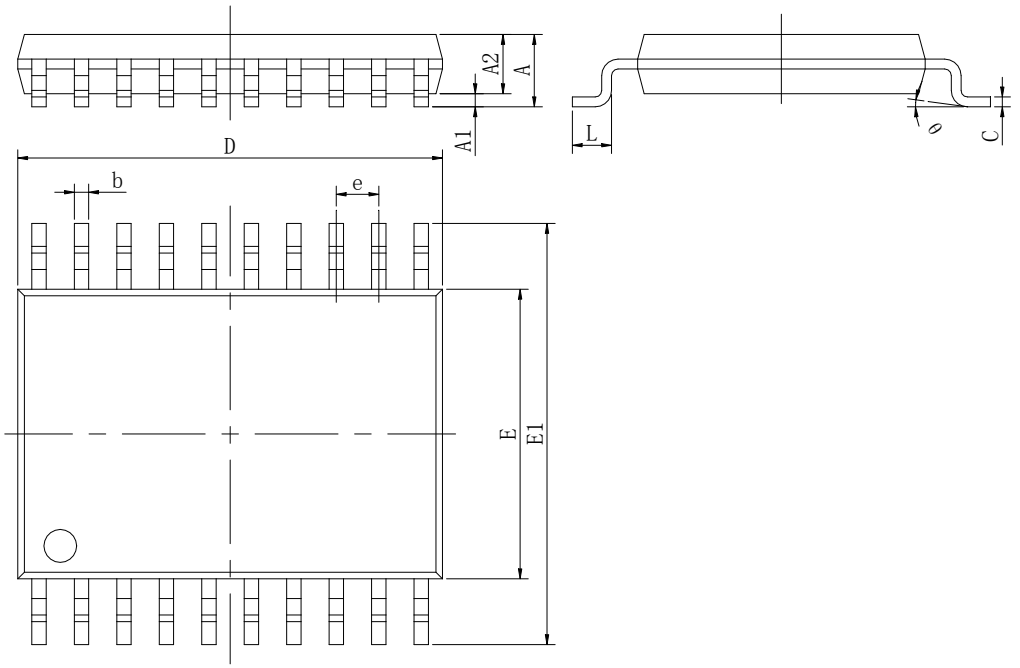


Fig.16 Typical Connection

Outline Dimensions

TSSOP20 Unit:mm



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	---	1.100	---	0.043
A1	0.150	0.200	0.006	0.008
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	6.400	6.600	0.252	0.260
E	4.340	4.540	0.171	0.179
E1	6.250	6.550	0.246	0.258
e	0.650(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
θ	1°	7°	1°	7°

Statements

- Silicore Technology reserves the right to make changes without further notice to any products or specifications herein. Before customers place an order, customers need to confirm whether datasheet obtained is the latest version, and to verify the integrity of the relevant information.

- Failure or malfunction of any semiconductor products may occur under particular conditions, customers shall have obligation to comply with safety standards when customers use Silicore Technology products to do their system design and machine manufacturing, and take corresponding safety measures in order to avoid potential risk of failure that may cause personal injury or property damage.

- The product upgrades without end, Silicore Technology will wholeheartedly provide customers integrated circuits that have better performance and better quality.