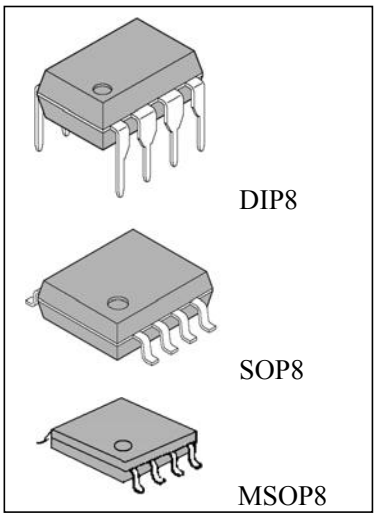
# D706/D706T/D706S
## Low Power µP Supervisor Circuits

### DESCRIPTION

The D706/D706T/D706S CMOS supervisor circuits monitor power-supply and battery voltage level, and µP/µC operation. Compared to pin-compatible devices offered by Maxim Integrated Products, these devices feature 60 percent lower maximum supply current.




The family offers several functional options. Each device generates a reset signal during power-up, power-down and during brownout conditions.

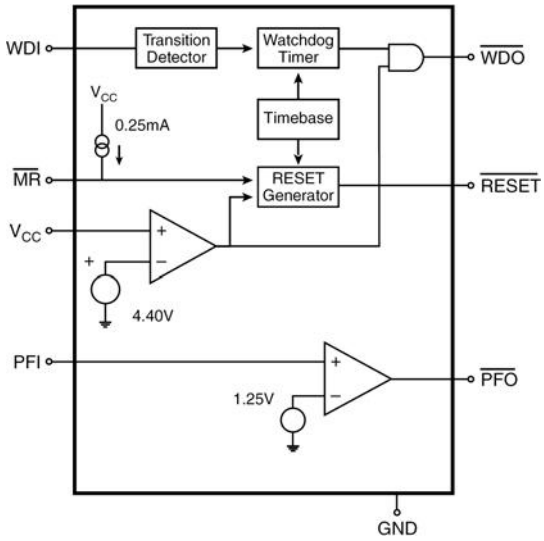
A reset is generated when the supply drops below4.4V (D706),3.08V (D706T),2.93V(D706S).In addition,the D706/T/S feature a 1.6 second watchdog timer. A versatile power-fail circuit has a1.25V threshold, useful in checking battery levels and non-5V supplies. All devices have a manual reset ( $\overline{MR}$ ) input. The watchdog timer output will trigger a reset if connected to $\overline{MR}$.

All devices are available in DIP8, SOP8 and MSOP8 packages.

### FEATURES

- Improved replacements for the Maximum D706/T/S
  - 140µA maximum supply current
  - 60% improvement
- Precision power supply monitor
  - 4.4V threshold (D706)
  - 3.08V threshold (D706T)
  - 2.93V threshold (D706S)
- Debounced manual reset input
- Voltage monitor
  - 1.25V threshold
  - Battery monitor/Auxiliary supply monitor

### BLOCK DIAGRAM

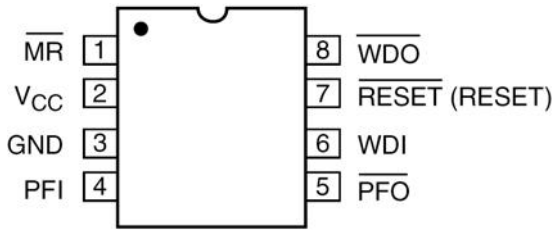


- Watchdog timer (D706/D706T/D706S)
- 300ms reset pulse width
- MicroSO Package

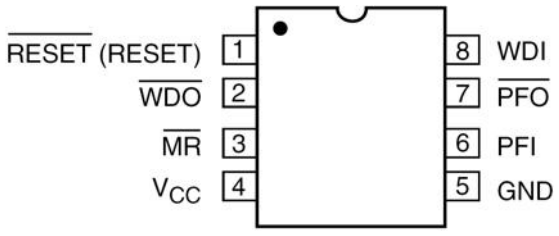
## APPLICATIONS

- Computers and embedded controllers
- Intelligent instruments
- PDAs and handheld equipment
- Battery-operated systems
- Wireless communication systems

## PIN CONFIGURATION




DIP/SOP8




MSOP8

## PIN DESCRIPTION

| Pin No. | | Name | Pin Function |
|---|---|---|---|
| D706/706T/D706S | | | |
| DIP/SOP | MSO | | |
| 1 | 3 | $\overline{MR}$ | Manual RESET input. The active LOW input triggers a reset pulse. A 250μA pull-up current allows the pin to be driven by TTL / CMOS logic or shorted to ground with a switch. |
| 2 | 4 | Vcc | +5V power supply input. |
| 3 | 5 | GND | Ground reference for all signals. |
| 4 | 6 | PFI | Power-fail voltage monitor input. With PFI less than 1.25V, $\overline{PFO}$ goes low. Connect PFI to ground or $V_{CC}$ when not used. |
| 5 | 7 | $\overline{PFO}$ | Power-fail output. The output is active LOW and sinks current when PFI is less than1.25V. |
| 6 | 8 | WDI | Watchdog input. WDI controls the internal watchdog timer. A HIGH or LOW signal for2.4sec at WDI allows the internal timer to run-out, setting $\overline{WDO}$ LOW. The watchdog function is disabled by floating WDI or by connecting WDI to a high-impedance |

| | | | |
|---|---|---|---|
| 6 | 8 | WDI | three-state buffer. The internal watchdog timer clears when: RESET is asserted; WDI is three-stated; or WDI sees a rising or falling edge. |
| 7 | 1 | $\overline{RESET}$ | Active-LOW reset output. Pulses LOW for 300ms when triggered, and stays low whenever Vcc is below the reset threshold (D706: 4.4V, D706T: 3.08V, D706S: 2.93 V). $\overline{RESET}$ remains LOW for 300ms after Vcc rises above the RESET threshold or $\overline{MR}$ goes from LOW to HIGH. A watchdog timeout will not trigger $\overline{RESET}$ unless $\overline{WDO}$ is connected to $\overline{MR}$. |
| 8 | 2 | $\overline{WDO}$ | Watchdog output. $\overline{WDO}$ pulls LOW when the 1.6 sec internal watchdog timer times-out and does not go HIGH until the watchdog is cleared. In addition, when Vcc is below the reset threshold, $\overline{WDO}$ remains low. Unlike $\overline{RESET}$, $\overline{WDO}$ does not have a minimum pulse width and as soon as Vcc exceeds the reset threshold, $\overline{WDO}$ goes HIGH with no delay. |

**ABSOLUTE MAXIMUM RATING** (Ta=25℃)

| Characteristics | Va lue | Unit |
|---|---|---|
| Supply voltage | -0.3 ～+6.0 | V |
| All other inputs *1 | -0.3 ～Vcc+0.3 | V |
| Input current at Vcc and GND | 20 | mA |
| Output current :All outputs | 20 | mA |
| Rate of Rise at Vcc | 100 | V/μs |
| Plastic DIP power dissipation (Derate 9mW/℃ above 70℃) | 700 | mW |
| SOP power dissipation (Derate 5.9mW/℃ above 70℃) | 470 | mW |
| MSOP power dissipation (Derate 4.1mW/℃ above 70℃) | 330 | mW |
| Operating temperature range | 0～70 | ℃ |
| Storage temperature range | -65 ～+150 | ℃ |
| Lead temperature (soldering,10 sec.) | 300 | ℃ |

*1. *The input voltage limits on PFI and $\overline{MR}$ can be exceeded if the input current is less than 10mA.*

## ELECTRICAL CHARACTERISTICS

（ Unless otherwise noted, $V_{CC}$ = 4.5V to 5.5V for the D706/D706T/D706S）

| Characteristics | Symbol | Conditions | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Operating voltage range | Vcc | D706/T/S | 1.2 | | 5.5 | V |
| Supply current | Icc | D706/T/S | | 75 | 140 | μA |
| $\overline{RESET}$ threshold | $V_{RT}$ | D 706 | 4.25 | 4.4 | 4.5 | V |
| | | D 706 T | 2.98 | 3.08 | 3.15 | |
| | | D 706 S | 2.83 | 2.93 | 3 | |
| $\overline{RESET}$ threshold hysteresis | | | | 40 | | mV |
| $\overline{RESET}$ pulse width | $t_{RS}$ | | 140 | 200 | 280 | ms |
| $\overline{MR}$ pulse width | $t_{MR}$ | | 0.15 | | | μ s |
| $\overline{MR}$ to $\overline{RESET}$ out delay | $t_{MD}$ | | | | 0.25 | μ s |
| $\overline{MR}$ input threshold | $V_{IH}$ | | 2.0 | | | V |
| | $V_{IL}$ | | | | 0.8 | |
| $\overline{MR}$ pull-up current | | $\overline{MR}$ =0V | 100 | 250 | 600 | μ A |
| $\overline{RESET}$ output voltage | | $I_{SOURCE}$ =800μA | Vcc-1.5 | | | V |
| | | $I_{SINK}$ =3.2mA | | | 0.4 | |
| | | D706/T/S,Vcc=1.2 V, $I_{SINK}$ =100μA | | | 0.3 | |
| Watchdog timeout period | $t_{WD}$ | D 706 / T/ S | 1.00 | 1.60 | 2.25 | s |
| WDI pulse width | $t_{WP}$ | $V_{IL}$ =0.4V,$V_{IH}$ =0.8Vcc | 50 | | | ns |
| WDI input threshold | $V_{IH}$ | D706/T/S ,Vcc=5V | 3.5 | | | V |
| | $V_{IL}$ | | | | 0.8 | |
| WDI input current | | D 706 / T/ S,WDI=Vcc | | 50 | 150 | μA |
| | | D 706 / T/ S,WDI=0V | - 150 | - 50 | | |
| $\overline{WDO}$ output voltage | | D706/T/S, $I_{SOURCE}$ =800μA | Vcc-1.5 | | | V |
| | | D706/T/S, $I_{SINK}$ =1.2mA | | | 0.4 | |
| PFI input threshold | | Vcc=5V | 1.20 | 1.25 | 1.30 | V |
| PFI input current | | | -25 | 0.01 | 25 | nA |
| $\overline{PFO}$ output voltage | | $I_{SOURCE}$ =800μA | Vcc-1.5 | | | V |
| | | $I_{SINK}$ =3.2mA | | | 0.4 | |

## FEATURE SUMMARY

| | D706 | D706T | D706S |
|---|---|---|---|
| Power-fail detector | ● | ● | ● |
| Brownout detection | ● | ● | ● |
| Manual RESET input | ● | ● | ● |
| Power- up/down RESET | ● | ● | ● |
| Watchdog timer | ● | ● | ● |
| Active-HIGH RESET output | | | |
| Active-LOW RESET output | ● | ● | ● |
| RESET threshold | 4.4V | 3.08V | 2.93V |

## DETAIL DESCRIPTIONS

### $\overline{RESET}$ Operation

The $\overline{RESET}$ signals are designed to start a μP/μC in a known state or return the system to a known state.

$\overline{RESET}$ is guaranteed to be LOW with Vcc above 1.2V. During a power-up sequence, $\overline{RESET}$ remains low until the supply rises above the threshold level, either 4.4V, 3.08V, 2.93V. $\overline{RESET}$ goes high approximately 200ms after crossing the threshold.

During power-down, $\overline{RESET}$ goes LOW as Vcc falls below the threshold level and is guaranteed to be under 0.4V with Vcc above 1.2V.

In a brownout situation where Vcc falls below the threshold level, $\overline{RESET}$ pulses low. If a brownout occurs during an already initiated reset, the pulse will continue for a minimum of 140ms.

### Auxiliary Comparator

All devices have an auxiliary comparator with 1.25V trip point and uncommitted output ( $\overline{PFO}$ ) and noninverting input (PFI). This comparator can be used as a supply voltage monitor with an external resistor voltage divider. The attenuated voltage at PFI should be set just below the 1.25 threshold. As the supply level falls, PFI is reduced causing the $\overline{PFO}$ output to transit LOW. Normally $\overline{PFO}$ interrupts the processor so the system can be shut down in a controlled manner.

### Manual Reset ( $\overline{MR}$ )

The active-LOW manual reset input is pulled high by a 250μA pull-up current and can be driven low by CMOS/TTL logic or a mechanical switch to ground. An external debounce circuit is unnecessary since the 140ms minimum reset time will debounce mechanical pushbutton switches.

By connecting the watchdog output ( $\overline{WDO}$ ) and $\overline{MR}$, a watchdog timeout forces $\overline{RESET}$ to be generated.

### Watchdog Timer

The watchdog timer available on the D706/D706T/D706S monitors μP/μC activity. If activity is not detected within 1.6 seconds, the internal timer puts the watchdog output, $\overline{WDO}$ ,into a LOW state . $\overline{WDO}$ will remain LOW until activity is detected at WDI.

The watchdog function is disabled, meaning it is cleared and not counting, if WDI is floated or connected to a three-stated circuit. The watchdog timer is also disabled if RESET is asserted. When RESET becomes inactive and the WDI input sees a high or low transition as short as 50ns, the watchdog timer will begin a 1.6 second countdown. Additional transitions at WDI will reset the watchdog timer and initiate a new countdown sequence.

$\overline{WDO}$ will also become LOW and remain so, whenever the supply voltage, Vcc , falls below the device threshold level. $\overline{WDO}$ goes HIGH as soon as Vcc transitions above the threshold. There is no minimum pulse width for $\overline{WDO}$ as there is for the RESET outputs. If WDI is floated, $\overline{WDO}$ essentially acts as a low-power output indicator.

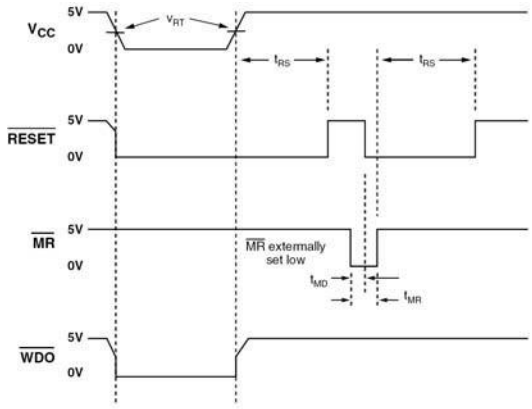



*Figure 1. WDI Three-state operation*

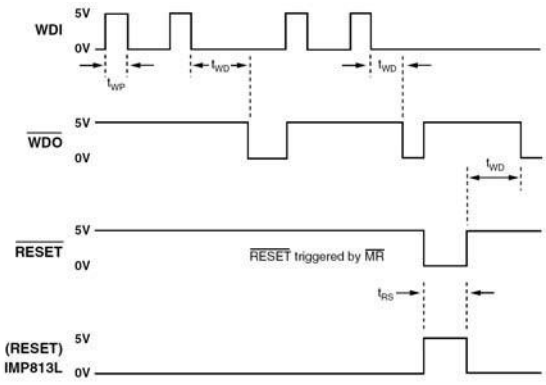



*Figure 2. Watchdog Timing*

## APPLICATION INFORMATION

**Ensuring That $\overline{RESET}$ is Valid Down to Vcc = 0V**

When Vcc falls below 1.1V, the D706/D706T/D706S $\overline{RESET}$ output no longer pulls down; it becomes indeterminate. To avoid the possibility that stray charges build up and force $\overline{RESET}$ to the wrong state, a pull-down resistor should be connected to the $\overline{RESET}$ pin,thus draining such charges to ground and holding RESET low. The resistor value is not critical. A 100k Ω resistor will pull $\overline{RESET}$ to ground without loading it.

**Bi-directional Reset Pin Interfacing**

The D706/D706T/D706S can interface with μP/μC bi-directional reset pins by connecting a 4.7k Ω resistor in series with the $\overline{RESET}$ output μP/μC bi-directional $\overline{RESET}$ pin.

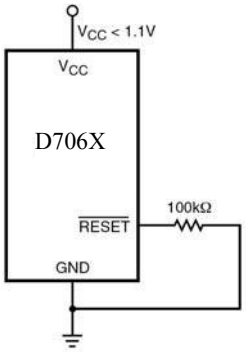



*Figure 3. Ensuring That $\overline{RESET}$ is Valid Down to $V_{CC}$ = 0V*

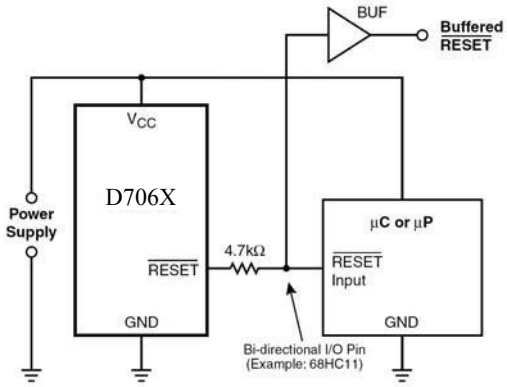



*Figure 3. Bi-directional Reset Pin Interfacing*

**Monitoring Voltages Other Than Vcc**

The D706/D706T/D706S can monitor voltages other than Vcc using the Power Fail circuitry. If a resistive divider is connected from the voltage to be monitored to the power Fail input, PFI, the $\overline{PFO}$ (output) will go LOW if the divider voltage goes below its 1.25V reference. Should hysteresis be desired, connect a resistor (equal to approximately 10 times the sum of the two resistors in the divider) between the PFI and $\overline{PFO}$ pins. A capacitor between PFI and GND will reduce circuit sensitivity to input high-frequency noise. If it is desired to assert a RESET in addition to the $\overline{PFO}$ flag, this may be achieved by connecting the $\overline{PFO}$ output to $MR$.

**Monitoring a Negative Voltage**

The Power-Fail circuitry can also monitor a negative supply rail. When the negative rail is OK, $\overline{PFO}$ will be LOW, and when the negative rail is failing (not negative enough), $\overline{PFO}$ goes HIGH(the opposite of when positive voltages are monitored). To trigger a reset, these outputs need to be inverted: adding the resistors and transistor as shown achieves this. The $\overline{RESET}$ output will then have the same sense as for positive voltages: good = HIGH, bad = LOW. It should be noted that this circuit's accuracy depends on the Vcc line, the PFI threshold tolerance, and the resistors.

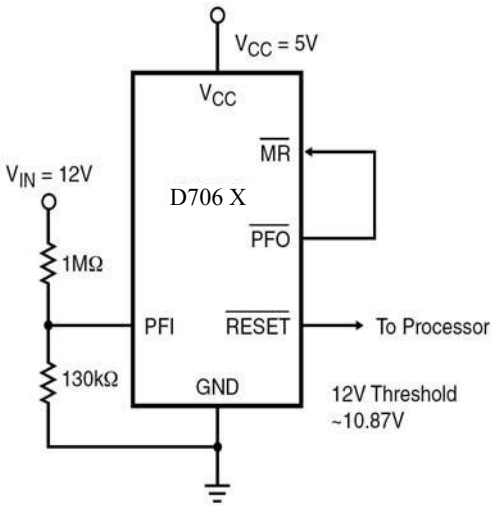



*Figure 4. Monitoring Voltages Other Than $V_{CC}$*

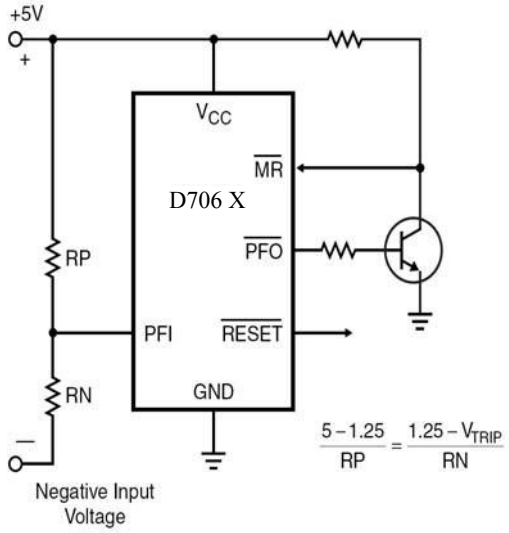


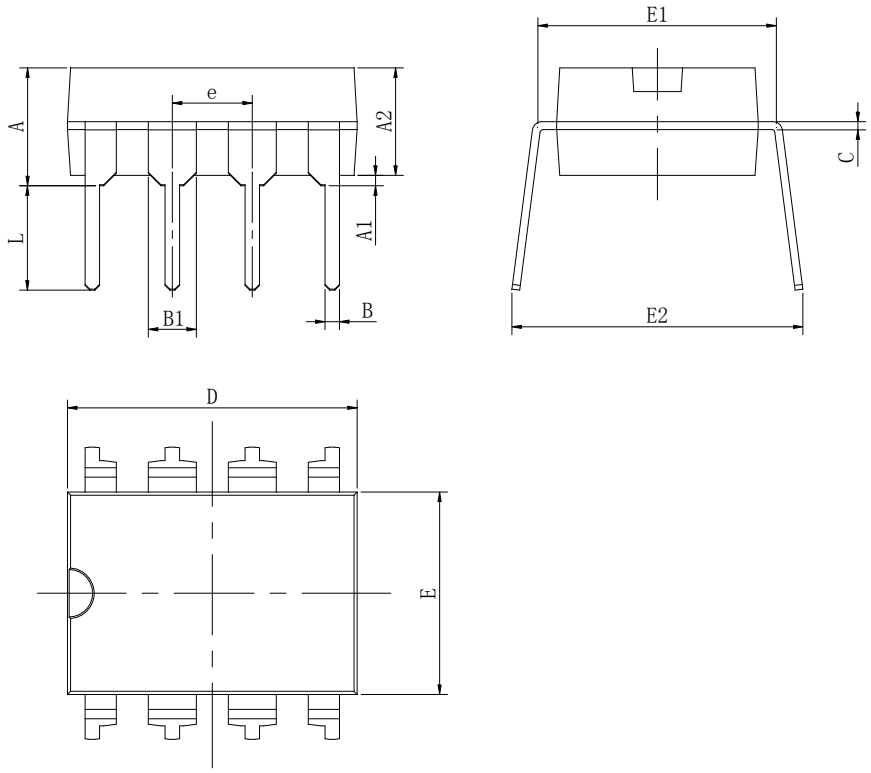

*Figure 5. Monitoring a Negative Voltage*

## PRINT INFORMATIONS

| Voltage | Marking | | |
|---|---|---|---|
| | DIP8 | SOP8 | MSOP8 |
| 4 . 40 V | D 706 | D 706 F | D 706 M |
| 3 . 08 V | D 706 T | D 706 TF | D 706 TM |
| 2 . 93 V | D 706 S | D 706 SF | D 706 SM |

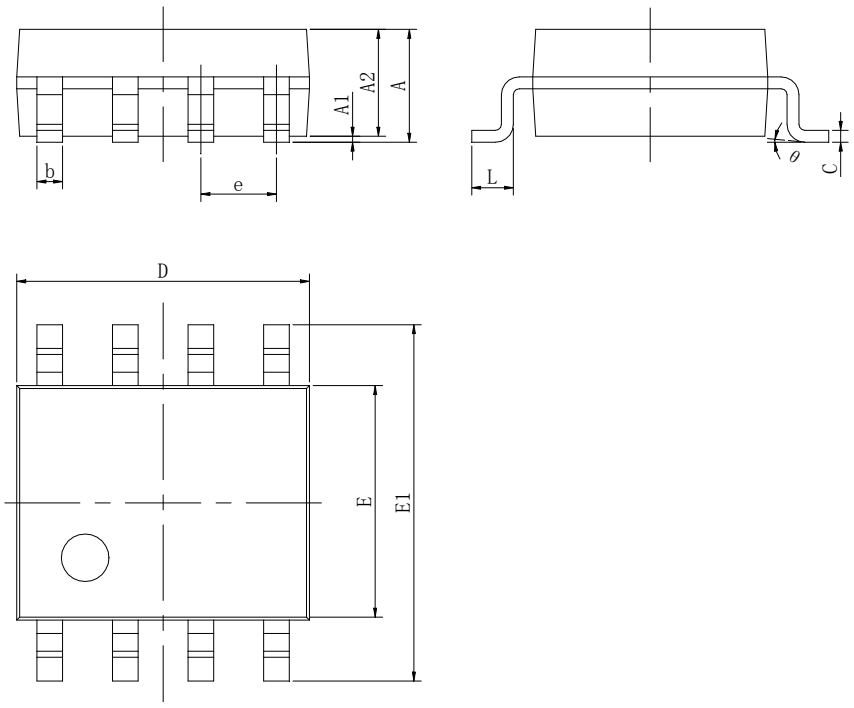
## OUTLINE DRAWING

**DIP8** Unit: mm



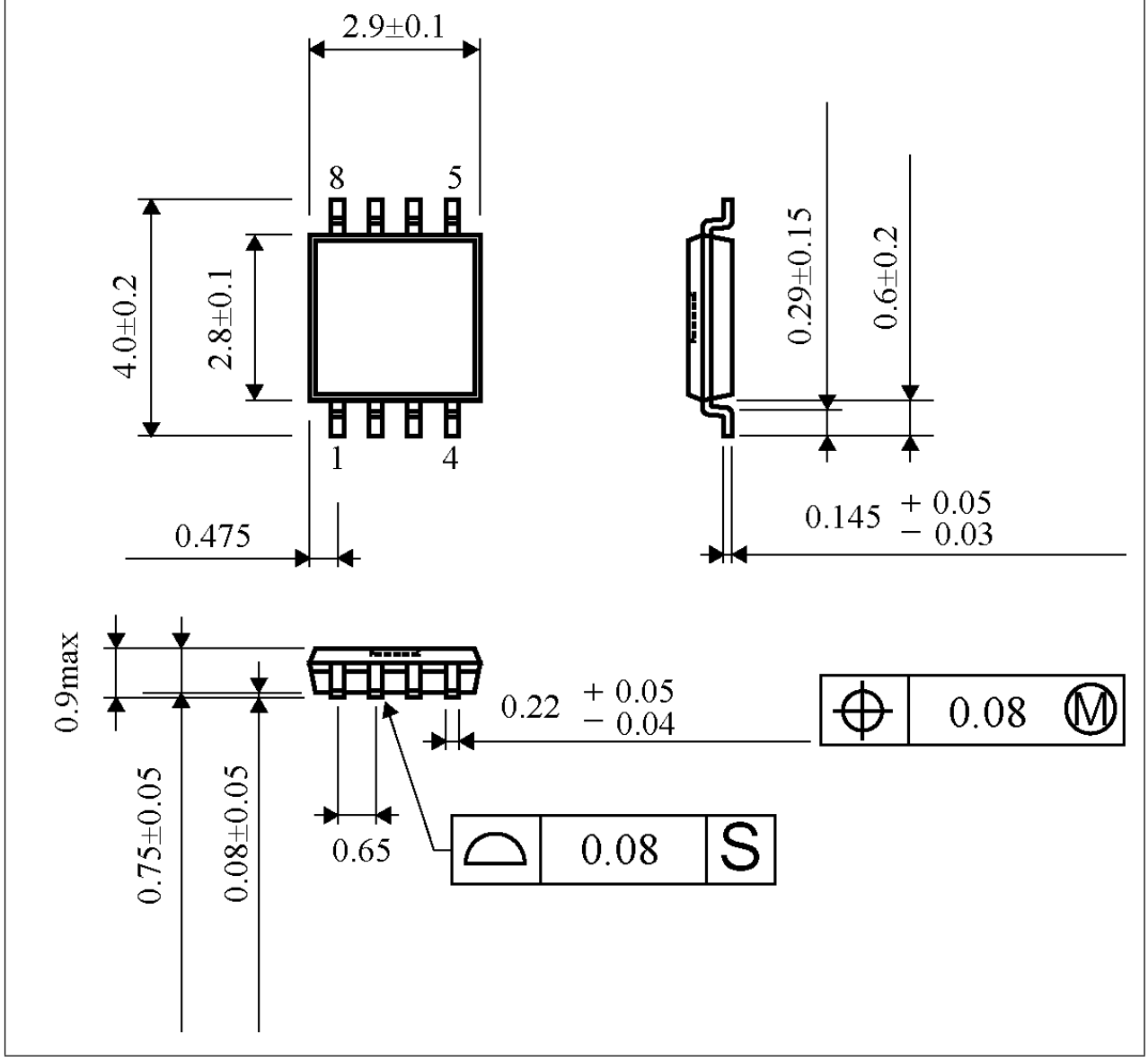

| | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 3.710 | 4.310 | 0.146 | 0.170 |
| A1 | 0.510 | | 0.020 | |
| A2 | 3.200 | 3.600 | 0.126 | 0.142 |
| B | 0.380 | 0.570 | 0.015 | 0.022 |
| B1 | 1.524(BSC) | | 0.060(BSC) | |
| C | 0.204 | 0.360 | 0.008 | 0.014 |
| D | 9.000 | 9.400 | 0.354 | 0.370 |
| E | 6.200 | 6.600 | 0.244 | 0.260 |
| E1 | 7.320 | 7.920 | 0.288 | 0.312 |
| e | 2.540(BSC) | | 0.100(BSC) | |
| L | 3.000 | 3.600 | 0.118 | 0.142 |
| E2 | 8.400 | 9.000 | 0.331 | 0.354 |

**SOP8** Unit: mm




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.350 | 1.800 | 0.053 | 0.071 |
| A1 | 0.050 | 0.250 | 0.004 | 0.010 |
| A2 | 1.250 | 1.550 | 0.053 | 0.061 |
| b | 0.330 | 0.510 | 0.013 | 0.020 |
| c | 0.170 | 0.250 | 0.006 | 0.010 |
| D | 4.780 | 5.000 | 0.185 | 0.197 |
| E | 3.800 | 4.000 | 0.150 | 0.157 |
| E1 | 5.800 | 6.300 | 0.228 | 0.244 |
| e | 1.270(BSC) | | 0.050(BSC) | |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |

**MSOP8** Unit: mm



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