

GX18B20H Programmable Resolution 1Wire Digital Thermometer

1.FEATURES

- 1-Wire Interface Requires Only One Port Pin for Communication
- Each chip has an independent 64-bit serial number
- Multidrop Capability Simplifies Distributed Temperature-Sensing Applications
- Requires No External Components
- Can be powered by the data line.
the supply voltage range is: 2.5V~5.5V
- Measuring Range: -55°C to +125°C (-67°F to +257°F)
- $\pm 0.1^{\circ}\text{C}$ Accuracy from 0°C to +50°
- Thermometer Resolution is User Selectable from 9 to 12 Bits
- Converts Temperature to 12-Bit Digital Word in 750ms (Max)
- User-Definable Nonvolatile (NV) Alarm Settings
- Alarm Search Command Identifies and Addresses Devices Whose Temperature is Outside Programmed Limits
- Available in MSOP8 and 3-Pin TO-92,Packages

2.Application Scenario

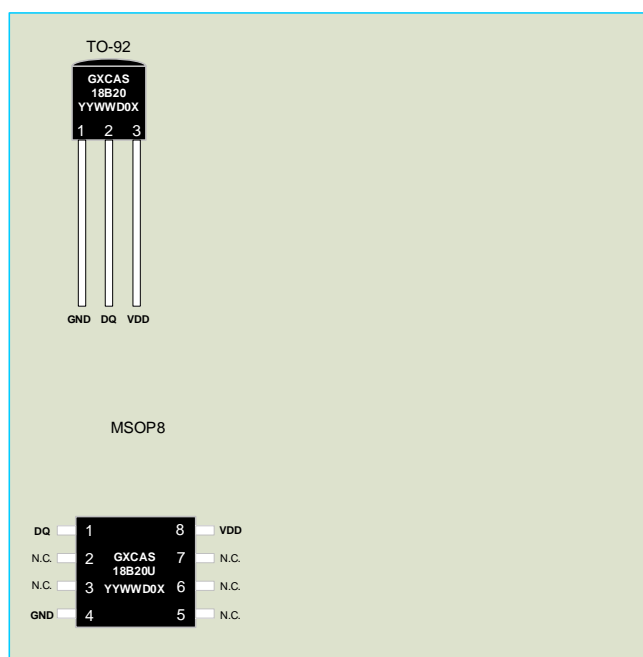
- temperature control
- industrial system
- consumer goods
- grain temperature measurement
- thermometer
- any thermal system

3.DESRIPTION

The GX18B20H digital thermometer provides 9-bit to 12-bit Celsius temperature measurements and has an alarm function with nonvolatile user- programmable upper and lower trigger points. The GX18B20H communicates over a 1-Wire bus that by definition requires only one data

line (and ground) for communication with a central microprocessor. It has an operating temperature range of -55° C to +125° C and is accurate to $\pm 0.1^{\circ}\text{C}$ over the range of 0° C to +50° C. In addition, the GX18B20H can derive power directly from the data line (“parasite power”), eliminating the need for an external power supply. Each GX18B20H has a unique 64-bit serial code, which allows multiple GX18B20Hs to function on the same 1-Wire bus. Thus, it is simple to use one microprocessor to control many GX18B20Hs distributed over a large area. Applications that can benefit from this feature include HVAC environmental controls, temperature monitoring systems inside buildings, equipment, or machinery, and process monitoring and control systems.

4.PIN CONFIGURATIONS



PIN CONFIGURATIONS

Pin location						Name	Function
MOSP8	TO-92						
2,3,5,6,7	—					N.C.	No Connection
8	3					VDD	Optional VDD. VDD must be grounded for operation in parasite power mode.
1	2					DQ	Data Input/Output. Open-drain 1-Wire interface pin. Also provides power to the device when used in parasite power mode (see the Powering the
4	1					GND	Ground

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5. Details

5.1 Overview

Figure 1 shows a block diagram of the GX18B20H, and pin descriptions are given in the Pin Description table. The 64-bit ROM stores the device's unique serial code. The scratchpad memory contains the 2-byte temperature register that stores the digital output from the temperature sensor. In addition, the scratchpad provides access to the 1-byte upper and lower alarm trigger registers (TH and TL) and the 1-byte configuration register. The configuration register allows the user to set the resolution of the temperature- to-digital conversion to 9, 10, 11, or 12 bits. And there are 2-byte user programmable EEPROM. The TH, TL, configuration registers, and 2-byte user programmable EEPROM are nonvolatile (EEPROM), so they will retain data when the device is powered down.

The GX18B20H uses 1-Wire bus protocol that implements bus communication using one control signal. The control line requires a weak pullup resistor since all devices are linked to the bus via a 3-state or opendrain port (the DQ pin in the case of the GX18B20H). In this bus system, the microprocessor (the master device) identifies and addresses devices on the bus using each device's unique 64-bit code. Because each device has a unique code, the number of devices that can be addressed on one bus is virtually unlimited. The 1-Wire bus protocol, including detailed explanations of the commands and "time slots," is covered in the 1-Wire Bus System section.

Another feature of the GX18B20H is the ability to operate without an external power supply. Power is instead supplied through the 1-Wire pullup resistor via the DQ pin when the bus is high. The high bus signal also charges an internal capacitor (CPP), which then supplies power to the device when the bus is low. This method of deriving power from the 1-Wire bus is referred to as "parasite power." As an alternative, the GX18B20H may also be powered by an external supply on VDD.

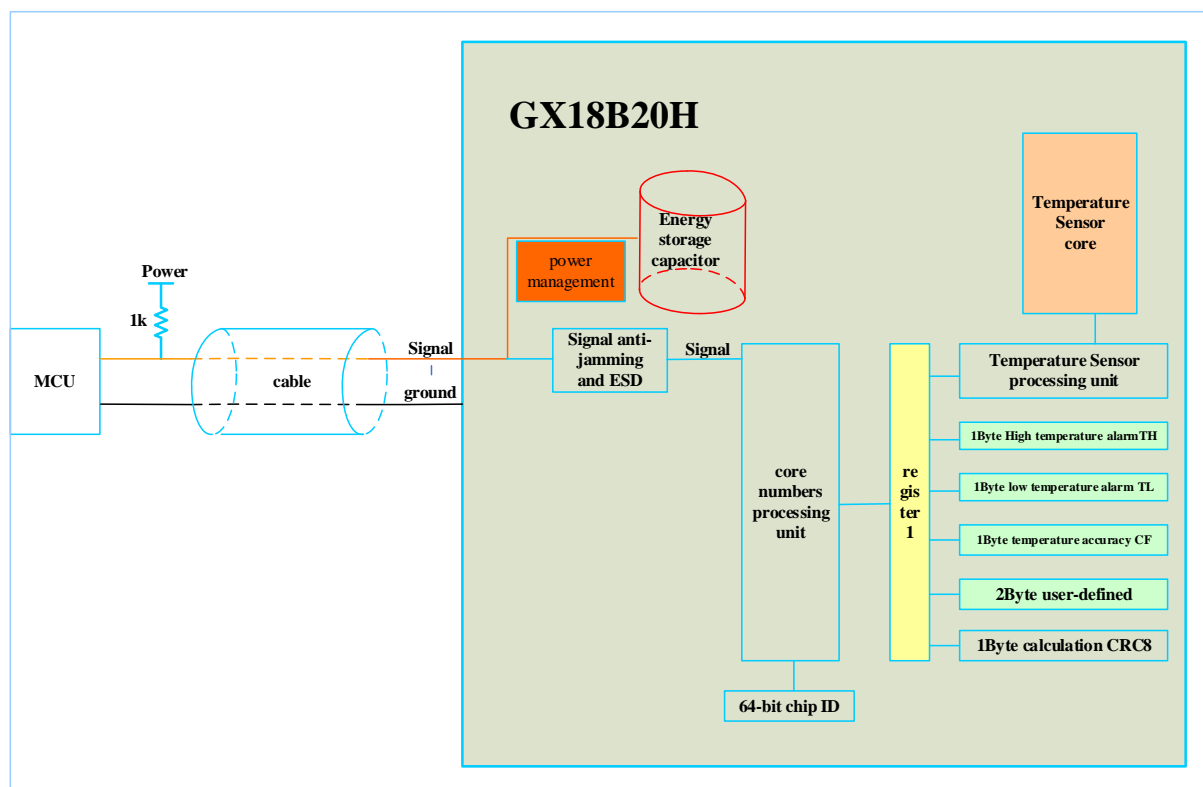


Figure 1. GX18B20H Block Diagram

5.2 Temperature measurement operation

The core functionality of the GX18B20H is its direct-to-digital temperature sensor. The resolution of the temperature sensor is user-configurable to 9, 10, 11, or 12 bits, corresponding to increments of 0.5°C, 0.25°C, 0.125°C, and 0.0625°C, respectively. The default resolution at power-up is 12-bit. The GX18B20H powers up in a low-power idle state. To initiate a temperature measurement and A-to-D conversion, the master must issue a Convert T [44h] command. Following the conversion, the resulting thermal data is stored in the 2-byte temperature register in the scratchpad memory and the GX18B20H returns to its idle state. If the GX18B20H is powered by an external supply, the master can issue “read time slots” (see the 1-Wire Bus System section) after the Convert T command and the GX18B20H will respond by transmitting 0 while the temperature conversion is in progress and 1 when the conversion is done. If the GX18B20H is powered with parasite power, this notification technique cannot be used since the bus must be pulled high by a strong pullup during the entire temperature conversion. The bus requirements for parasite power are explained in detail in the Powering the GX18B20H section.

The GX18B20H output temperature data is calibrated in degrees Celsius; for Fahrenheit applications, a lookup table or conversion routine must be used. The temperature data is stored as a 16-bit sign-extended two’s complement number in the temperature register (see Figure 2). The sign bits (S) indicate if the temperature is positive or negative: for positive numbers S

= 0 and for negative numbers S = 1. If the GX18B20H is configured for 12-bit resolution, all bits in the temperature register will contain valid data. For 11-bit resolution, bit 0 is undefined. For 10-bit resolution, bits 1 and 0 are undefined, and for 9-bit resolution bits 2, 1, and 0 are undefined. Table 1 gives examples of digital output data and the corresponding temperature reading for 12-bit resolution conversions.

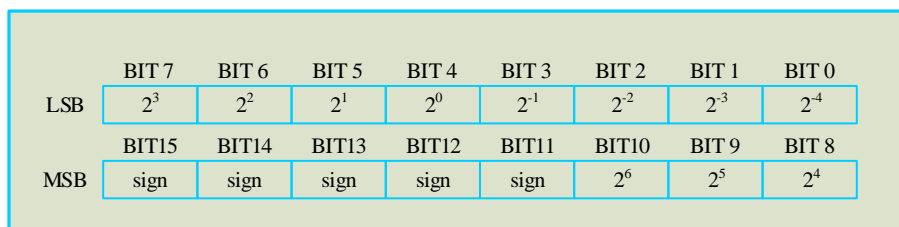


Figure 2. Temperature Register Format

Table 1. Temperature/Data Relationship

Temperature (°C)	Digital output (Binary)	Digital output (Hexadecimal)
+125	0000 0111 1101 0000	07D0h
+85	0000 0101 0101 0000	0550h
+25.0625	0000 0001 1001 0001	0191h
+10.125	0000 0000 1010 0010	00A2h
+0.5	0000 0000 0000 1000	0008h
0	0000 0000 0000 0000	0000h
-0.5	1111 1111 1111 1000	FFF8h
-10.125	1111 1111 0101 1110	FF5Eh
-25.0625	1111 1110 0110 1111	FE6Fh
-55	1111 1100 1001 0000	FC90h

*The power-on reset value of the temperature register is +85° C.

5.3 Alarm operation

After the GX18B20H performs a temperature conversion, the temperature value is compared to the user- defined two's complement alarm trigger values stored in the 1-byte TH and TL registers (see Figure 3). The sign bit (S) indicates if the value is positive or negative: for positive numbers S = 0 and for negative numbers S = 1. The TH and TL registers are nonvolatile (EEPROM) so they will retain data when the device is powered down. TH and TL can be accessed through bytes 2 and 3 of the scratchpad as explained in the Memory section.

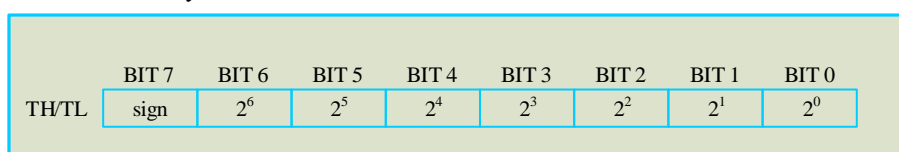


Figure 3. TH and TL Register Format

Only bits 11 through 4 of the temperature register are used in the TH and TL comparison since TH and TL are 8-bit registers. If the measured temperature is lower than or equal to TL or higher than or equal to TH, an alarm condition exists and an alarm flag is set inside the GX18B20H. This flag is updated after every temperature measurement; therefore, if the alarm condition goes away, the flag will be turned off after the next temperature conversion.

The master device can check the alarm flag status of all GX18B20Hs on the bus by issuing an Alarm Search [ECh] command. Any GX18B20Hs with a set alarm flag will respond to the command, so the master can determine exactly which GX18B20Hs have experienced an alarm condition. If an alarm condition exists and the TH or TL settings have changed, another temperature conversion should be done to validate the alarm condition.

5.4 Power supply of GX18B20H

The GX18B20H can be powered by an external supply on the VDD pin, or it can operate in “parasite power” mode, which allows the GX18B20H to function without a local external supply. Parasite power is very useful for applications that require remote temperature sensing or that are very space constrained. Figure 1 shows the GX18B20H’s parasite-power control circuitry, which “steals” power from the 1-Wire bus via the DQ pin when the bus is high. The stolen charge powers the GX18B20H while the bus is high, and some of the charge is stored on the parasite power capacitor (CPP) to provide power when the bus is low. When the GX18B20H is used in parasite power mode, the VDD pin must be connected to ground.

In parasite power mode, the 1-Wire bus and CPP can provide sufficient current to the GX18B20H for most operations as long as the specified timing and voltage requirements are met (see the DC Electrical Characteristics and AC Electrical Characteristics). However, when the GX18B20H is performing temperature conversions or copying data from the scratchpad memory to EEPROM, the operating current can be as high as 1.5mA. This current can cause an unacceptable voltage drop across the weak 1-Wire pullup resistor and is more current than can be supplied by CPP. To assure that the GX18B20H has sufficient supply current, it is necessary to provide a strong pullup on the 1-Wire bus whenever temperature conversions are taking place or data is being copied from the scratchpad to EEPROM. This can be accomplished by using a MOSFET to pull the bus directly to the rail as shown in Figure 4. The 1-Wire bus must be switched to the strong pullup within 10 μ s (max) after a Convert T [44h] or Copy Scratchpad [48h] command is issued, and the bus must be held high by the pullup for the duration of the conversion (t_{conv}) or data transfer (t_{wr} = 10ms). No other activity can take place on the 1-Wire bus while the pullup is enabled.

The GX18B20H can also be powered by the conventional method of connecting an external power supply to the VDD pin, as shown in Figure 5. The advantage of this method is that the MOSFET pullup is not required, and the 1-Wire bus is free to carry other traffic during the temperature conversion time.

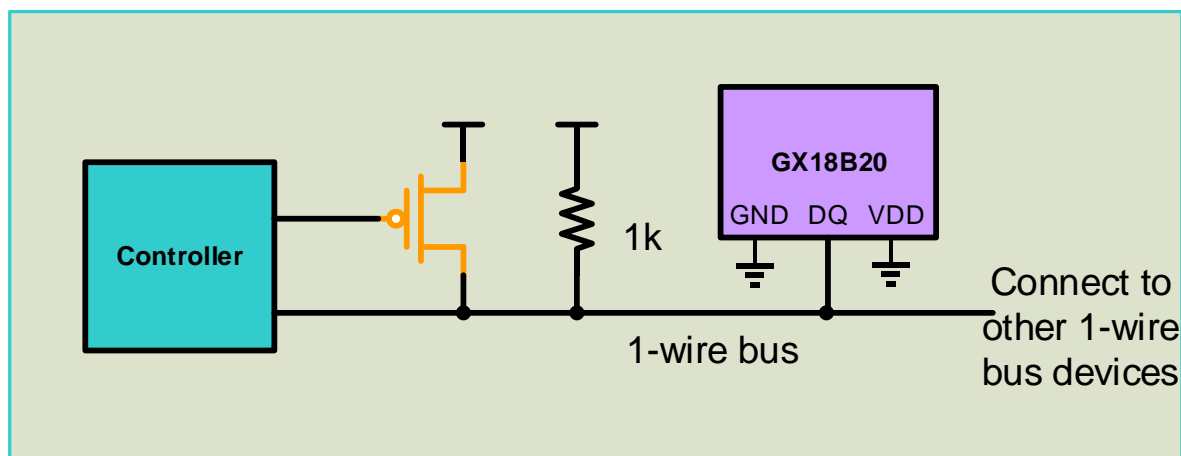


Figure 4. Supplying the Parasite-Powered GX18B20H During Temperature Conversions

The use of parasite power is not recommended for temperatures above +100°C since the GX18B20H may not be able to sustain communications due to the higher leakage currents that can exist at these temperatures. For applications in which such temperatures are likely, it is strongly recommended that the GX18B20H be powered by an external power supply.

In some situations the bus master may not know whether the GX18B20Hs on the bus are parasite powered or powered by external supplies. The master needs this information to determine if the strong bus pullup should be used during temperature conversions. To get this information, the master can issue a Skip ROM [CCh] command followed by a Read Power Supply [B4h] command followed by a “read time slot”. During the read time slot, parasite powered GX18B20Hs will pull the bus low, and externally powered GX18B20Hs will let the bus remain high. If the bus is pulled low, the master knows that it must supply the strong pullup on the 1-Wire bus during temperature conversions.

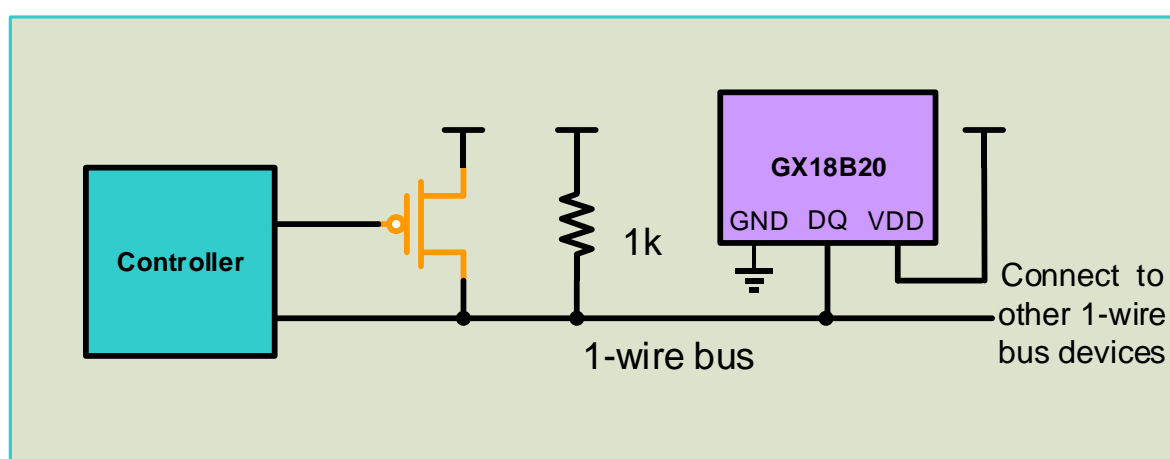


Figure 5. Powering the GX18B20H with an External Supply

6. Memory

6.1 64-bit ROM

Each GX18B20H contains a unique 64-bit code (see Figure 6) stored in ROM. The least significant 8 bits of the ROM code contain the GX18B20H's 1-Wire family code: 28h. The next 48 bits contain a unique serial number. The most significant 8 bits contain a cyclic redundancy check (CRC) byte that is calculated from the first 56 bits of the ROM code. A detailed explanation of the CRC bits is provided in the CRC Generation section. The 64-bit ROM code and associated ROM function control logic allow the GX18B20H to operate as a 1-Wire device using the protocol detailed in the 1-Wire Bus System section.

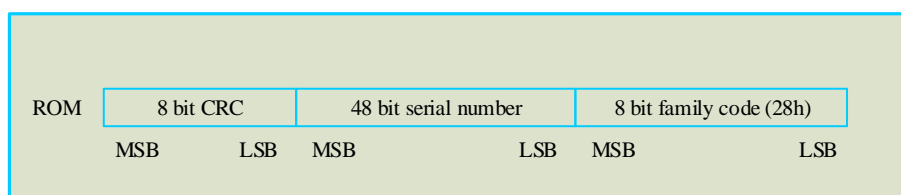


Figure 6. 64-Bit Lasered ROM Code

6.2 Memory unit

The GX18B20H's memory is organized as shown in Figure 7. The memory consists of an SRAM scratchpad with nonvolatile EEPROM storage for the high and low alarm trigger registers (TH and TL), configuration register, and 2-byte user programmable EEPROM. Note that if the GX18B20H alarm function is not used, the TH and TL registers can serve as general-purpose memory. All memory commands are described in detail in the GX18B20H Function Commands section.

Byte 0 and byte 1 of the scratchpad contain the LSB and the MSB of the temperature register, respectively. These bytes are read-only. Bytes 2 and 3 provide access to TH and TL registers. Byte 4 contains the configuration register data, which is explained in detail in the Configuration Register section. Byte 5 is reserved for internal use by the device and cannot be overwritten. Bytes 6, and 7 are for User. Byte 8 of the scratchpad is read-only and contains the CRC code for bytes 0 through 7 of the scratchpad. The GX18B20H generates this CRC using the method described in the CRC Generation section. Data is written to bytes 2, 3, 4, 6, and 7 of the scratchpad using the Write Scratchpad [4Eh] command; the data must be transmitted to the GX18B20H starting with the least significant bit of byte 2. To verify data integrity, the scratchpad can be read (using the Read Scratchpad [BEh] command) after the data is written. When reading the scratchpad, data is transferred over the 1-Wire bus starting with the least significant bit of byte 0. To transfer the TH, TL and configuration data from the scratchpad to EEPROM, the master must issue the Copy Scratchpad [48h] command. Data in the EEPROM registers is retained when the device is powered down; at power-up the EEPROM data is reloaded into the corresponding scratchpad locations. Data can also be reloaded from EEPROM to the scratchpad at any time using the Recall E2 [B8h] command. The master can issue read time slots following the Recall E2 command and the GX18B20H will indicate the status of the recall by transmitting 0 while

the recall is in progress and 1 when the recall is done.

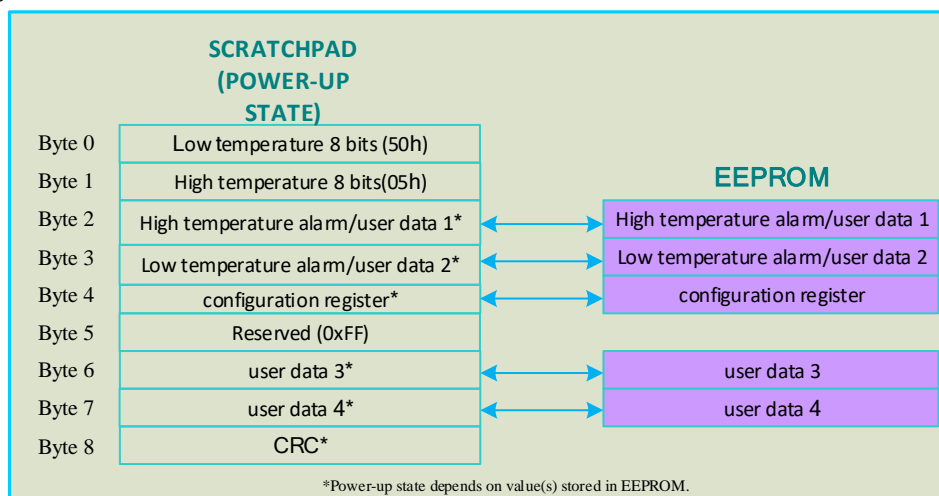


Figure 7. GX18B20H Memory Map

6.3 CONFIGURATION REGISTER

Byte 4 of the scratchpad memory contains the configuration register, which is organized as illustrated in Figure 8. The user can set the conversion resolution of the GX18B20H using the R0 and R1 bits in this register as shown in Table 2. The power-up default of these bits is R0 = 1 and R1 = 1 (12-bit resolution). Note that there is a direct tradeoff between resolution and conversion time. Bit 7 and bits 0 to 4 in the configuration register are reserved for internal use by the device and cannot be overwritten.

Figure 8. Configuration Register

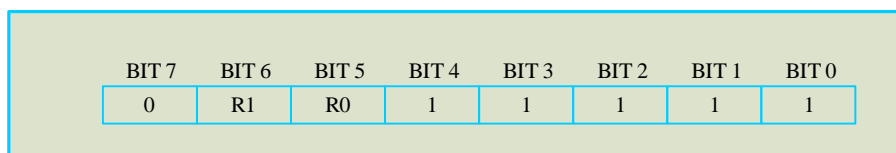


Table 2. Thermometer Resolution Configuration

R1	R0	Resolution (BITS)	Maximum conversion time	
0	0	9	93.75ms	(t _{CONV} /8)
0	1	10	187.5ms	(t _{CONV} /4)
1	0	11	375ms	(t _{CONV} /2)
1	1	12	750ms	(t _{CONV})

7. CRC generator

CRC bytes are provided as part of the GX18B20H's 64-bit ROM code and in the 9th byte of the scratchpad memory. The ROM code CRC is calculated from the first 56 bits of the ROM code and is contained in the most significant byte of the ROM. The

$$\text{CRC} = X^8 + X^5 + X^4 + 1$$

The diagram illustrates the CRC8 calculation process. It shows a sequence of data bytes (MSB to LSB) being processed by a series of XOR operations. The final result is the CRC8 value.

Figure 9. CRC Generator

8. 1-wire bus system

All data and commands are transmitted least significant bit first over the 1-Wire bus. The following discussion of the 1-Wire bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing).

9. hardware structure

The 1-Wire bus has by definition only a single data line. Each device (master or slave) interfaces to the data line via an open-drain or 3-state port. This allows each device to “release” the data line when the device is not transmitting data so the bus

is available for use by another device. The 1-Wire port of the GX18B20H (the DQ pin) is open drain with an internal circuit equivalent to that shown in Figure 10.

The 1-Wire bus requires an external pullup resistor of approximately $1k\Omega$; thus, the idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus **MUST** be left in the idle state if the transaction is to resume. Infinite recovery time can occur between bits so long as the 1-Wire bus is in the inactive (high) state during the recovery period. If the bus is held low for more than $480\mu s$, all components on the bus will be reset.

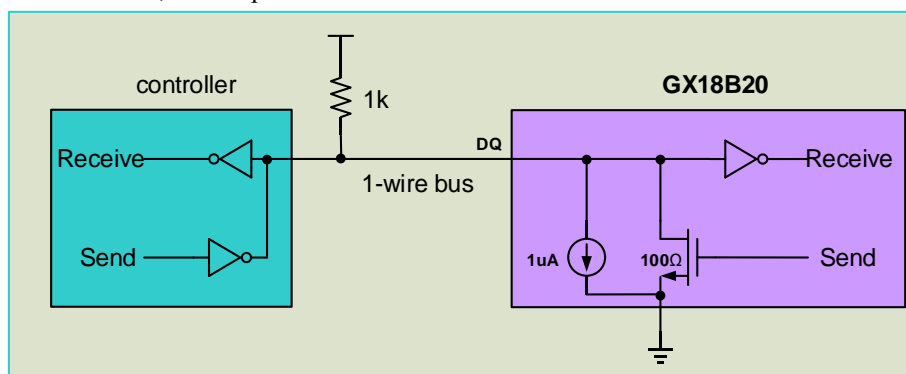


Figure 10. Hardware Configuration

10. execution sequence

The transaction sequence for accessing the GX18B20H is as follows:

- Step 1. Initialization
- Step 2. ROM Command (followed by any required data exchange)
- Step 3. GX18B20H Function Command (followed by any required data exchange)

It is very important to follow this sequence every time the GX18B20H is accessed, as the GX18B20H will not respond if any steps in the sequence are missing or out of order. Exceptions to this rule are the Search ROM and Alarm Search commands. After issuing either of these ROM commands, the master must return to Step 1 in the sequence.

10.1 initialization

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that slave devices (such as the GX18B20H) are on the bus and are ready to operate. Timing for the reset and presence pulses is detailed in the 1-Wire Signaling section.

10.2 ROM instruction

After the bus master has detected a presence pulse, it can issue a ROM command. These commands operate on the unique 64-bit ROM codes of each slave device and allow the master to single out a specific device if many are present on the 1-Wire bus. These commands also allow the master to determine how many and what types of devices are present on the bus or if any

device has experienced an alarm condition. There are five ROM commands, and each command is 8 bits long. The master device must issue an appropriate ROM command before issuing a GX18B20H function command. A flowchart for operation of the ROM commands is shown in Figure 11.

SEARCH ROM [F0h]

When a system is initially powered up, the master must identify the ROM codes of all slave devices on the bus, which allows the master to determine the number of slaves and their device types. The master learns the ROM codes through a process of elimination that requires the master to perform a Search ROM cycle (i.e., Search ROM command followed by data exchange) as many times as necessary to identify all of the slave devices. If there is only one slave on the bus, the simpler Read ROM command (see below) can be used in place of the Search ROM process. After every Search ROM cycle, the bus master must return to Step 1 (Initialization) in the transaction sequence.

READ ROM [33h]

This command can only be used when there is one slave on the bus. It allows the bus master to read the slave's 64-bit ROM code without using the Search ROM procedure. If this command is used when there is more than one slave present on the bus, a data collision will occur when all the slaves attempt to respond at the same time.

MATCH ROM [55h]

The match ROM command followed by a 64-bit ROM code sequence allows the bus master to address a specific slave device on a multidrop or single-drop bus. Only the slave that exactly matches the 64-bit ROM code sequence will respond to the function command issued by the master; all other slaves on the bus will wait for a reset pulse.

SKIP ROM [CCh]

The master can use this command to address all devices on the bus simultaneously without sending out any ROM code information. For example, the master can make all GX18B20Hs on the bus perform simultaneous temperature conversions by issuing a Skip ROM command followed by a Convert T [44h] command. Note that the Read Scratchpad [BEh] command can follow the Skip ROM command only if there is a single slave device on the bus. In this case, time is saved by allowing the master to read from the slave without sending the device's 64-bit ROM code. A Skip ROM command followed by a Read Scratchpad command will cause a data collision on the bus if there is more than one slave since multiple devices will attempt to transmit data simultaneously.

ALARM SEARCH [ECh]

The operation of this command is identical to the operation of the Search ROM command except that only slaves with a set alarm flag will respond. This command allows the master device to determine if any GX18B20Hs experienced an alarm condition during the most recent temperature conversion. After every Alarm Search cycle (i.e., Alarm Search command followed by data exchange), the bus master must return to Step 1 (Initialization) in the transaction sequence. See the Operation—Alarm Signaling section for an explanation of alarm flag operation.

10.3 GX18B20H function instruction

After the bus master has used a ROM command to address the GX18B20H with which it wishes to communicate, the master can issue one of the GX18B20H function commands. These commands allow the master to write to and read from the GX18B20H's scratchpad memory, initiate temperature conversions and determine the power supply mode. The GX18B20H function commands, which are described below, are summarized in Table 3 and illustrated by the flowchart in Figure 12.

CONVERT T [44h]

This command initiates a single temperature conversion. Following the conversion, the resulting thermal data is stored in the 2-byte temperature register in the scratchpad memory and the GX18B20H returns to its low-power idle state. If the device is being used in parasite power mode, within 10 μ s (max) after this command is issued the master must enable a strong pullup on the 1-Wire bus for the duration of the conversion (tCONV) as described in the Powering the GX18B20H section. If the GX18B20H is powered by an external supply, the master can issue read time slots after the Convert T command and the GX18B20H will respond by transmitting a 0 while the temperature conversion is in progress and a 1 when the conversion is done. In parasite power mode this notification technique cannot be used since the bus is pulled high by the strong pullup during the conversion.

WRITE SCRATCHPAD [4Eh]

This command allows the master to write at most 5 bytes of data to the GX18B20H's scratchpad. The first data byte is written into the TH register (byte 2 of the scratchpad), the second byte is written into the TL register (byte 3), the third byte is written into the configuration register (byte 4), and the last two bytes are written into the User Bytes 3 and 4. Data must be transmitted least significant bit first. All 5 bytes MUST be written before the master issues a reset, or the data may be corrupted.

READ SCRATCHPAD [BEh]

This command allows the master to read the contents of the scratchpad. The data transfer starts with the least significant bit of byte 0 and continues through the scratchpad until the 9th byte (byte 8 – CRC) is read. The master may issue a reset to terminate reading at any time if only part of the scratchpad data is needed.

COPY SCRATCHPAD [48h]

This command copies the contents of the scratchpad TH, TL, configuration registers and User Bytes 3 and 4 (bytes 2, 3, 4, 6 and 7) to EEPROM. If the device is being used in parasite power mode, within 10 μ s (max) after this command is issued the master must enable a strong pullup on the 1-Wire bus for at least 10ms as described in the Powering the GX18B20H section.

RECALL E2 [B8h]

This command recalls the alarm trigger values (TH and TL), configuration data and User Byte 4 and 5 from EEPROM and places the data in bytes 2, 3, 4, 6 and 7, respectively, in the scratchpad memory. The master device can issue read time slots following the Recall E2 command and the GX18B20H will indicate the status of the recall by transmitting 0 while the recall is in progress and 1 when the recall is done. The recall operation happens automatically at power-up, so valid data is available in the scratchpad as soon as power is applied to the device.

READ POWER SUPPLY [B4h]

The master device issues this command followed by a read time slot to determine if any GX18B20Hs on the bus are using parasite power. During the read time slot, parasite powered GX18B20Hs will pull the bus low, and externally powered GX18B20Hs will let the bus remain high. See the Powering the GX18B20H section for usage information for this command.

Table 3. GX18B20H Function Command Set

COMMAND	DESCRIPTION	PROTOCOL	1-Wire BUS ACTIVITY AFTER COMMAND IS ISSUED	NOTES
TEMPERATURE CONVERSION COMMANDS				
Convert T	Initiates temperature conversion	44h	GX18B20H transmits conversion status to master (not applicable for parasite- powered GX18B20H).	1
MEMORY COMMANDS				
Read Scratchpad	Reads the entire scratchpad including the CRC byte.	BEh	GX18B20H transmits up to 9 data bytes to master.	2
Write Scratchpad	Writes data into scratchpad bytes 2, 3, 4, and 6, 7 (T _H , T _L , configuration registers and User Bytes).	4Eh	Master transmits 3 or 4 or 5 data bytes to GX18B20H.	3
Copy Scratchpad	Copies T _H , T _L , config register and User Bytes data from the scratchpad	48h	None	1
Recall E ²	Recalls T _H , T _L , config register and User Bytes data from EEPROM to the	B8h	GX18B20H transmits recall status to master.	
Read Power Supply	Signals GX18B20H power supply mode to the	B4h	GX18B20H transmits supply status to master.	

Note1:For parasite-powered GX18B20Hs, the master must enable a strong pullup on the 1-Wire bus during temperature conversions and copies from the scratchpad to EEPROM. No other bus activity may take place during this time.

Note2:The master can interrupt the transmission of data at any time by issuing a reset.

Note3:The TH, TL and CR must be written before the start of reset signal.

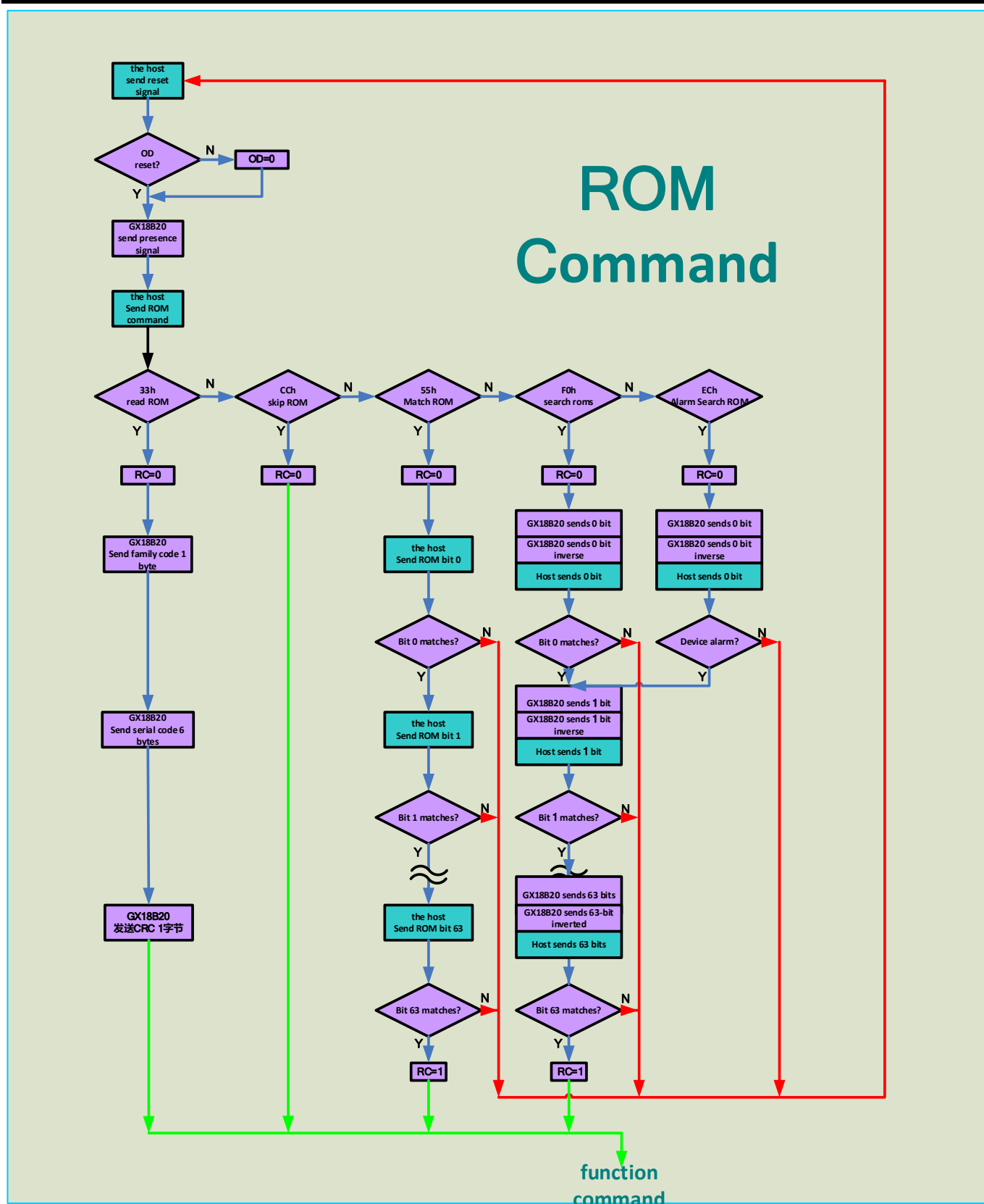


Figure 11. ROM Instruction Flowchart

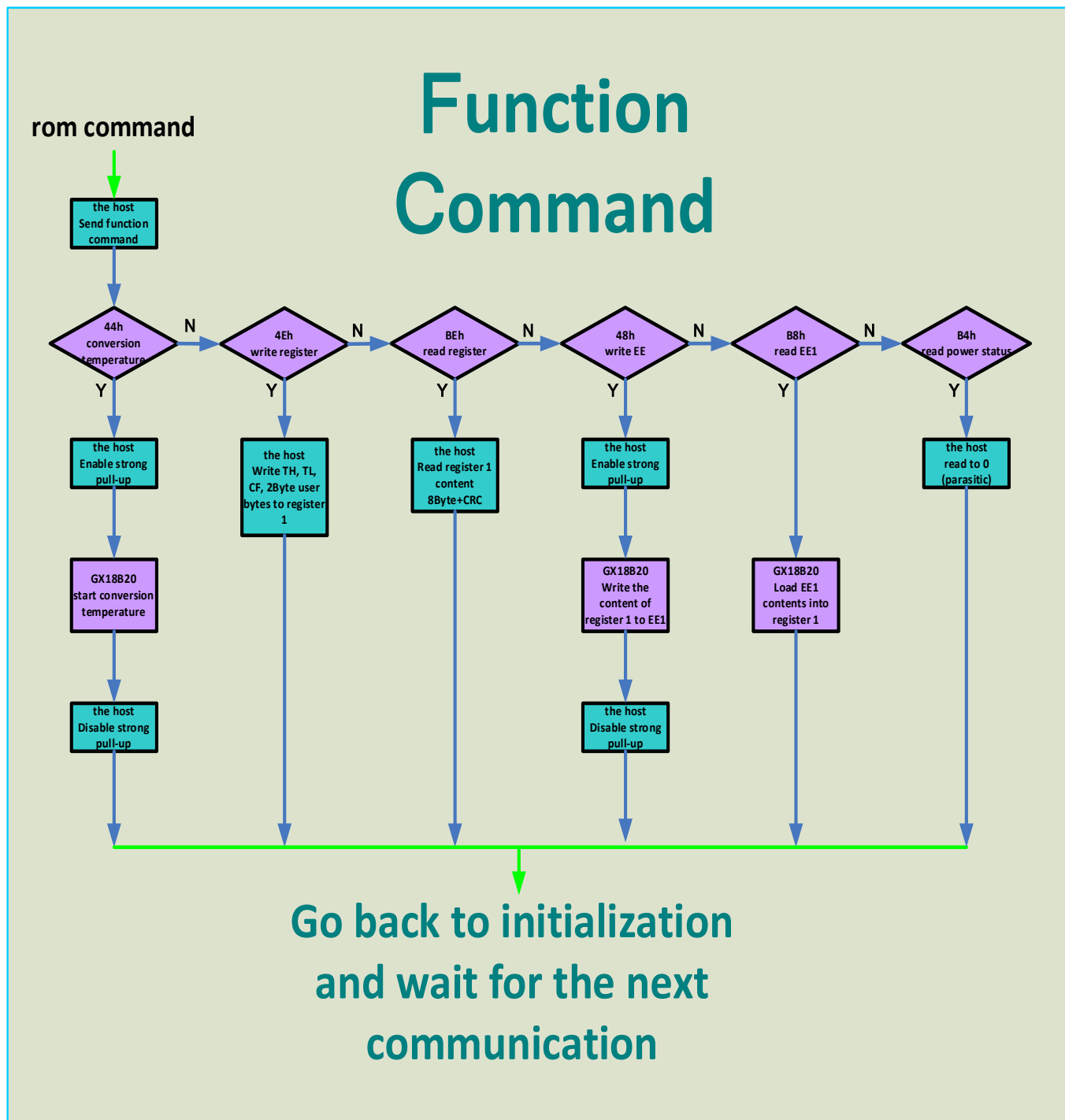


Figure 12. GX18B20H function instruction flowchart

11. 1-wire bus signal

The GX18B20H uses a strict 1-Wire communication protocol to ensure data integrity. Several signal types are defined by this protocol: reset pulse, presence pulse, write 0, write 1, read 0, and read 1. The bus master initiates all these signals, with the exception of the presence pulse.

11.1 RESET SEQUENCE: RESET AND PRESENCE PULSE

All communication with the GX18B20H begins with an initialization sequence that consists of a reset pulse from the master followed by a presence pulse from the GX18B20H. This is illustrated in Figure 13. When the GX18B20H sends the presence pulse in response to the reset, it is indicating to the master that it is on the bus and ready to operate.

During the initialization sequence the bus master transmits (TX) the reset pulse by pulling the 1-Wire bus low for a minimum of 480 μ s. The bus master then releases the bus and goes into receive mode (RX). When the bus is released, the 1k pullup resistor pulls the 1-Wire bus high. When the GX18B20H detects this rising edge, it waits 15 μ s to 60 μ s and then transmits a presence pulse by pulling the 1-Wire bus low for 60 μ s to 240 μ s.

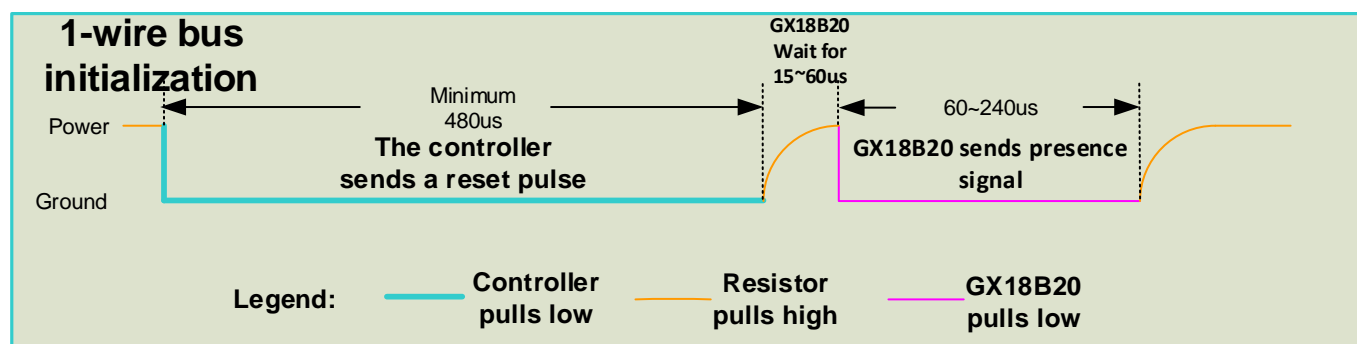


Figure 13. Initialization Timing

11.2 Read/Write Timing

The bus master writes data to the GX18B20H during write time slots and reads data from the GX18B20H during read time slots. One bit of data is transmitted over the 1-Wire bus per time slot.

WRITE TIME SLOTS

There are two types of write time slots: “Write 1” time slots and “Write 0” time slots. The bus master uses a Write 1 time slot to write a logic 1 to the GX18B20H and a Write 0 time slot to write a logic 0 to the GX18B20H. All write time slots must be a minimum of 60 μ s in duration with a minimum of a 1 μ s recovery time between individual write slots. Both types of write time slots are initiated by the master pulling the 1-Wire bus low (see Figure 14).

To generate a Write 1 time slot, after pulling the 1-Wire bus low, the bus master must release the 1-Wire bus within 15 μ s. When the bus is released, the 1k pullup resistor will pull the bus high. To generate a Write 0 time slot, after pulling the 1-Wire bus low, the bus master must continue to hold the bus low for the duration of the time slot (at least 60 μ s).

The GX18B20H samples the 1-Wire bus during a window that lasts from 15 μ s to 60 μ s after the master initiates the write time slot. If the bus is high during the sampling window, a 1 is written to the GX18B20H. If the line is low, a 0 is written to the GX18B20H.

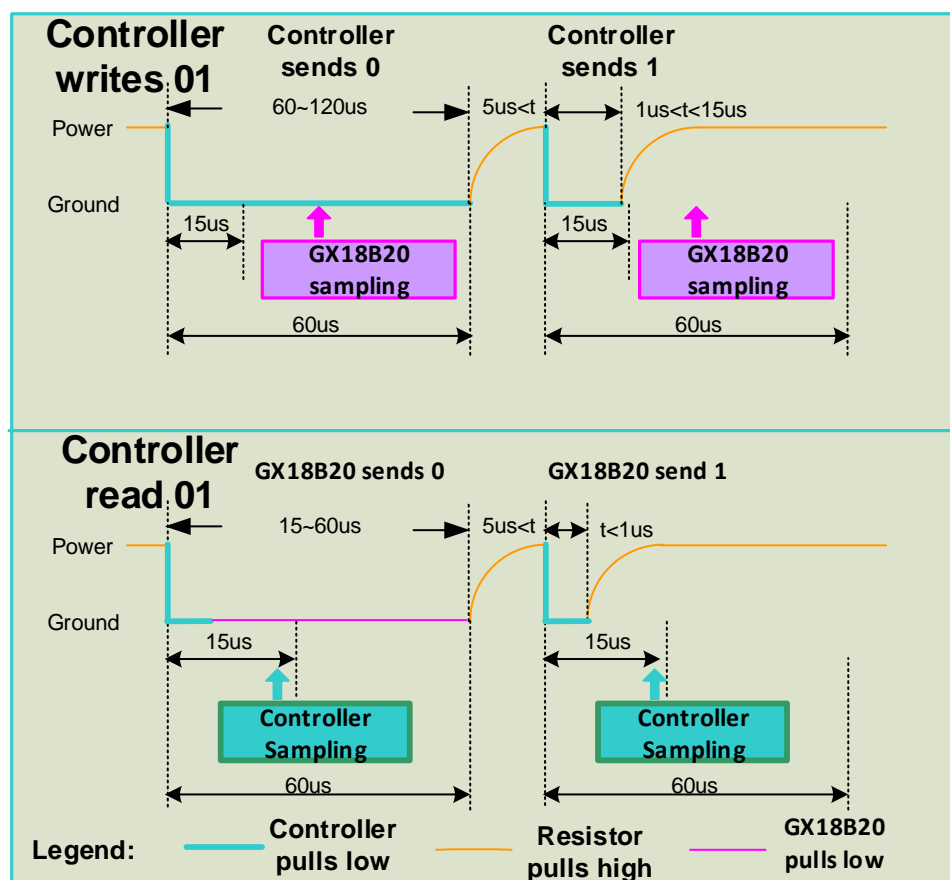


Figure 14. Read/Write Time Slot Timing Diagram

READ TIME SLOTS

The GX18B20H can only transmit data to the master when the master issues read time slots. Therefore, the master must generate read time slots immediately after issuing a Read Scratchpad [BEh] or Read Power Supply [B4h] command, so that the GX18B20H can provide the requested data. In addition, the master can generate read time slots after issuing Convert T [44h] or Recall E2 [B8h] commands to find out the status of the operation as explained in the GX18B20H Function Commands section.

All read time slots must be a minimum of 60μs in duration with a minimum of a 1μs recovery time between slots. A read time slot is initiated by the master device pulling the 1-Wire bus low for a minimum of 1μs and then releasing the bus (see Figure 14). After the master initiates the read time slot, the GX18B20H will begin transmitting a 1 or 0 on bus. The GX18B20H transmits a 1 by leaving the bus high and transmits a 0 by pulling the bus low. When transmitting a 0, the GX18B20H will release the bus by the end of the time slot, and the bus will be pulled back to its high idle state by the pullup resistor. Output data from the GX18B20H is valid for 15μs after the falling edge that initiated the read time slot. Therefore, the master must release the bus and then sample the bus state within 15μs from the start of the period.

Figure 15 illustrates that the sum of TINIT, TRC, and TSAMPLE must be less than 15μs for a read time slot. Figure 16 shows that system timing margin is maximized by keeping TINIT and TRC as short as possible and by locating the master sample time during read time slots towards the end of the 15μs period.

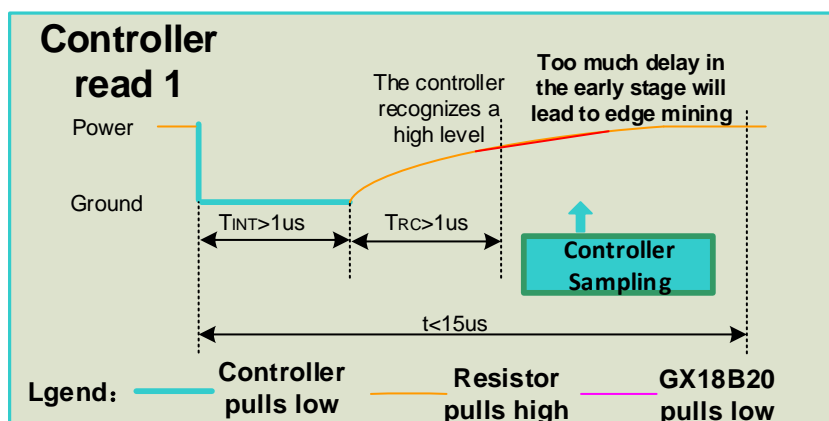


Figure 15. Detailed Master Read 1 Timing

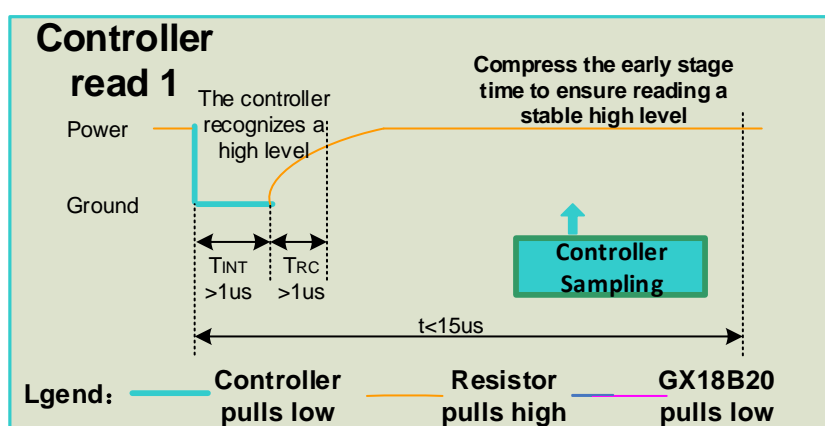


Figure 16. Recommended Master Read 1 Timing

12. GX18B20H operation example

12.1 Example 1

In this example there are multiple GX18B20Hs on the bus and they are using parasite power. The bus master initiates a temperature conversion in a specific GX18B20H and then reads its scratchpad and recalculates the CRC to verify the data.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
Tx	Reset	Master issues reset pulse.
Rx	Presence	GX18B20Hs respond with presence pulse.
Tx	55h	Master issues Match ROM command.
Tx	64-bit ROM code	Master sends GX18B20H ROM code.
Tx	44h	Master issues Convert T command
Tx	DQ line held high by strong pullup	Master applies strong pullup to DQ for the duration of the conversion (t_{conv})
Tx	Reset	Master issues reset pulse.

Rx	Presence	GX18B20H respond with presence pulse.
Tx	55h	Master issues Match ROM command.
Tx	64-bit ROM code	Master sends GX18B20H ROM code.
Tx	BEh	The main control issues a read register command
Rx	9 data bytes	Master reads entire scratchpad including CRC. The master then recalculates the CRC of the first eight data bytes from the scratchpad and compares the calculated CRC with the read CRC. If they match, the master continues; if not, the read operation is repeated.

12.1 Example 2

In this example there is only one GX18B20H on the bus and it is using parasite power. The master writes to the TH, TL, and configuration registers in the GX18B20H scratchpad and then reads the scratchpad and recalculates the CRC to verify the data. The master then copies the scratchpad contents to EEPROM.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
Tx	Reset	Master issues reset pulse.
Rx	Presence	GX18B20H responds with presence pulse.
Tx	CCh	Master issues Skip ROM command.
Tx	4Eh	Master issues Write Scratchpad command.
Tx	3 data bytes	Master sends three data bytes to scratchpad (TH, TL, CR).
Tx	Reset	Master issues reset pulse.
Rx	Presence	GX18B20H responds with presence pulse
Tx	CCh	Master issues Skip ROM command.
Tx	BEh	Master issues Read Scratchpad command.
Rx	9 data bytes	Master reads entire scratchpad including CRC. The master then recalculates the CRC of the first eight data bytes from the scratchpad and compares the calculated CRC with the read CRC. If they match, the master continues; if not, the read operation is repeated.
Tx	Reset	Master issues reset pulse.
Rx	Presence	GX18B20H responds with presence pulse
Tx	CCh	Master issues Skip ROM command.
Tx	48h	Master issues Copy Scratchpad command.
Tx	DQ line held high by strong pullup	Master applies strong pullup to DQ for at least 10ms while copy operation is in progress.

13. Extreme conditions of use

Voltage Range on Any Pin Relative to Ground-0.5V to +6.0V

Operating Temperature Range..... -55°C to +125°C

Storage Temperature Range -55°C to +125°C

Solder TemperatureRefer to the J-STD-020 Specification.

These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

14. DC characteristics

(-55°C to +125°C; $V_{DD}=2.5V$ to $5.5V$)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTES
supply voltage	V_{DD}	local power	+2.5		+5.5	V	1
Pull up supply voltage	V_{PU}	parasitic power	+2.5		+5.5	V	1,2
		local power	+2.5		V_{DD}		
temperature error	t_{ERR}	0°C~+50°C			±0.1	°C	3
		-55°C~+125°C			±1.0		
input logic low	V_{IL}		-0.3		+0.8	V	1,4,5
input logic high	V_{IH}	local power	+2.2		The lower of 5.5 or $V_{DD}+0.3$	V	1,6
		parasitic power	+2.5				
Sink current	I_L	$V_{IO} = 0.4V$	4.0			mA	1
stand-by current	I_{DDs}			750	1000	nA	7,8
Working current	I_{DD}	$V_{DD} = 5V$		1	1.5	mA	9
DQ input current	I_{DQ}			5		μA	10
Drift				±0.1		°C	11

NOTES:

- 1) All voltages are referenced to ground.
- 2) The Pullup Supply Voltage specification assumes that the pullup device is ideal, and therefore the high level of the pullup is equal to V_{PU} . In order to meet the V_{IH} spec of the GX18B20H, the actual supply rail for the strong pullup transistor must include margin for the voltage drop across the transistor when it is turned on; thus: $V_{PU_ACTUAL} = V_{PU_IDEAL} + V_{TRANSISTOR}$.
- 3) See typical performance curve in Figure 17.

- 4) Logic-low voltages are specified at a sink current of 4mA.
- 5) To guarantee a presence pulse under low voltage parasite power conditions, VILMAX may have to be reduced to as low as 0.5V.
- 6) Logic-high voltages are specified at a source current of 1mA.
- 7) Standby current specified up to +70°C. Standby current typically is 3μA at +125°C.
- 8) To minimize IDDS, DQ should be within the following ranges: $GND \leq DQ \leq GND + 0.3V$ or $VDD - 0.3V \leq DQ \leq VDD$.
- 9) Active current refers to supply current during active temperature conversions or EEPROM writes.
- 10) DQ line is high ("high-Z" state).
- 11) Drift data is based on a 1000-hour stress test at +125°C with VDD = 5.5V.

15. AC characteristics

(-55°C to +125°C; V_{DD} = 2.5V to 5.5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
NV Write Cycle Time	t _{WR}			8	12	ms
EEPROM Writes	N _{EEWR}	-55°C to +125°C	1000			writes
EEPROM Data Retention	t _{EDR}	-55°C to +125°C	10			years

(-55°C to +125°C; V_{DD} = 2.5V to 5.5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Temperature Conversion Time	t _{CONV}	9-bit resolution			93.75	ms	1
		10-bit resolution			187.5		
		11-bit resolution			375		
		12-bit resolution			750		
Time to Strong Pullup On	t _{SPON}	Start Convert T Command Issued			10	μs	
Time Slot	t _{SLOT}		60		120	μs	1
Recovery Time	t _{REC}		1			μs	1
Write 0 Low Time	t _{LOW0}		60		120	μs	1
Write 1 Low Time	t _{LOW1}		1		15	μs	1
Read Data Valid	t _{RDV}				15	μs	1
Reset Time High	t _{RSTH}		480			μs	1
Reset Time Low	t _{RSTL}		1			ms	1
Presence-Detect High	t _{PDHIGH}		15		60	μs	1
Presence-Detect Low	t _{PDLOW}		60		240	μs	1
Capacitance	C _{IN/OUT}				25	pF	

2) See Figure 17 for the timing sequence.

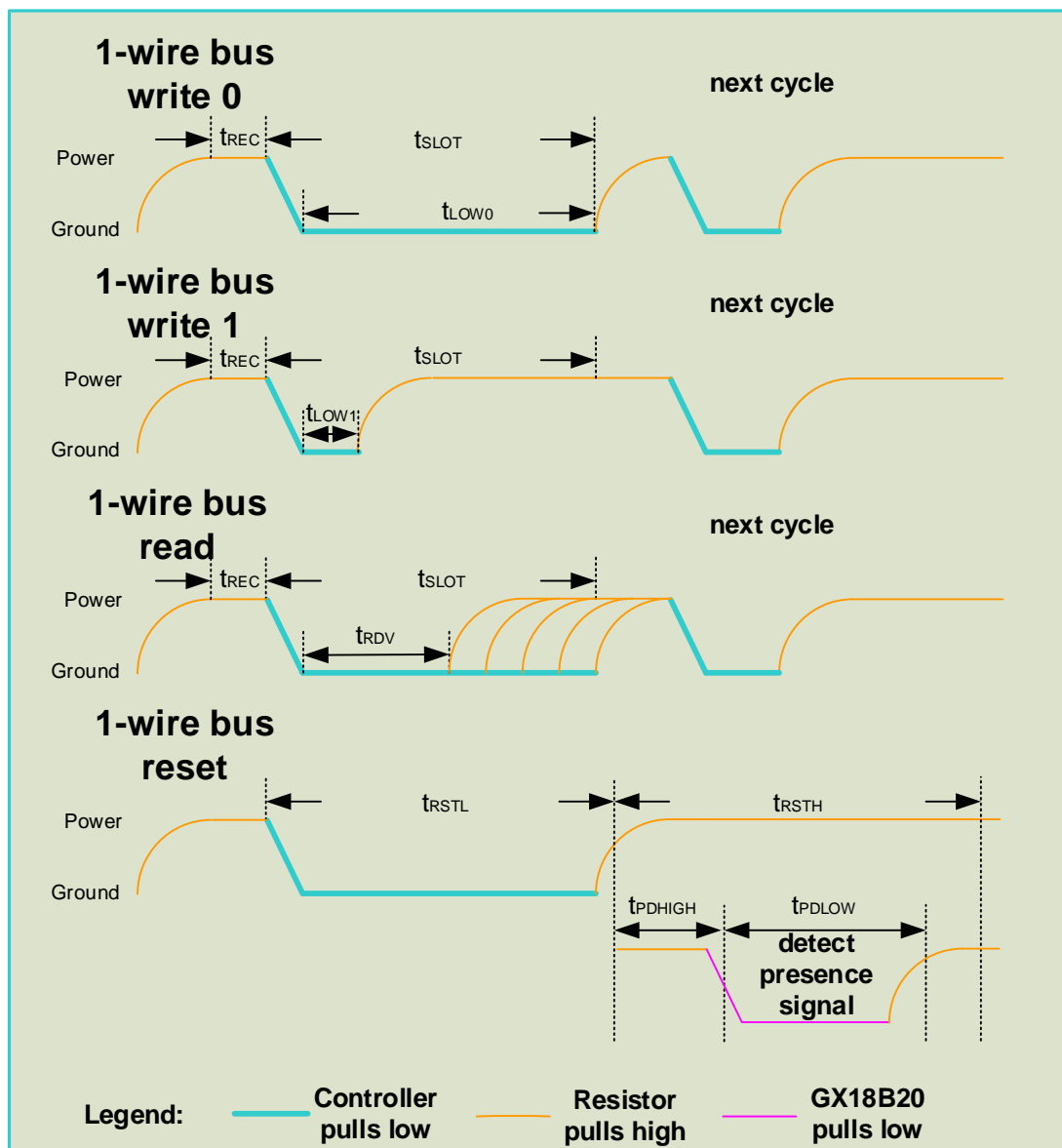


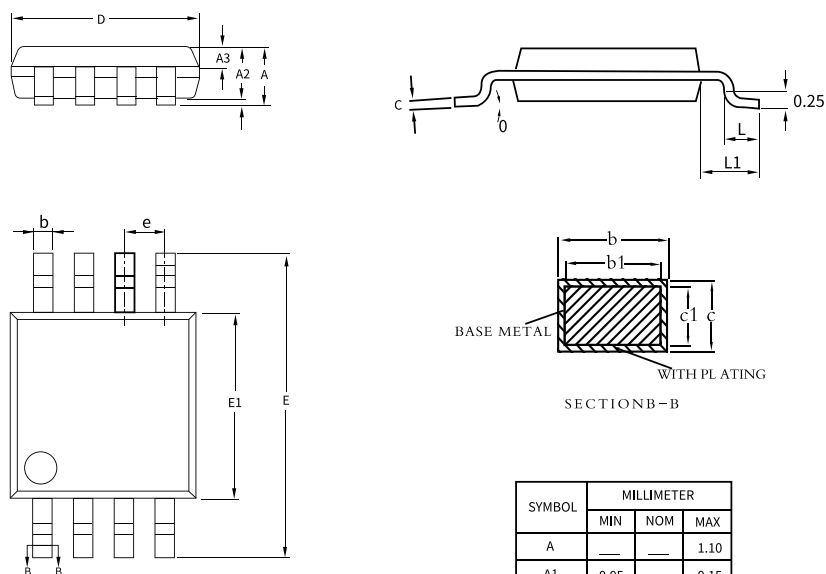
Figure 17. Timing Diagrams

16. Product Package Model List

Product	package	accuracy
GX18B20H	TO-92 (3 pin)	$\pm 0.1^{\circ}\text{C}$
GX18B20UH	MSOP8	$\pm 0.1^{\circ}\text{C}$

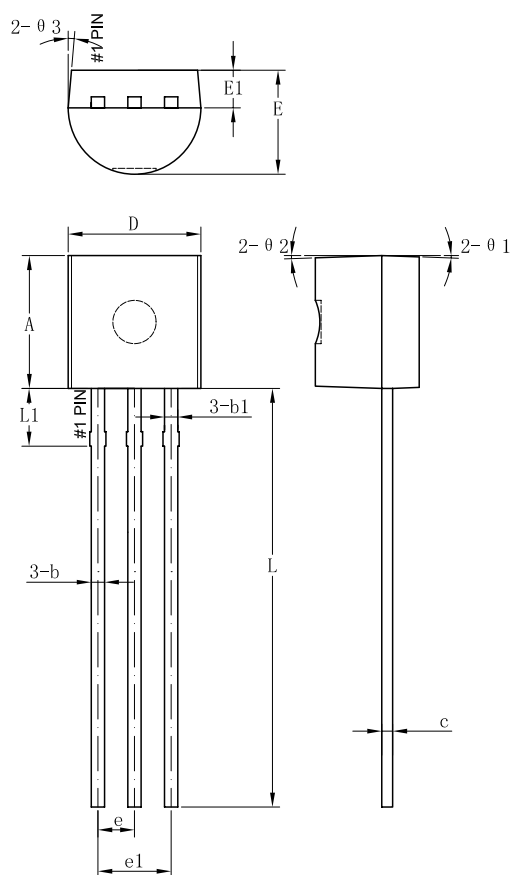
16.1 Package size

MSOP8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.10
A1	0.05	—	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.28	—	0.36
b1	0.27	0.30	0.33
c	0.15	—	0.19
c1	0.14	0.15	0.16
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
e	0.65BSC		
L	0.40	—	0.70
L1	0.95REF		
0	0	—	8°

T092



符号	机械尺寸/mm		
	最小值	典型值	最大值
A	4.5	4.6	4.7
b	0.38	0.45	0.56
b1		0.45	
c	0.36	0.38	0.51
D	4.5	4.6	4.7
E	3.45	3.6	3.75
E1	1.2	1.3	1.4
e		1.27	
e1		2.54	
L	13.5	14.5	15.3
L1		1.96	
$\theta 1$		2°	
$\theta 2$		2°	
$\theta 3$		5°	

Ordering Information

Purchase Number	Device	PIN-Package	SPQ	Remarks
GX18B20H-Bu	GX18B20H	TO92(3)	2000	Bulk
GX18B20UH-T&R	GX18B20UH	MSOP8	4000	Tape and reel