

十四位二进制串行计数器

概述

CD4060 包含一个振荡器和一组十四位二进制串行计数器。振荡器的结构可以是 RC 或晶振电路。Reset 为高电平时，计数器清零且振荡器使用无效，所有的计数器位均为主从触发器。在 CP1 (和 CP0) 的下降沿计数器以二进制进行计数，在时钟脉冲线上使用施密特触发器对时钟上升和下降时间无限制。

CD4060 提供了 16 引线多层陶瓷双列直插 (D)、熔封陶瓷双列直插 (J)、塑料双列直插 (P) 和陶瓷片状载体 (C) 4 种封装形式。

主要特点

- 高达18V的电源（极限）
- 公共复位RESET

- 15V时输入可达12MHz
- 可全静态的工作
- 缓冲输入和输出
- 施密特触发输入脉冲
- 标准化，对称的输出特性
- 5V，10V，15V三个等级

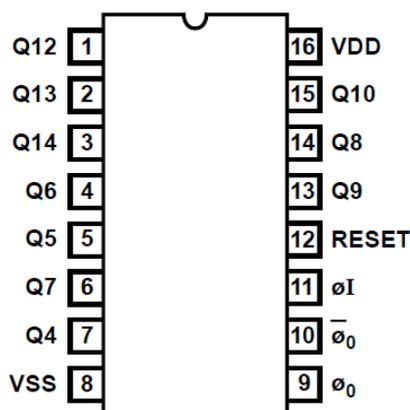
振荡器特点

- RC或晶体振荡器配置
- 在15V时，RC振荡器可达690kHz的频率

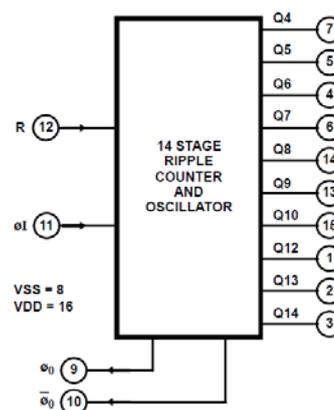
应用

- 控制计数
- 定时器
- 分频器
- 时延电路

引脚排列图



功能框图



极限值 (Ta=25°C)

参数名称	符号	数值	单位
电源电压	Vdd	-0.5 to +17	V
工作电流	Idd	±10	mA
输入电压	VPOL	-0.5 to VDD +0.5	V
工作温度	Topr	-10 to +85	°C
贮存温度	Tstg	-55 to +150	°C

电气参数特性 (若无其它规定: Ta = 25°C)

参数	符号	测试条件 (NOTE 1)		TEMPERATURE (°C)	规范		单位
					MIN	MAX	
Supply Current	IDD	VDD = 15V, VIN = VDD or GND		+25	-	15	uA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 15V	+25	-1	-	uA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 15V	+25	-	1	uA
Output Voltage	VOL15	VDD = 15V, No Load		+25	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		+25	14.95	-	V
Output Current (Sink) (Excluding pins 9 & 10)	IOL5	VDD = 5V, VOUT = 0.4V		+25	0.53	-	mA
	IOL10	VDD = 10V, VOUT = 0.5V		+25	1.4	-	mA
	IOL15	VDD = 15V, VOUT = 1.5V		+25	3.5	-	mA
Output Current (Source) (Excluding pins 9 & 10)	IOH5A	VDD = 5V, VOUT = 4.6V		+25	-	-0.53	mA
	IOH5B	VDD = 5V, VOUT = 2.5V		+25	-	-1.8	mA
	IOH10	VDD = 10V, VOUT = 9.5V		+25	-	-1.4	mA
	IOH15	VDD = 15V, VOUT = 13.5V		+25	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10uA		+25	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10uA		+25	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		+25	VOH > VDD/2	VOL < VDD/2	V
		VDD = 18V, VIN = VDD or GND					
		VDD = 3V, VIN = VDD or GND					
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		+25	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		+25	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		+25	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		+25	11	-	V

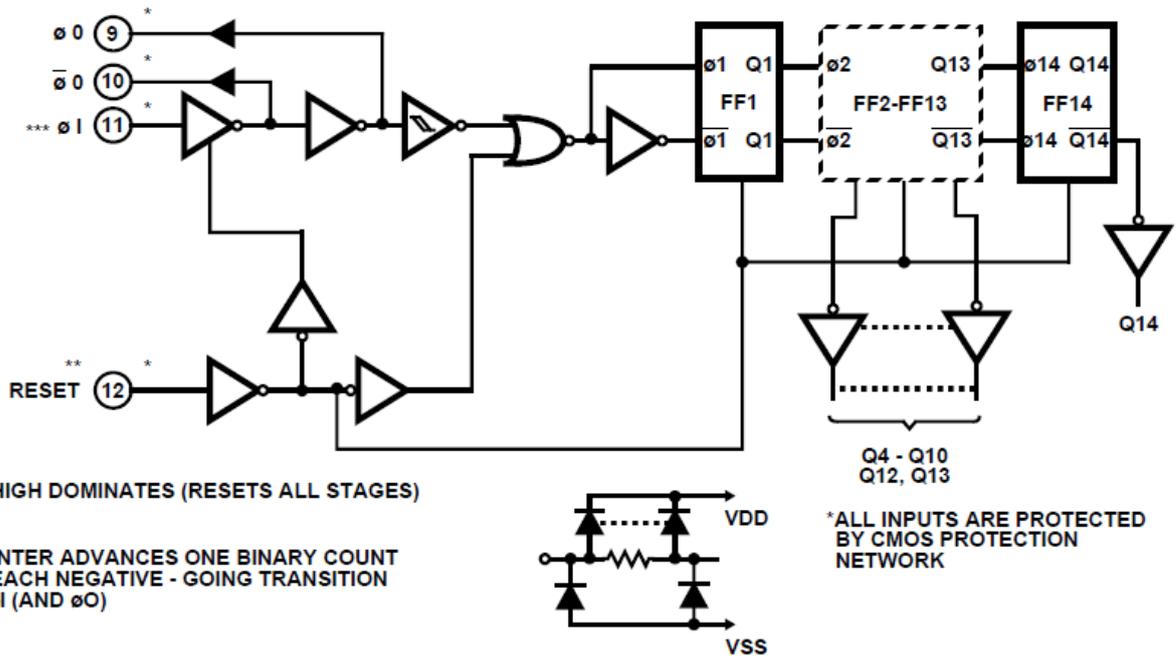
Notes: 1. All voltages referenced to device GND, 100% testing being implemented.

2. Go/No Go test with limits applied to inputs.

3. For accuracy, voltage is measured differentially to VDD. Limits 0.050V max.

参数	符号	测试条件 (NOTE 1)	TEMPERATURE (° C)	规范		单位
				MIN	MAX	
Drive Current at Pin 9 Oscillator Design	IOL	VDD = 5V, VO = .4V	+25	0.16	-	mA
		VDD = 10V, VO = .5V	+25	0.42	-	mA
		VDD = 15V, VO = 1.5V	+25	-1.0	-	mA
Drive Current at Pin 9 Oscillator Design	IOH	VDD = 5V	+25	-	-.16	mA
		VDD = 10V	+25	-	-.42	mA
		VDD = 15V	+25	-	1.0	mA
Propagation Delay Input Pulse ϕ I to Q4	TPLH1	VDD = 10V	+25	-	300	ns
Propagation Delay QN to QN + 1	TPLH2	VDD = 15V	+25	-	200	ns
Propagation Delay RESET	TPHL3	VDD = 10V	+25	-	100	ns
		VDD = 15V	+25	-	80	ns
Transition Time	TTHL TTLH	VDD = 10V	+25	-	160	ns
		VDD = 15V	+25	-	100	ns
Maximum Input Pulse Frequency	F ϕ I	VDD = 10V	+25	-	8	MHz
		VDD = 15V	+25	-	12	MHz
Minimum RESET Pulse Width	TW	VDD = 5V	+25	-	120	ns
		VDD = 10V	+25	-	60	ns
		VDD = 15V	+25	-	40	ns
Minimum Input Pulse Width F = 100kHz	TW	VDD = 5V	+25	-	100	ns
		VDD = 10V	+25	-	40	ns
		VDD = 15V	+25	-	30	ns
RC Operation RX Max	RX	VDD = 5V, CX = 10 F	+25	-	20	M Ω
		VDD = 10V, CX = 50 F	+25	-	20	M Ω
		VDD = 15V, CX = 10 F	+25	-	10	M Ω
RC Operation CX Max	CX	VDD = 5V, RX = 500k Ω	+25	-	1000	F
		VDD = 10V, RX = 300k Ω	+25	-	50	F
		VDD = 15V, RX = 300k Ω	+25	-	50	F
Maximum Oscillator Frequency (Note 4)	RX = 5k Ω	VDD = 10V	+25	530	810	ns
	CX = 15pF	VDD = 15V	+25	690	940	ns
RC Operation Variation of Frequency	CX = 200pF	VDD = 5V	+25	18	25	kHz
	RS = 560K	VDD = 10V	+25	20	26	kHz
	RX = 50k	VDD = 15V	+25	21.1	27	kHz
Variation of Frequency with	CX = 200pF RS = 560K	5V to 10V	+25	-	2	kHz
		10V to 15V	+25	-	1	kHz
Input Capacitance	CIN	Any Input	+25	-	7.5	pF

内部框图



特性曲线

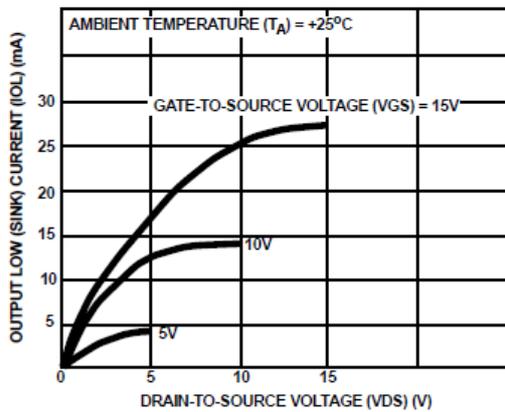


FIGURE 1. TYPICAL N-CHANNEL OUTPUT LOW SINK CURRENT CHARACTERISTICS

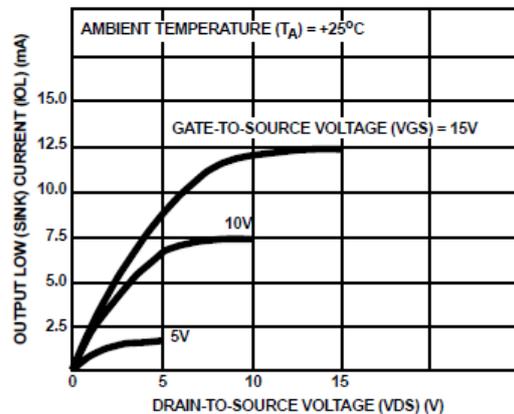


FIGURE 2. MINIMUM N-CHANNEL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

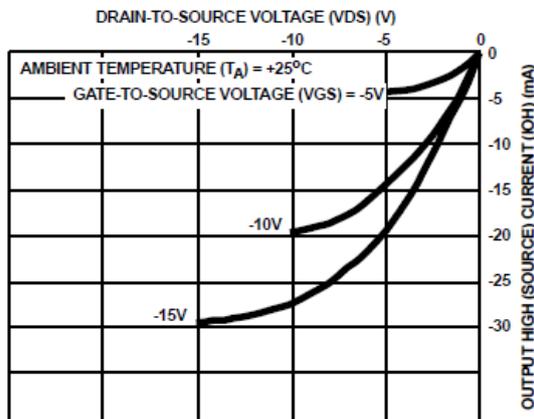


FIGURE 3. TYPICAL P-CHANNEL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

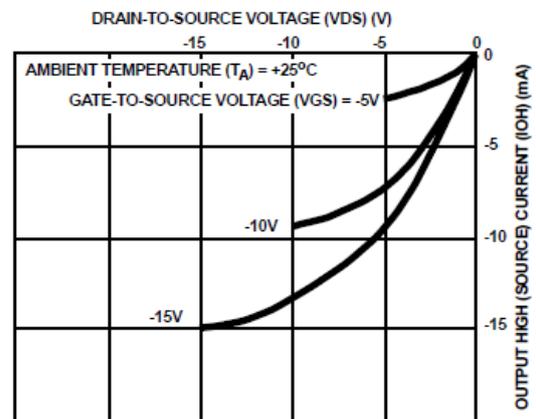


FIGURE 4. MINIMUM P-CHANNEL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

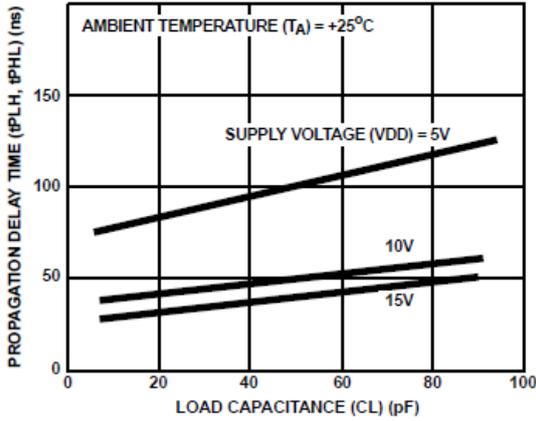


FIGURE 5. TYPICAL PROPAGATION DELAY TIME (Q_N TO Q_{N+1}) AS A FUNCTION OF LOAD CAPACITANCE

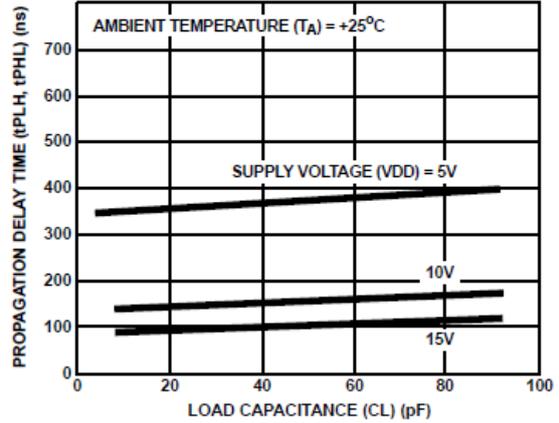


FIGURE 6. TYPICAL PROPAGATION DELAY TIME (Ø1 TO Q4 OUTPUT) AS A FUNCTION OF LOAD CAPACITANCE

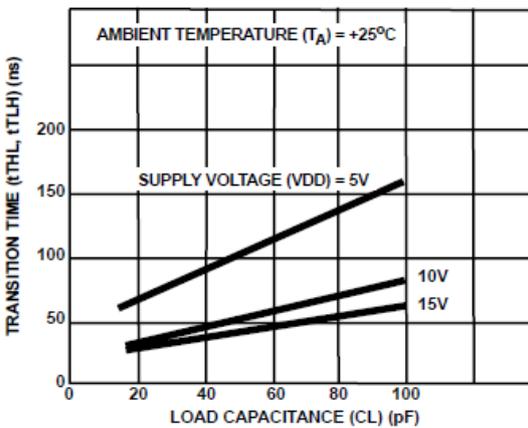


FIGURE 7. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

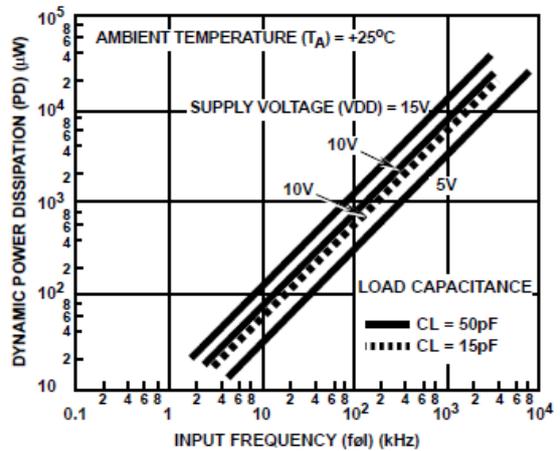


FIGURE 8. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF INPUT FREQUENCY

测试电路

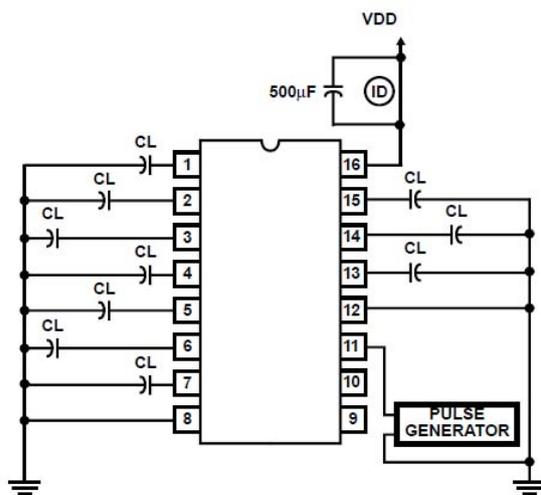


FIGURE 9. DYNAMIC POWER DISSIPATION TEST CIRCUIT

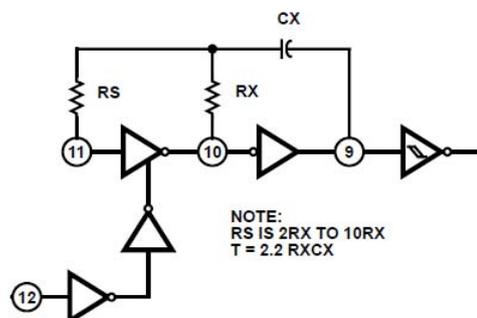
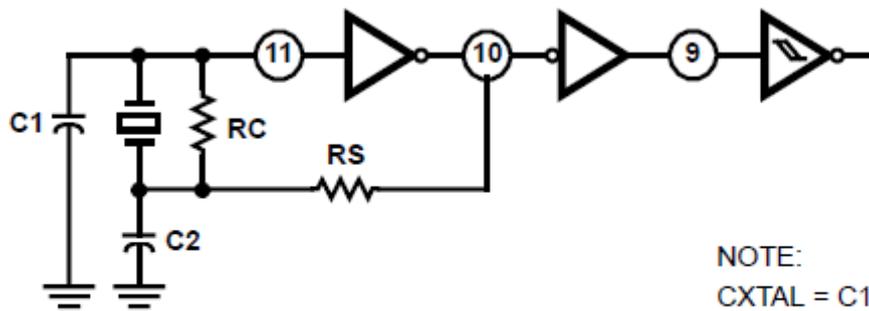


FIGURE 10. TYPICAL RC CIRCUIT



NOTE:
 $C_{XTAL} = C1 + C2 + C_{STRAY}$
 RC = Broader frequency response
 RS = Current limiting

FIGURE 11. TYPICAL CRYSTAL CIRCUIT

封装信息

