N-Channel Enhancement Mode Field Effect Transistor

General Description

Greenchip adopts advanced trench gate super junction technology and design to provide excellent RDS(ON) with low gate charge. This super junction MOSFET fits the industry's AC-DC SMPS requirements for UPS, AC-DC power conversion,ATX power supplies, and industrial power applications.

Features

- Large current and voltage handling capability
- Strong surge current prevention
- New technology for high voltage device
- Low on-resistance and low conduction losses
- Small package
- Ultra Low Gate Charge cause lower driving requirements
- ROHS compliant

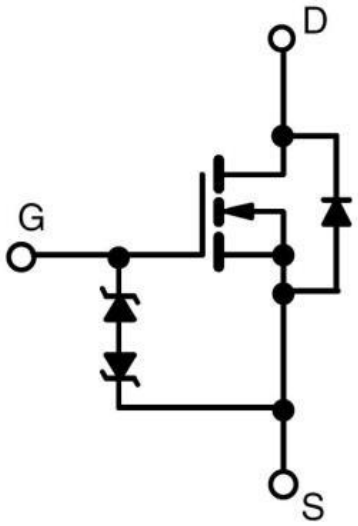
Typical information

$V_{(BR)DSS}$	$R_{DS(ON)typ}$	I_D
650V	70mΩ	50A

Applications

- LCD/LED/PDP TV
- Switched mode power supplies(SMPS)
- Uninterruptible Power Supply（UPS）
- ATX power supplies
- Industrial power applicatio

FRD MOSFET



Schematic diagram

ABSOLUTE MAXIMUN RATINGS

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	V_{DS}	650	V
Drain Current –continuous @25°C	I_D	50	A
Drain Current –continuous @100°C	I_D	30	A
Pulsed Drain Current[1]	I_{DM}	200	A
Gate-Source Voltage	V_{GS}	±30	V
Single Pulse Avalanche[2]	E_{AS}	2160	mJ
Operating Junction & Storage Temperature	T_j, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10sec.)	T_L	300	°C

Note:

1. Pulse width limited by maximum junction temperature.
2. VDD = 90V, VDS = 650V, L=30mH

ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	650			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	2	3	4	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±30V			1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 650V, V_{GS} = 0V			1	mA
		V_{DS} = 650V, V_{GS} = 0V, T_J =150°C			1	mA
On-State Drain Current	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 25A		70	75	mΩ
Body Diode Forward Voltage	V_{SD}	T_J = 25°C, V_{GS} = 0V, I_{SD} = 50A		1	1.4	V
DYNAMIC PARAMETERS						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 50V, f = 1 MHz		3346		pF
Output Capacitance	C_{oss}			218		
Reverse Transfer Capacitance	C_{rss}			1.9		
Total Gate Charge	Q_g	V_{DD} = 100V, I_D = 50A, V_{GS} = 10V		107		nC
Gate-Source Charge	Q_{gs}			27.8		
Gate-Drain Charge	Q_{gd}			37.6		
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{(on)}$	V_{GS} = 10V, V_{DD} = 100V, I_D = 50A, R_G = 25Ω,		44		ns
Rise Time	t_r			40.8		
Turn-Off Delay Time	$t_{(off)}$			268		
Fall Time	t_f			62.3		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				50	A
Forward Voltage	V_{SD}	I_F =Is, V_{GS} = 0V		1		V
Body Diode Reverse Recovery Time	T_{rr}	I_F =Is, di/dt =100A/us		151		nS
Body Diode Reverse Recovery Charge	Q_{rr}			753		nC

ELECTRICAL CHARACTERISTICS DIAGRAMS

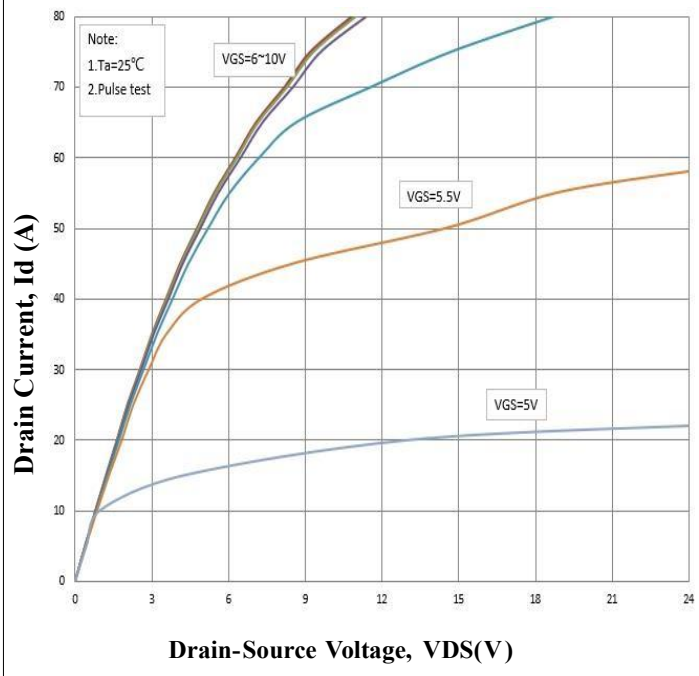


Figure 1. Output characteristics

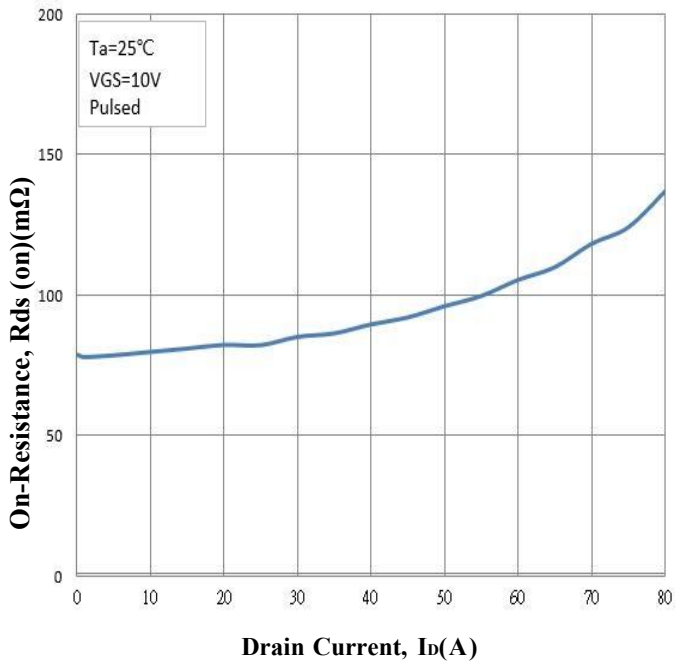


Figure 2. Rdson vs. I_D

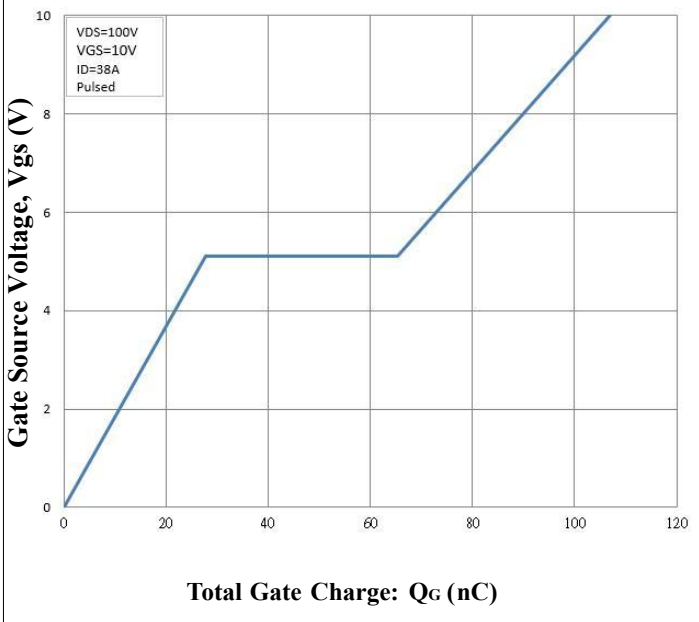


Figure 3. Gate Charge characteristics

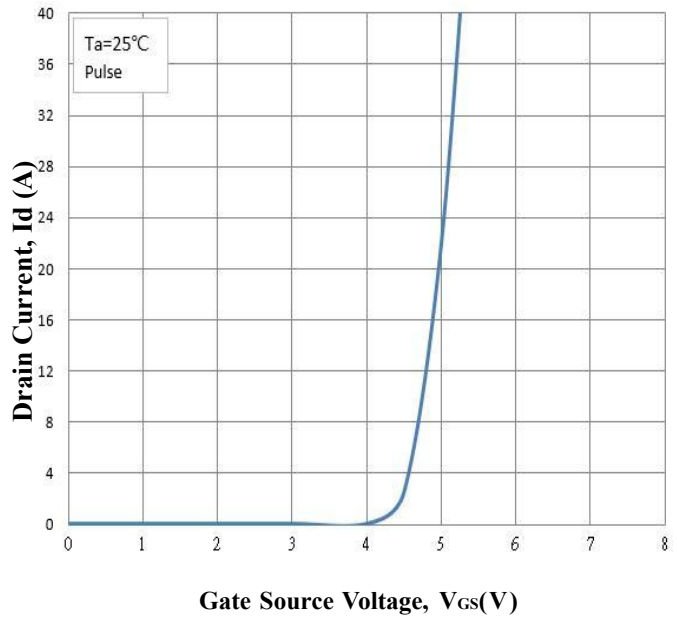


Figure 4. I_D vs. Vgs

ELECTRICAL CHARACTERISTICS DIAGRAMS

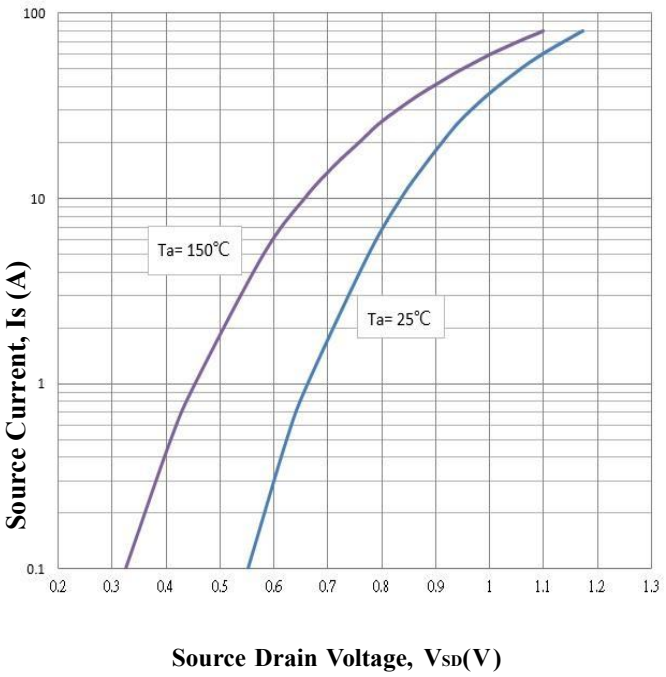


Figure 5. Is vs. V_{SD}

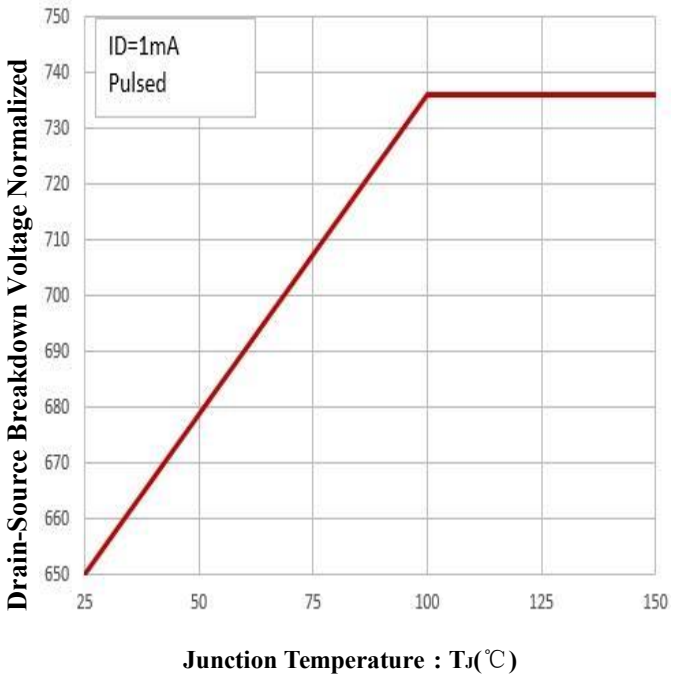


Figure 6. Breakdown vs. Temperature

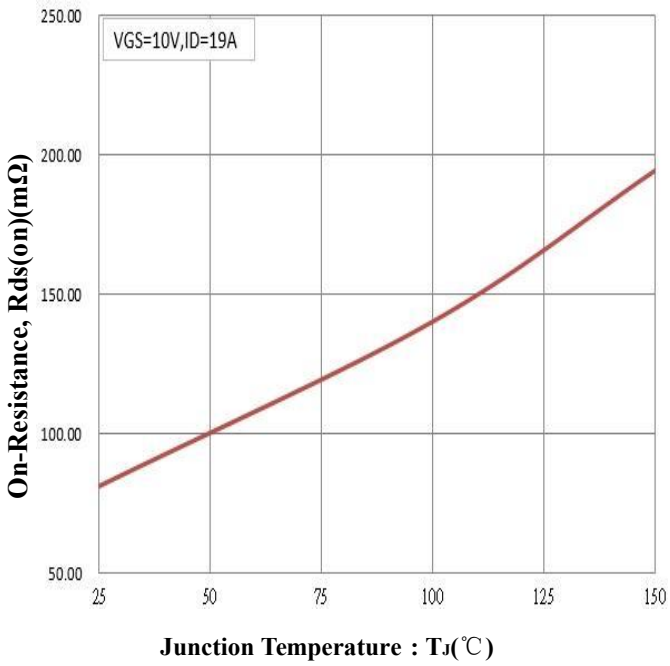


Figure 7. On-Resistance vs. Junction Temperature

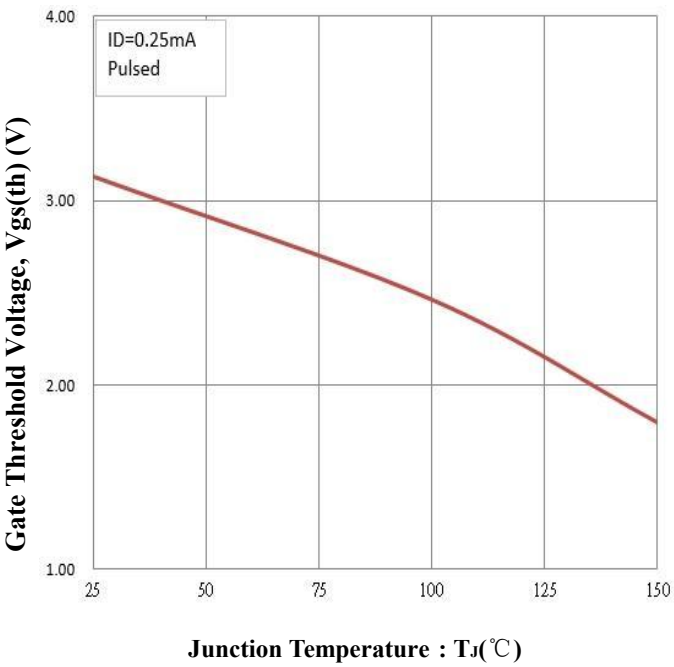


Figure 8. Vth vs. Junction Temperature

ELECTRICAL CHARACTERISTICS DIAGRAMS

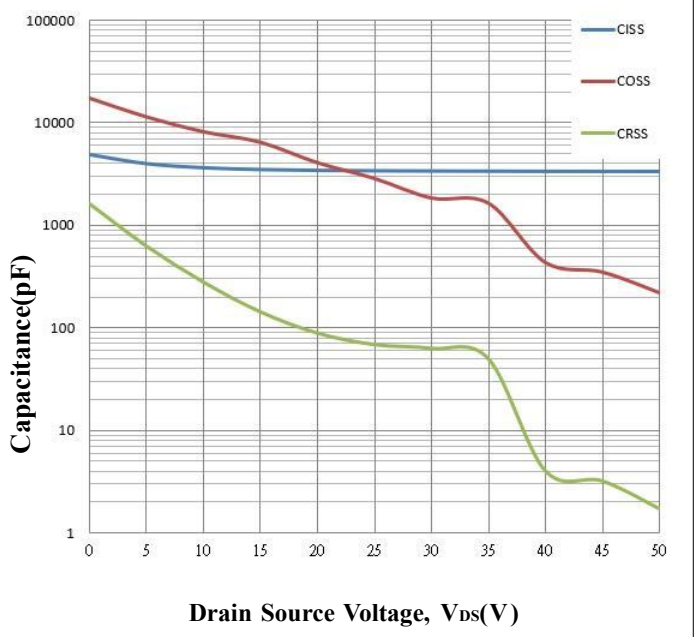


Figure 9. Capacitance characteristics

TO-247-3L Package Outline