# GX28E17 1-Wire-to-I²C Master Communication Bridge

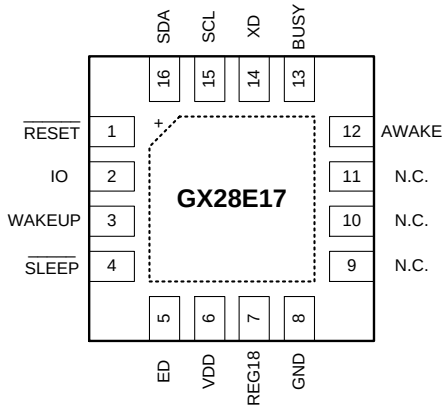
## Features

- Extending I²C Communication Distance via 1-Wire Protocol (Typically 100 meters)
- Pre-programmed unique 64-bit 1-Wire ROM ID at the factory
- 1-Wire interface supports communication speeds of 15kbps and 77kbps
- I²C interface supports communication speeds of 100kHz, 400kHz, and 1MHz
- I²C interface supports clock stretching function
- Chip package: 16-Pin TQFN
- Temperature range: -40°C to +125°C
- Power supply range: 2.4V to 5.5V
- Low static current
  - Normal operation: 250 μA (typ)
  - Sleep mode: 0.3 μA (typ)

## Applications

- Remote Peripheral Identification and Control
- I²C Sensors
- Display Controllers
- Digital-to-Analog, Analog-to-Digital Converters

## Pin Configurations




## Description

GX28E17 is a communication bridge that serves as a 1-Wire slave to I²C master interface. Communication data is serialized through the 1-Wire protocol and converted into corresponding I²C output. The 1-Wire protocol requires only a single signal line, effectively conserving GPIO resources.

Within the 1-Wire bus, GX28E17 possesses a unique ROM ID used as a node address, ensuring the chip can coexist with other devices on the 1-Wire bus and can be individually accessed without affecting other devices.

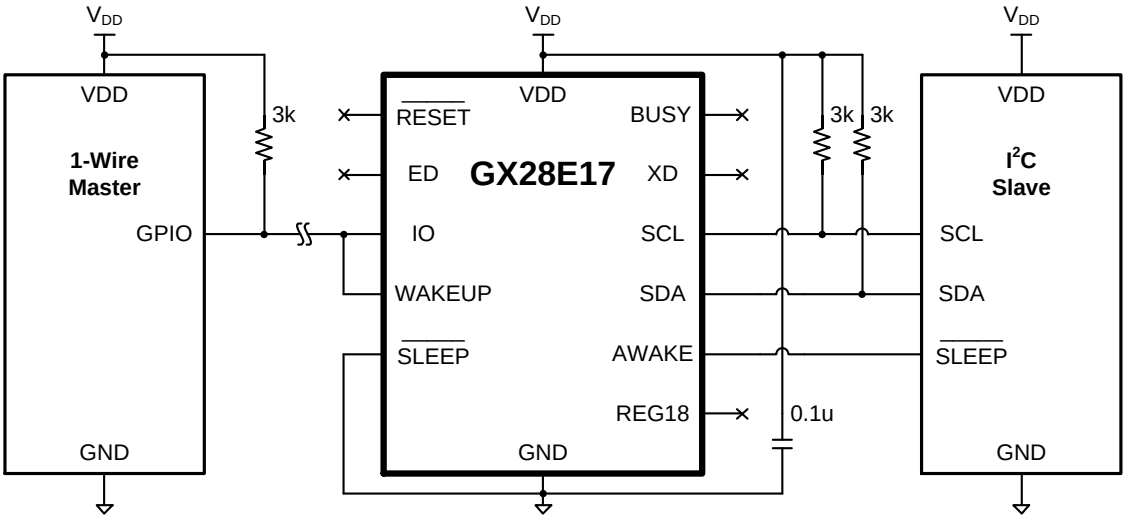
GX28E17 offers flexibility by supporting various 1-Wire and I²C speed modes, making it suitable for multiple complex I²C slave scenarios such as display controllers, ADC, DAC, I²C sensors, and more.

GX28E17 is designed for low-power applications. By utilizing the Sleep pin or a 1-Wire command, it can enter sleep mode, reducing power consumption to 0.3uA. The independent Sleep pin, Wakeup pin, and Awake pin offer flexible options to meet user requirements, with the Awake pin capable of controlling remote power supply.

**Device Information**

| TYPE | Package | Package Size |
|---|---|---|
| GX28E17 | TQFN（16） | 4.0mm × 4.0mm |

## Typical application circuit schematic




## Pin Configurations

| No. | Name | Type | description |
|---|---|---|---|
| 1 | RESET | Bi-directional | Low-level effective reset. This pin can be used as an output to serve as a reset source for other devices. This pin can also accept an external low-level effective reset input. Built-in pull-up resistors enable Wire-AND functionality with internal reset sources. |
| 2 | IO | Open-drain output | 1- Wire communication pin. Open-drain output, requiring a pull-up resistor. |
| 3 | WAKEUP | output | Wake-up pin: When detecting a rising edge, GX28E17 will enter the wake-up state. |
| 4 | SLEEP | output | Sleep pin: When detecting a falling edge, GX28E17 will enter the sleep state. |
| 5 | ED | Push-pull output | Error flag: When GX28E17 detects communication errors, this pin outputs low until receiving a 1-Wire reset command. Communication errors include invalid function commands, CRC-16 checksum errors, and I²C communication errors. |
| 6 | VDD | - | Power supply pin: Voltage range is 2.4V to 5.5V. This pin requires a 0.1uF bypass capacitor. |
| 7 | REG18 | - | Voltage regulator output pin: Typical output is 1.8V. This pin can drive a maximum load of 200uA. |

| | | | |
|---|---|---|---|
| 8 | GND | - | Ground Pin |
| 9,10,11 | N.C. | - | NA |
| 12 | AWAKE | Push-pull output | Wake-up indicator: When GX28E17 is in the wake-up state, this pin outputs high; otherwise, it outputs low. This pin can be used to wake up or put other devices to sleep (based on the wake-up state of GX28E17). |
| 13 | BUSY | Push-pull output | Busy indicator: After GX28E17 receives a complete 1-Wire data packet, this pin outputs low until the I²C communication is completed. When this indicator is low, GX28E17 will ignore all 1-Wire communications. |
| 14 | XD | Push-pull output | Wait-for-data indicator: After GX28E17 receives a function command, this pin outputs low until a complete 1-Wire data packet is received. Note: For function commands that do not require a complete 1-Wire data packet, this pin will not output low. |
| 15 | SCL | Open-drain output | I²C Serial Clock Pin. Requires a pull-up resistor. |
| 16 | SDA | Open-drain output | I²C Serial data Pin. Requires a pull-up resistor. |

## Specifications

### Abusolute Maximum Ratings

| | Min | Max | Units |
|---|---|---|---|
| Supply VDD | -0.5 | 6 | V |
| Voltage on any pin | -0.5 | (VDD+0.5) and ≤ 6 | V |
| Operating temperature range | -55 | 150 | °C |
| Junction temperature | | 150 | °C |
| Storage temperature | -60 | 150 | °C |

### ESD Ratings

| | | Value | Units |
|---|---|---|---|
| Electrostatic discharge voltage $V_{ESD}$ | Human Body Mode (HBM), per ANSI/ESDA/JEDEC JS-001 | ±5000 | V |
| | Machine Mode (MM), per JEDEC-STD Classification | 300 | V |

## Suggested operating range

| | Min | Typ | Max | Units |
|---|---|---|---|---|
| Suppy VDD | 2.4 | 3.3 | 5.5 | V |
| Operating temperature $T_A$ | - 40 | 25 | 125 | °C |

## Electrical characteristics

If not otherwise specified, the following data represent the characteristics of the chip within the TA = - 40~125℃, VDD=2.4V~5.5V range. (Typical operating conditions are +25℃ and 3.3V).

| Parameters | Test conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Supply current | Wake-up state | | 250 | 500 | uA |
| | Sleep state | | 0.3 | 16 | uA |
| Wake-up time | | | 2 | | us |
| Regulated output | | 1.62 | 1.8 | 1.98 | V |

## Detailed Description

GX28E17 consists of a 1-Wire communication front-end (slave), an I²C bus controller (master), and master control logic bridging the two communication protocols. Serial data transmission between the host machine and GX28E17 occurs via the 1-Wire bus. The host machine controls the I²C bus by sending and receiving 1-Wire data packets, which consist of function commands, I²C slave addresses, I²C data lengths, and I²C data content, among other elements. Note: Both read and write operations on the 1-Wire bus begin with the least significant bit of the data.

The 1-Wire bus is a single-master, multiple-slave communication system implemented using a single signal line. All devices on the bus must drive the bus at the appropriate times, requiring them to be mounted on the bus in an open-drain output configuration. The 1-Wire protocol is command-based, and the command hierarchy architecture of GX28E17 is depicted in Figure 1.

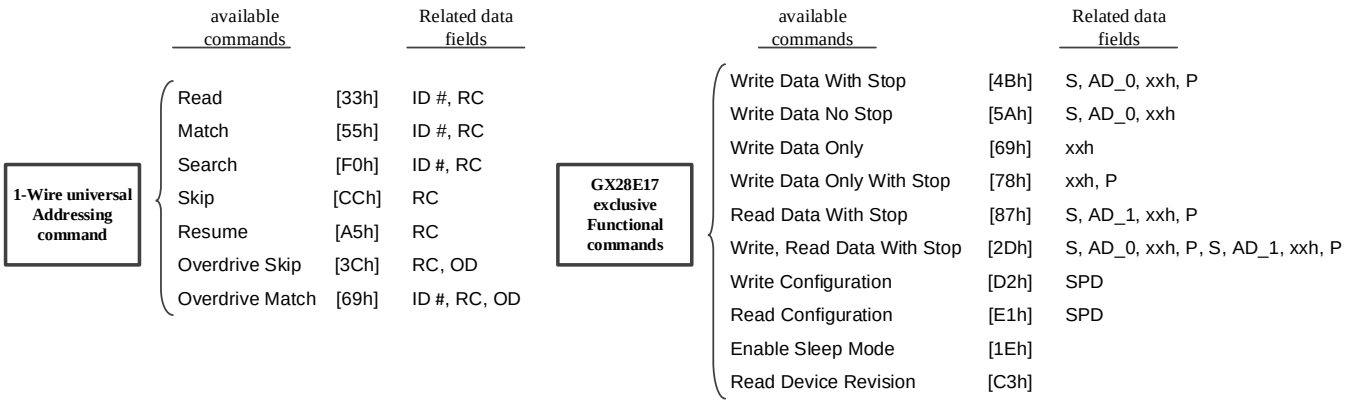



Figure 1: Command Hierarchy Architecture of GX28E17

GX28E17 supports Standard Mode and Overdrive Mode, corresponding to maximum communication rates of 15kbps and 77kbps, respectively, on the 1-Wire bus. The pull-up resistor value on the 1-Wire bus mainly depends on the network size and the capacitance load of the bus. Generally, larger networks or heavier loads typically require smaller pull-up resistors to meet the 1-Wire timing requirements.

In the 1-Wire bus, GX28E17 has a 64-bit unique ROM ID used as a node address, ensuring the chip's coexistence with other devices on the 1-Wire bus and allowing individual access without affecting other devices. The ROM ID comprises an 8-bit family code, a 48-bit unique serial number, and an 8-bit CRC (Cyclic Redundancy Check) as shown in Figure 2. The CRC is computed using a polynomial $x^8 + x^5 + x^4 + 1$ over the family code and serial number.

The CRC generator consists of a shift register and XOR gates, as depicted in Figure 3. Initially, the shift register is set to all zeros, and then the bits are sequentially shifted in from the least significant bit of the family code to the most significant bit of the serial number. When all data bits have been shifted in, the value in the shift register represents the CRC. If the bits of the CRC are shifted in again in the same order, the value in the shift register will rever to all zeros.

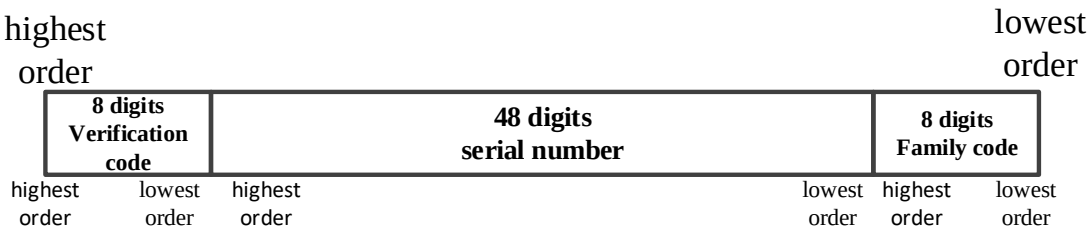



Figure 2: 64-bit ROM ID

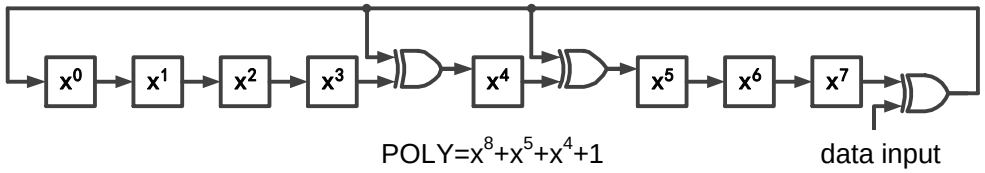



Figure 3: CRC-8 Generator

## 1-Wire Signal Timing

GX28E17 requires a strict protocol to ensure the integrity of communication data. The 1-Wire protocol defines six basic signal types on a single signal line: Reset Pulse, Presence Pulse, Write 0, Write 1, Read 0, and Read 1. Except for the Presence Pulse, all signals are initiated by the master and are timed from the falling edge of the bus. GX28E17 supports two 1-Wire communication speed modes: Standard Mode and Overdrive Mode. Overdrive Mode needs a specific command to enter and exits upon receiving a standard mode reset pulse (bus pulled low for more than 480us). Faster timing is applied under Overdrive Mode.

The initialization sequence, consisting of a Reset Pulse followed by a Presence Pulse (as shown in Figure 4), is a necessary starting step for all communication in the 1-Wire protocol. The master sends a Reset Pulse by pulling the bus low for more than 480us in Standard Mode or more than 48us in Overdrive Mode. GX28E17 recognizes the Reset Pulse, resets its communication state, and then waits for a certain time after the Reset Pulse ends (master releases the bus) to send a Presence Pulse (by pulling the bus low for 60~240us or 8~24us ). To detect the Presence Pulse, the master must sample the bus within a specific window of time. If the bus is sampled as low, it indicates the Presence Pulse, signifying that GX28E17 is ready to start communication. If the bus is sampled as high, it indicates no Presence Pulse, meaning the Reset Pulse wasn't recognized by GX28E17, or no device is attached to the bus

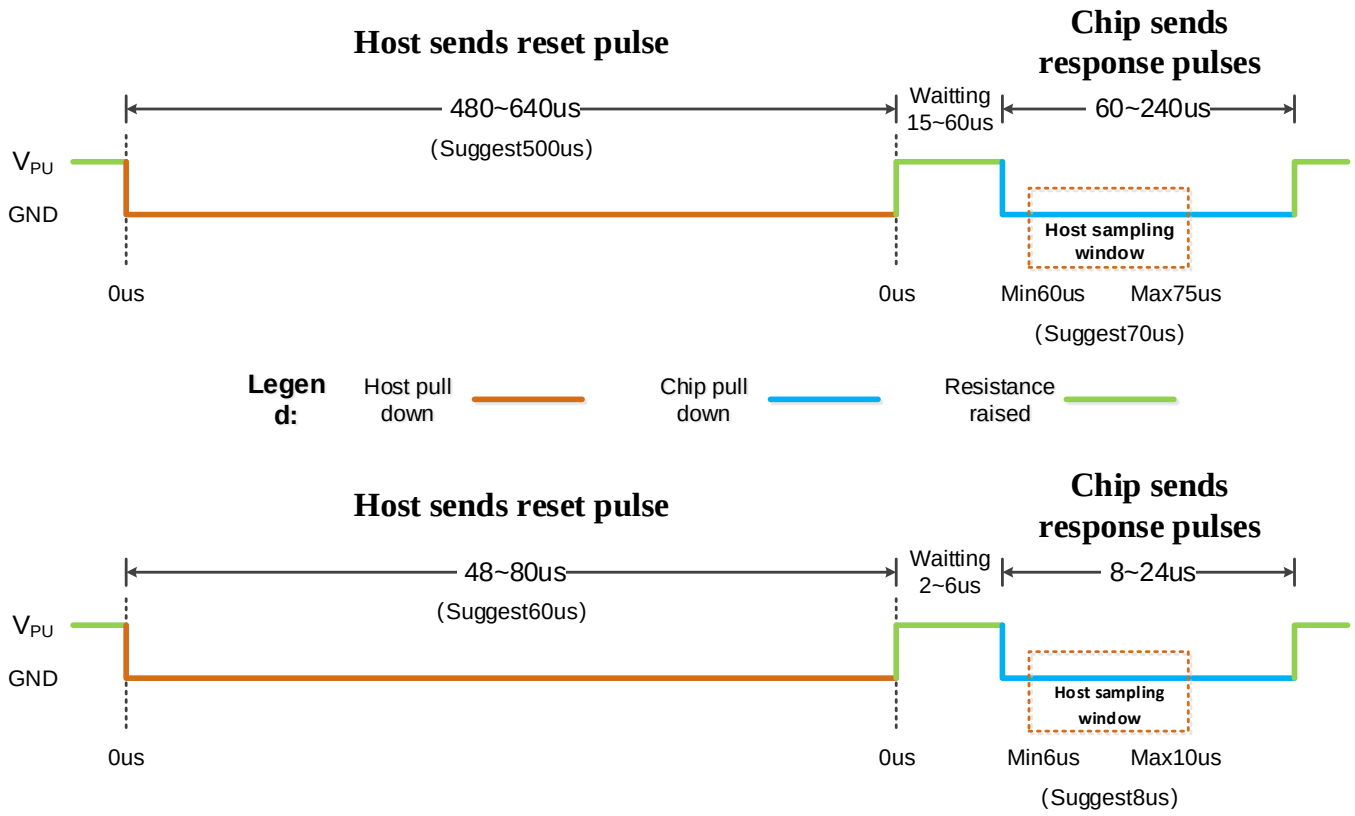



Figure 4: Initialization Sequence (Above: Standard Mode; Below: Overdrive Mode)

1- Wire data transmission operates on time slots, serving as the fundamental unit, carrying only one bit of data per slot. Write slots transfer data from the master to GX28E17, while read slots transfer data from GX28E17 to the master. Both read and write slots start with the master pulling the bus low. The slot width is not less than 65us in Standard Mode and not less than 13us in Overdrive Mode. There must be a recovery time of not less than 1us between adjacent slots. These determine the maximum achievable communication rate.

Upon initiation of a write slot, GX28E17 samples the bus within a specific window of time, as illustrated in Figure 5. The sample result represents one bit of data received by GX28E17. Thus, write slots can further be classified into the following two signals:

Write 1 slot: After the master pulls the bus low, it must release the bus within 15us (or 2us in Overdrive Mode).

Write 0 slot: After the master pulls the bus low, it must maintain it low for at least 60us before releasing the bus (or at least 6us in Overdrive Mode).

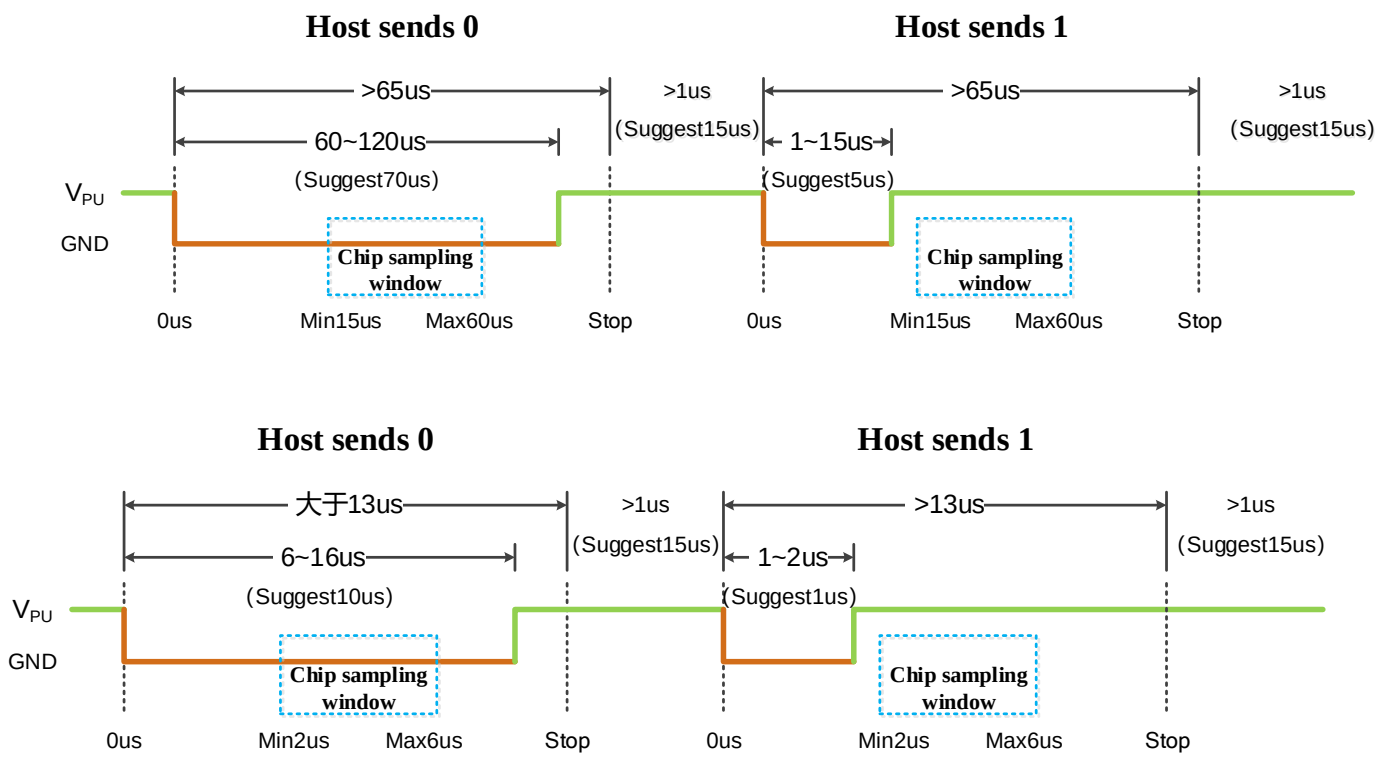
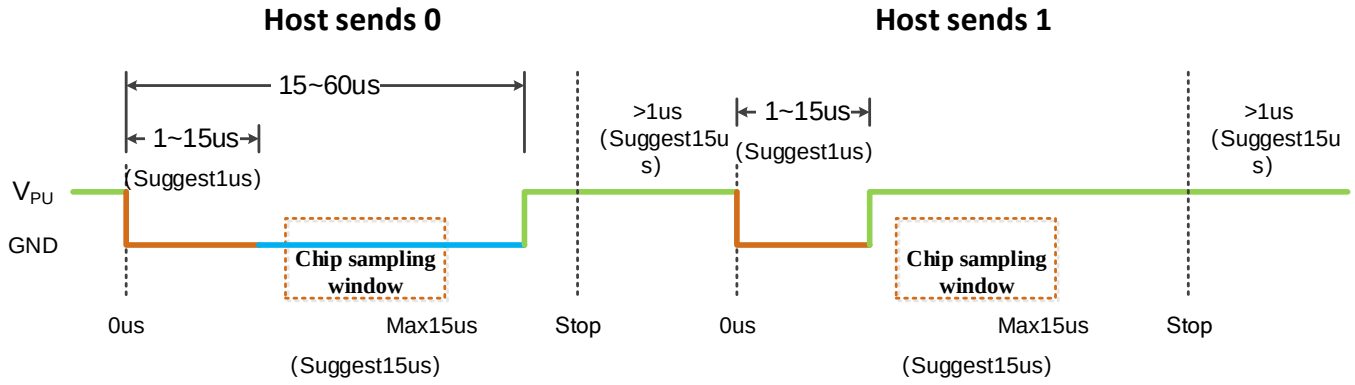



Figure 5: Write Slot (Above: Standard Mode; Below: Overdrive Mode)



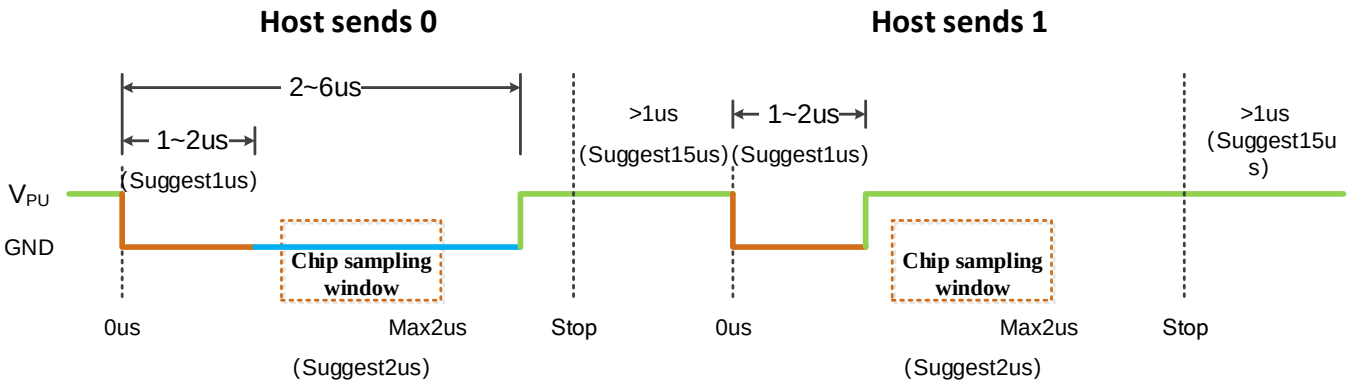



Figure 5: Read Slot (Above: Standard Mode; Below: Overdrive Mode)

When and only when the master initiates a read slot, GX28E17 can send data to the master. As shown in Figure 6, after the master pulls the bus low to initiate a read slot, it must maintain the bus low for 1~15us to ensure the bus's falling edge can be recognized by GX28E17. Upon successful recognition, GX28E17 determines the subsequent bus operation based on the data it intends to send. Thus, read slots can further be classified into the following two signals:

- Read 1 slot: The bus is released directly from the falling edge.
- Read 0 slot: Starting from the falling edge, the bus is pulled low and maintained for 15~60us (2~6us us in Overdrive Mode)

To receive data transmitted by GX28E17, the master must sample the bus within a specific window of time, and the sample result represents the received bit of data. Note: The effective duration of data for a Read 0 slot is at least 15us (or 2us in Overdrive Mode), therefore the sampling window should not exceed this effective duration. For maximum timing margin, it's recommended to release the bus by the master as early as possible (1us for both Standard Mode and Overdrive Mode), and delay the sampling time as much as possible (15us for Standard Mode and 2us for Overdrive Mode).

In a 1-Wire environment, due to factors such as noise interference and signal reflection, the bus transition may exhibit non-ideal waveforms such as ringing or glitches, leading GX28E17 to lose synchronization with the master. Consequently, this might result in scenarios like the Search ROM command entering a loop or the forced termination of function commands. To improve performance in a 1-Wire multi-slave network application, GX28E17 utilizes Schmitt trigger inputs and glitch filtering circuits to suppress sensitivity to bus noise. Figure 7 illustrates GX28E17's noise suppression characteristics in three typical scenarios: (the glitch filter is only enabled in Standard Mode and disabled in Overdrive Mode)

Scenario 1: The bus voltage exceeds the high threshold (VTH) but doesn't fall below the low threshold (VTL), this glitch is filtered by the Schmitt trigger.

Scenario 2: The bus voltage exceeds the high threshold and falls back to the low threshold within 1us, this glitch is filtered by the filtering circuit.

Scenario 3: The bus voltage exceeds the high threshold and falls back to the low threshold after 1us, this glitch is not filtered and is considered the start of a new slot.

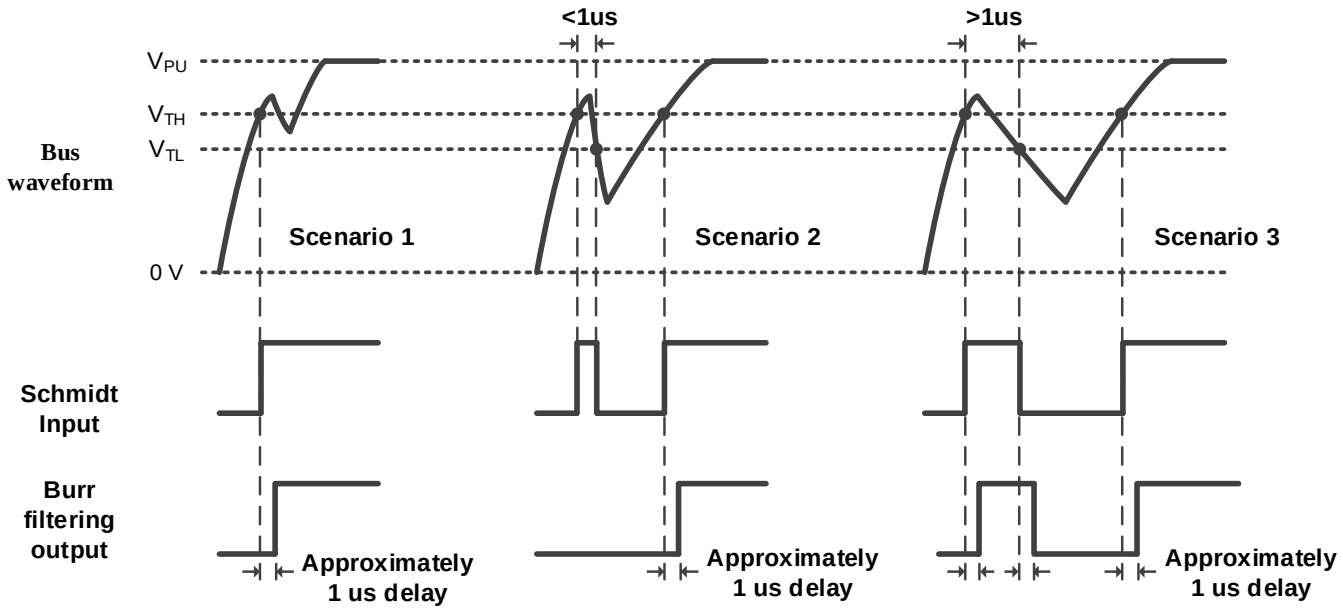



Figure 7: Noise Suppression Characteristics

The 1-Wire communication process of GX28E17 consists of four parts: Initialization Sequence, Addressing Commands, Function Commands, and I℃ data. After initialization, the master can send addressing commands to search for and select specific devices. GX28E17 supports seven addressing commands, and their execution flow is shown in Figure 8.

- Read ROM [33h]

This command reads the 64-bit ROM ID of the device. Note: If multiple devices are connected to the bus, all devices start sending data simultaneously, leading to bus conflicts. Under an open-drain connection, the bus behaves as a wire AND output. Therefore, the read data is the bitwise AND of all device ROM IDs. At this point, the cyclic redundancy check (CRC) of the read family code and serial number won't match the read checksum.

- Match ROM [55h]

This command directly follows the 64-bit ROM ID and is used to address a specific device. Only devices with fully matching ROM IDs proceed with subsequent function commands. All other devices remain in an idle state, waiting for the next reset pulse.

- Search ROM [F0h]

When the system starts, the master might not know the number or ROM IDs of connected devices. This command, combined with a corresponding binary tree search algorithm, identifies the ROM IDs of all devices on the bus. Starting from the least significant bit, for each bit of the ROM ID, the master initiates three slots. In the first slot, all devices involved in the search send the true value of their ROM ID bit. In the second slot, they send the complement of their ROM ID bit. In the third slot, the master sends the desired true value for that bit. Devices whose ROM IDs don't match the master's selection value exit the search process, waiting for the next reset pulse. Utilizing the wire AND property of the bus, information about the ROM ID bit of all devices participating in the search can be inferred from the results of the first and second slots. When both the true value and its complement are 0, it indicates a difference in the ROM ID bit among devices. By selecting the choice value in the third slot, the master enters a branch of the search tree. After a round of search, the 64-bit choice value becomes the ROM ID of one device on the bus. At this point, all devices except that one enter an idle state. Repeating multiple rounds confirms the ROM IDs of all devices on the bus.

- Skip ROM [CCh]

This command directly addresses all devices on the bus. Note: If subsequent function commands are read-type commands, bus data conflicts will occur.

- Resume ROM [A5h]

This command allows direct addressing of the previously selected device, maximizing data throughput. GX28E17 has an RC flag internally. The RC flag is set to 1 only when the search, match, or overdrive match commands are executed successfully. Before each execution of search, match, overdrive match, read, skip, or overdrive skip commands, the RC flag is set to 0. Once the RC flag is 1, the master can repeat addressing the device by using the resume command.

- Overdrive Skip ROM [3Ch]

This command addresses all devices on the bus while configuring all devices supporting overdrive mode to enter overdrive mode (OD=1). Subsequent communication must adhere to the signal timing of overdrive mode until a standard mode reset pulse (bus pulled low for more than 480us) resets all devices to standard mode (OD=0).

- Overdrive Match ROM [69h]

This command follows the 64-bit ROM ID sent in overdrive mode and addresses a specific device while configuring it to enter overdrive mode (OD=1). If a device is already in overdrive mode before receiving this command, whether the match is successful or not, it won't exit overdrive mode until receiving a standard mode reset pulse.

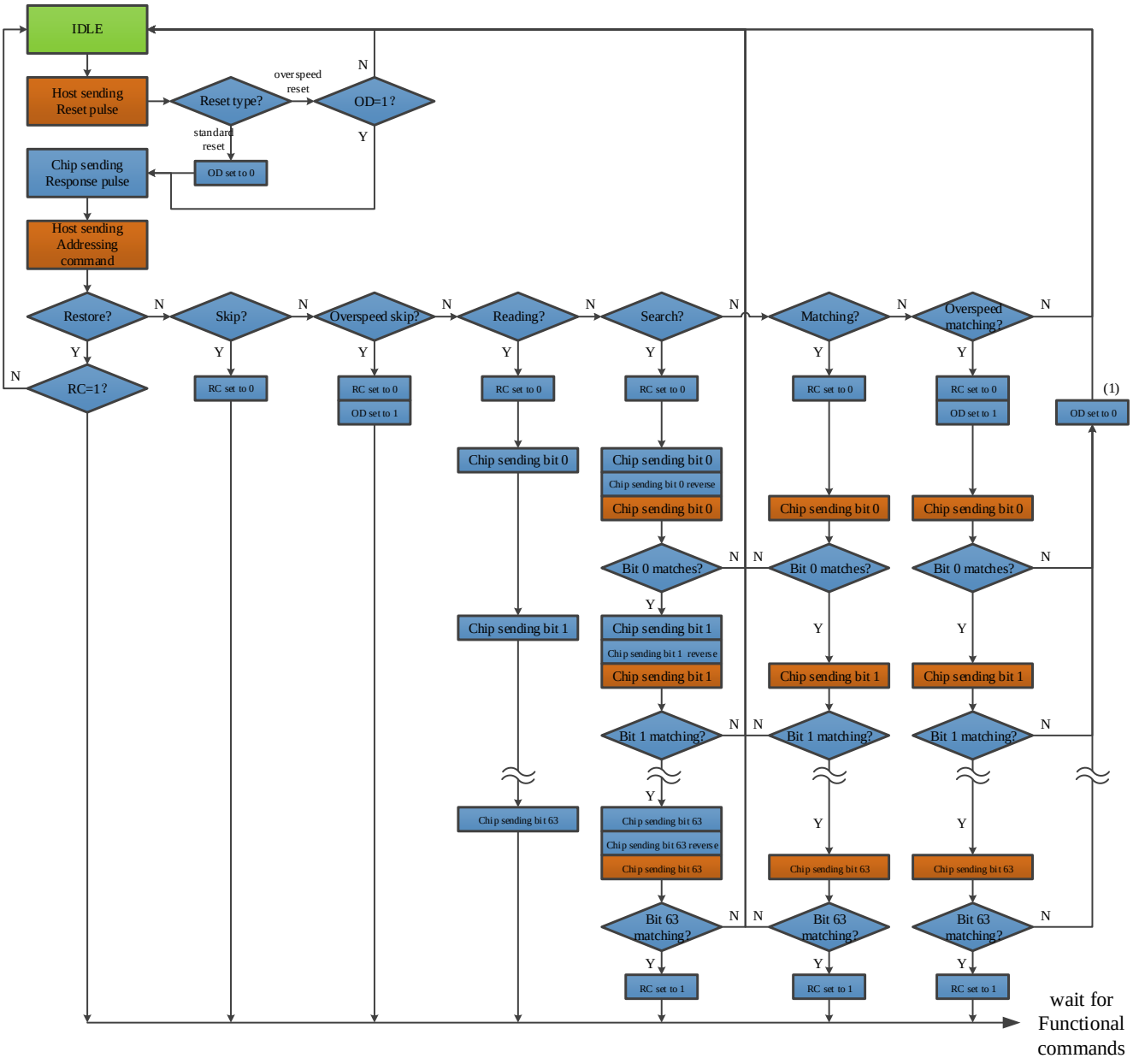



Figure 8 - Addressing Commands Flow

Note (1): If already in Overdrive Mode before receiving the [Overdrive-Match] command, the OD flag will remain at 1.

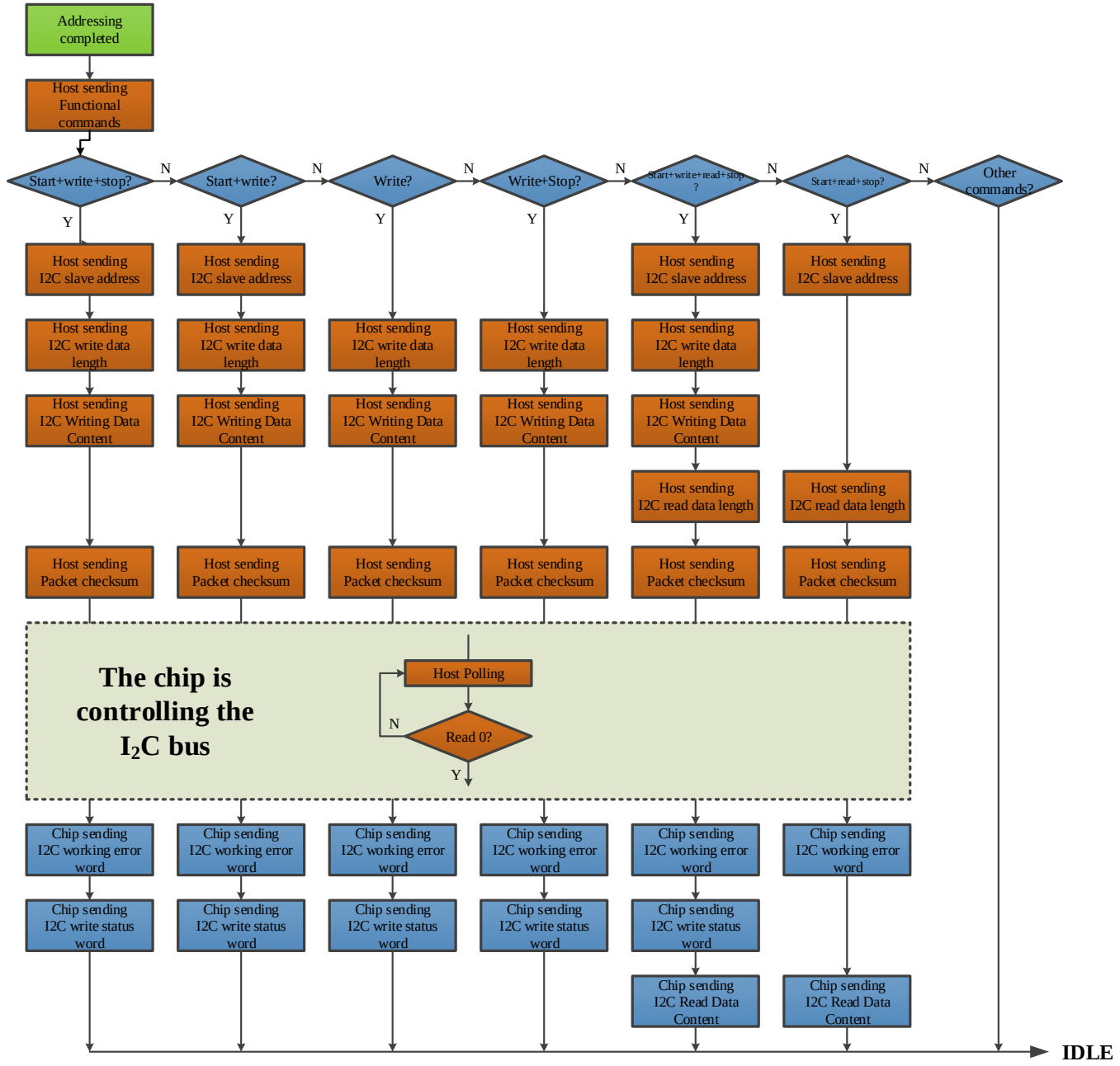



Figure 9 - Function Commands Flow

The addressed GX28E17 can receive and execute subsequent functional commands. GX28E17 supports six types of I²C control commands, as depicted in Figure 9. These commands, along with corresponding additional parameters (I²C slave address, write data length, write data content, read data length, and checksum), together form a 1-Wire data packet. The write/read data length indicates the number of bytes for data write or read, and can be set from 1 to 255. If the length is set to 0, it will cause the Error Detection (ED) pin to be set, and GX28E17 will enter an idle state. The 16-bit checksum serves as the cyclic redundancy check (CRC) of the 1-Wire data packet (excluding the checksum itself) with a generating polynomial of $x^{16} + x^{15} + x^2 + 1$. Unlike the CRC-8 in the ROM ID, the CRC-16 uses the complement of the verification result. GX28E17 integrates a CRC-16 generator as shown in Figure 10, which performs CRC-16 calculation simultaneously upon receiving the data packet. If the calculated result does not match the received checksum, it will cause the Error Detection (ED) pin to be set, and GX28E17 will enter an idle state.

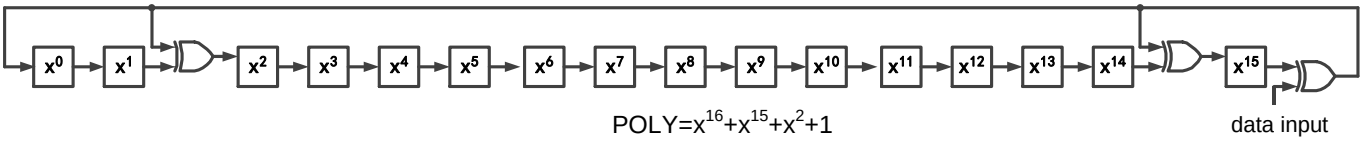



Figure 10 CRC-16 Generator

After the completion of sending the 1-Wire data packet, GX28E17 initiates control of the I²C bus based on the contents of the data packet. At this point, the host can query the completion status in three ways: 1. Wait for a specific delay; 2. Poll the Busy Flag pin (BUSY); 3. Poll the bus (continuously initiate read time slots, where a read 1 signifies the task is ongoing, and a read 0 indicates completion). Regardless of the method chosen, the host must query the bus at least once. Reading a bit value of 0 represents the completion of the task before any subsequent data bytes can be read. Upon completing the bus query, the host can choose to read two bytes representing the I²C communication status (error status byte and write status byte).

Table 1 - Error Status Byte

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Invalid Start | 0 | Invalid Adress | Checksum Error |

Table 2 - Description of Error Status Byte Contents

| Flag Name | Description |
|---|---|
| Invalid Start | A value of 1 indicates: When GX28E17 sends the start condition, the SCL line is pulled down by another device, preventing the correct generation of the start condition. |
| Invalid Adress | A value of 1 indicates: The I²C address sent by GX28E17 did not receive an ACK. |
| Checksum Error | A value of 1 indicates: The checksum calculated by GX28E17 does not match the received checksum. |

Table 3 - Write Status Byte

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| WB[7] | WB[6] | WB[5] | WB[4] | WB[3] | WB[2] | WB[1] | WB[0] |

Table 4 - Description of Write Status Byte Contents

| Flag Name | Description |
|---|---|
| WB[7:0] | Indicates from which byte the write data is not acknowledged (NACK) by the slave N. A value of 0 represents all bytes acknowledged by the slave. |

When the value of the error status byte is not 00h, the error flag pin (ED) will be set until a 1-Wire reset pulse is received, clearing it. Simultaneously, the value of the write status byte will be FFh because the I℃ communication hasn't been initiated yet.

To visually describe the functional commands, consider the following schematic:

Table 5 - Legend for Color Representation

| | |
|---|---|
| 1-Wire | The host writing to GX28E17 |
| | The host reading to GX28E17 |
| | "The host polling GX28E17 |
| I²C | GX28E17 writing to the I℃ slave. |
| | "GX28E17 read`ing to the I℃ slave." |

Table 6 - I℃ Identification Description

| Flag Name | Description |
|---|---|
| S | Start Condition |
| Sr | Repeated Start Condition |
| AD,0 | Write Address |
| AD,1 | Read Address |
| xxh[#] | Write Data |
| (xxh)[#] | Read Data |
| P | Stop Condition |
| ACK | ACK |
| NACK | NACK |

Table 7 - Generic 1-Wire Data Flow (Initialization and addressing details are omitted in the following text)

| initialization | | address | 1-Wire packet | | I²C Controlling | Return results | |
|---|---|---|---|---|---|---|---|
| reset pulse | Response pulse | Addressing command | Functional commands | Command parameters | Polling | status word | Read data |

Table 8 - Typical I²C Data Flow (Using a two-byte write as an example)

| I²C Controlling | | | | | | | |
|---|---|---|---|---|---|---|---|
| S | AD,0 | ACK | $xxh_{[1]}$ | ACK | $xxh_{[2]}$ | ACK | P |

- **The command "Start, Write Data, Stop (Write Data with Stop) [4Bh]**

Addresses the I²C slave and writes 1 to 255 bytes during a single communication. The number of bytes in the written data must match the specified write data length. GX28E17 determines when to cease receiving based on this length. If there is a mismatch, GX28E17 might incorrectly identify a portion of the data as CRC-16, leading to a command verification error.

1-Wire data flow

| command [4Bh] | slave adress | write length | write data | data packet | polling | Error Status Word | Write Status Word |
|---|---|---|---|---|---|---|---|

expected I²C output

| S | AD,0 | ACK | $xxh_{[1]}$ | ACK | … | $xxh_{[255]}$ | ACK | P |
|---|---|---|---|---|---|---|---|---|

- **Start, Write Data (no Stop) [5Ah]**

The command "Start, Write Data (no Stop) [5Ah]" is used to address an I²C slave device, where data ranging from 1 to 255 bytes is written, but a Stop condition is not sent to conclude the ongoing I²C communication.

1-Wire data flow

| command [5Ah] | slave adress | write length | write data | data packet | polling | Error Status Word | Write Status Word |
|---|---|---|---|---|---|---|---|

expected I²C output

| S | AD,0 | ACK | $xxh_{[1]}$ | ACK | … | $xxh_{[255]}$ | ACK |
|---|---|---|---|---|---|---|---|

- **Write Data Only[69h]**

The command writes 1 to 255 bytes but does not send a stop condition to end the current I²C communication.

1-Wire data flow

| command [69h] | slave adress | write length | write data | data packet | polling | Error Status Word | Write Status Word |
|---|---|---|---|---|---|---|---|

expected I²C output

| $xxh_{[1]}$ | ACK | … | $xxh_{[255]}$ | ACK |
|---|---|---|---|---|

- **Write Data Only with Stop[78h]**

The command writes 1 to 255 bytes and sends a stop condition to end the current communication. This command can be combined with the previous two commands for transmitting a large amount of data within a single I²C communication (starting with a start condition and ending with a stop condition).

1-Wire data flow

| command [78h] | slave adress | write length | write data | data packet | polling | Error Status Word | Write Status Word |
|---|---|---|---|---|---|---|---|

expected I²C output

| $xxh_{[1]}$ | ACK | … | $xxh_{[255]}$ | ACK | P |
|---|---|---|---|---|---|

- **Read Data with Stop[87h]**

The command addresses an I²C slave and reads 1 to 255 bytes within a single communication, finally sending a stop condition to end the I²C communication.

1-Wire data flow

| command [87h] | slave adress | write length | write data | data packet | polling | Error Status Word | Write Status Word |
|---|---|---|---|---|---|---|---|

expected I²C output

| S | AD,1 | ACK | $(xxh)_{[1]}$ | ACK | … | $(xxh)_{[255]}$ | NACK | P |
|---|---|---|---|---|---|---|---|---|

- **Write, Read Data with Stop[2Dh]**

The command initially addresses an I²C slave and writes 1 to 255 bytes. Following this, it readdresses to modify the I²C direction to read, then reads 1 to 255 bytes. Finally, it sends a stop condition to conclude this I²C communication.

1-Wire data flow

| command [2Dh] | slave adress | write length | write data | data packet | polling | Error Status Word | Write Status Word |
|---|---|---|---|---|---|---|---|

expected I²C output

| S | AD,0 | ACK | $xxh_{[1]}$ | ACK | … | $xxh_{[255]}$ | ACK | Sr |
|---|---|---|---|---|---|---|---|---|
| | AD,1 | ACK | $(xxh)_{[1]}$ | ACK | … | $(xxh)_{[255]}$ | NACK | P |

Apart from the aforementioned six I²C control commands, GX28E17 supports three configuration commands for modifying the I²C communication rate and entering sleep mode. As these configuration commands do not manipulate the I²C bus, they do not return error status words or write status words.

- **Write Configuration[D2h]**

This command is used to write the configuration word for the I²C communication rate.

1-Wire data flow

| Reset Pulse | Response Pulse | Addressing Command | Command [D2h] | Configuration Byte |
|---|---|---|---|---|

Table 9 Configuration Byte (Power-On Default Value is 01h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | SPD[1] | SPD[0] |

Table 10 Explanation of Configuration Byte Content

| Flag Name | Description |
|---|---|
| SPD[1:0] | 00b=100kHz, 01b=400kHz, 10b=1MHz, 11b=未用 |

- **Read Configuration[E1h]**

The command is used to read the I²C communication rate configuration byte.

1-Wire data flow

| Reset Pulse | Response Pulse | Addressing Command | Command [E1h] | Configuration Byte |
|---|---|---|---|---|

- **Enable Sleep Mode[1Eh]**

The command configures GX28E17 to enter a sleep state. This command functions similarly to the sleep pin (SLEEP). When GX28E17 enters sleep mode, it shuts down all modules, effectively ignoring all 1-Wire communication. Upon detecting a rising edge on the wakeup pin (WAKEUP), GX28E17 exits the sleep state.

1-Wire data flow

| Reset Pulse | Response Pulse | Addressing Command | Command [1Eh] |
|---|---|---|---|

## I²C Signal Timing

I²C bus is a two-wire half-duplex multi-slave communication system, consisting of a Serial Data Line (SDA) and a Serial Clock Line (SCL). SDA and SCL must be configured as open-drain outputs. Note: I²C reads and writes start from the most significant bit of data. For every bit of data transferred, SCL generates a corresponding clock pulse. To ensure the integrity of communication data, the I²C bus specifies that SDA must remain stable when SCL is high; SDA is allowed to change only when SCL is low. If SDA transitions while SCL is high, these two specific occurrences define the start and stop conditions of the I²C communication. Start and stop conditions, along with SCL clock pulses, are generated only by the master. Every slave on the bus must have a unique address and be addressed by the master.

GX28E17, acting as an I²C bus controller (i.e., master), supports three communication speeds: 100kHz, 400kHz, and 1MHz, with the following critical timing parameters:

Table 11 the I²C bus controller timing parameters

| Parameters | Symbol | 100kHz | 400kHz | 1MHz |
|---|---|---|---|---|
| Repeat Start Condition Setup Time | tSU,STA | 5.25us | 1.25us | 0.50us |
| Start Condition Hold Time | tHD,STA | 5.25us | 1.25us | 0.50us |
| Data Setup Time | tSU,DAT | 5.00us | 1.00us | 0.25us |
| Data Hold Time | tHD,DAT | 0.25us | 0.25us | 0.25us |
| Clock High Pulse Width | tHI,SCL | 5.25us | 1.25us | 0.50us |
| Clock Low Pulse Width | tLO,SCL | 5.25us | 1.25us | 0.50us |
| Stop Condition Setup Time | tSU,STO | 5.25us | 1.25us | 0.50us |
| Bus Recovery Time | tBUF | 5.25us | 1.25us | 0.50us |

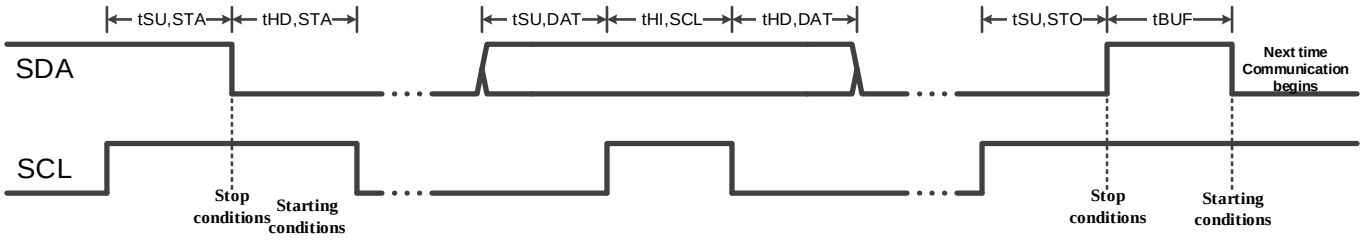



Figure 11 I²C Bus Controller Timing Diagram

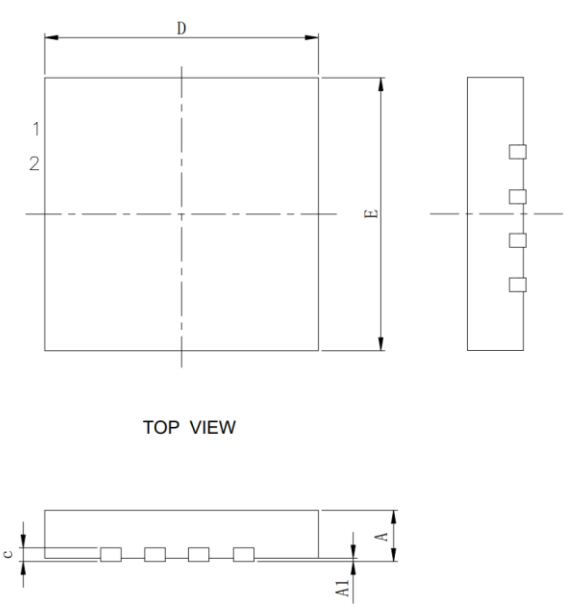
The GX28E17 supports clock stretching functionality in the I²C bus. The slave device can pause the current I²C communication by pulling down the SCL line and resume communication when it releases SCL by setting it high. This feature is primarily applicable in the following two scenarios:

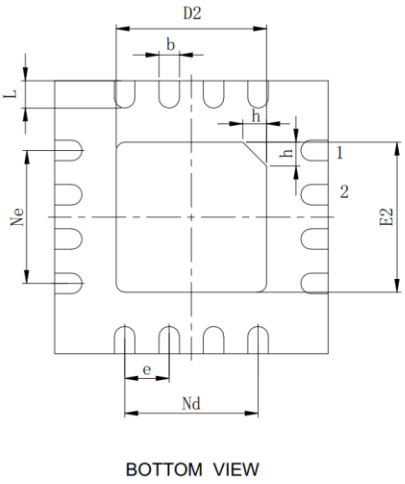
At the byte level, the slave device may require more time to store received bytes or prepare the bytes to be sent, even though it supports faster data byte reception rates. The slave device can pull down SCL after acknowledging a byte (ACK), forcing the GX28E17 or other devices to wait until the slave device is ready before starting the transmission of the next byte.

At the bit level, the slave device (e.g., hardware-limited MCUs) may not support receiving data bytes at faster rates. In such cases, the slave device can slow down the overall bus communication frequency by extending the low-level width of each SCL clock pulse. The GX28E17 adapts to the I²C working rate of such slave devices.

# Packaging Information

## Package Outline (TQFN-16)

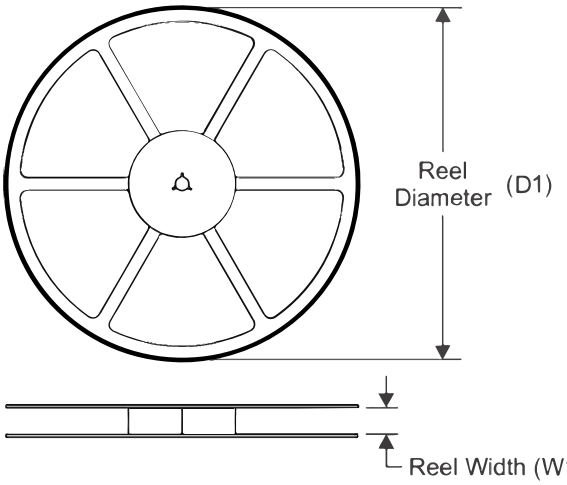


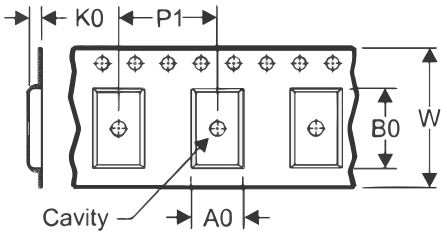

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | — | 0.02 | 0.05 |
| b | 0.25 | 0.30 | 0.35 |
| c | 0.18 | 0.20 | 0.25 |
| D | 3.90 | 4.00 | 4.10 |
| D2 | 2.10 | 2.20 | 2.30 |
| e | 0.65BSC | | |
| Ne | 1.95BSC | | |
| Nd | 1.95BSC | | |
| E | 3.90 | 4.00 | 4.10 |
| E2 | 2.10 | 2.20 | 2.30 |
| L | 0.35 | 0.40 | 0.45 |
| h | 0.30 | 0.35 | 0.40 |
| L/F载体尺寸 | 110*110 | | |

## Tape and Reel Information

REEL DIMENSIONS

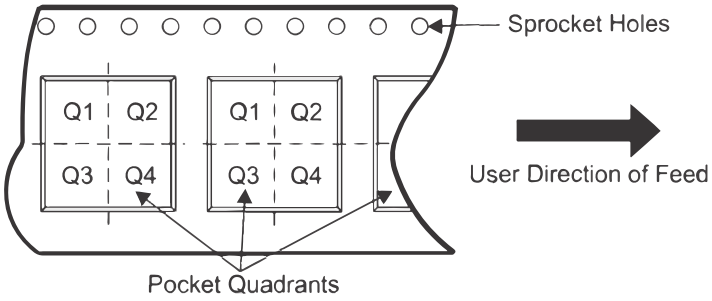



TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




| PACKAGE | D1 (mm) | W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 |
|---|---|---|---|---|---|---|---|---|
| TQFN (16) | 329 | 12.4 | 4.25 | 4.25 | 0.95 | 8.00 | 12.00 | Q1 |

Note: All dimensions mentioned above are in millimeters.

## 订购信息

| ORDER CODE | DEVICE | PACKAGE | QUANTITY | NOTES |
|---|---|---|---|---|
| GX28E17Q-T&R | GX28E17Q | TQFN (16) | 4000 | Tape&Reel |