Application Note: SQ24026

5.5V, Low $R_{DS(ON)}$ Dual-Channel 6A Load Switch

General Description

SQ24026 is a dual-channel 6A load switch. Extremely low $R_{DS(ON)}$ of the integrated two N-channel FETs help to reduce power loss during the normal operation. Programmable soft-start time controls the slew rate of the output voltage during start-up and minimizes the inrush current. Independent enable control allows the complicated system sequencing control. Integrated a discharge resistor for quick output discharge when switch turns off.

SQ24026 along with a small DFN3×2-14 package provides small PCB area application and better thermal performance.

Features

- Wide Input Voltage Range from 0.8V to 5.5V
- Dual-channel 6A Load Switch
- Low Bias Current:
  - 20μA Typical (Both Channels)
  - 18μA Typical (Single Channel)
- Extremely Low $R_{DS(ON)}$ for the Integrated Switch: 18mΩ (V_{BIAS}=5V)
- Programmable Soft-start Time
- Compact Package: DFN3×2-14

Applications

- Notebook PC or Tablet PC or Net PC
- Desktop PC
- Server
- Set Top Box
- E-Book or MID
- Smart TV
- Router
- Industrial PC
- Solid-state Drives (SSD)

Ordering Information

SQ24026 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SQ24026DUC	DFN3×2-14	

Typical Applications

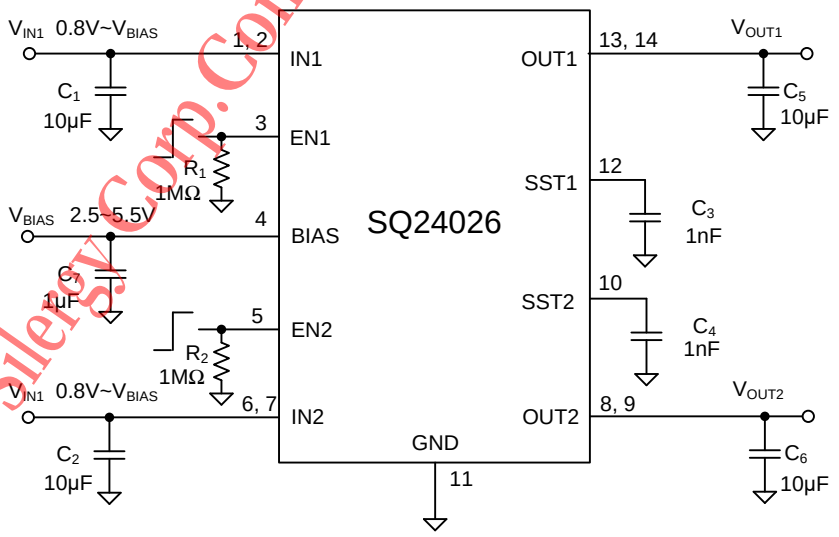
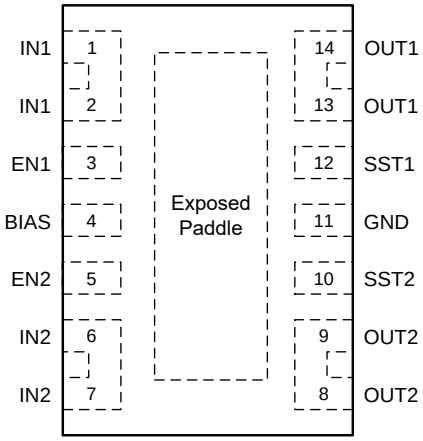


Figure1. Schematic Diagram

Pinout (top view)



(DFN3×2-14)

Top mark: **6Q*xyz*** for SQ24026DUC (Device code: 6Q, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
IN1	1,2	Power input pin for channel 1.
EN1	3	Enable control input for channel 1. Pull it High to enable the channel 1. Do not leave it floating.
BIAS	4	Bias pin. Bias supply for overdriving the gate of the pass switch between input and output. Recommended the BIAS voltage range is 2.5V to 5.5V.
EN2	5	Enable control input for channel 2. Pull it High to enable the channel 2. Do not leave it floating.
IN2	6,7	Power input pin for channel 2.
OUT2	8,9	Power output pin for channel 2.
SST2	10	Soft Start pin of the channel 2. Connect a capacitor from this pin to ground for slew rate programming. Can be floating.
GND	11	Ground pin.
SST1	12	Soft Start pin of the channel 1. Connect a capacitor from this pin to ground for slew rate programming. Can be floating.
OUT1	13,14	Power output pin for channel 1.
Thermal Pad	Exposed paddle	Thermal pad, tie to GND.

Block Diagram

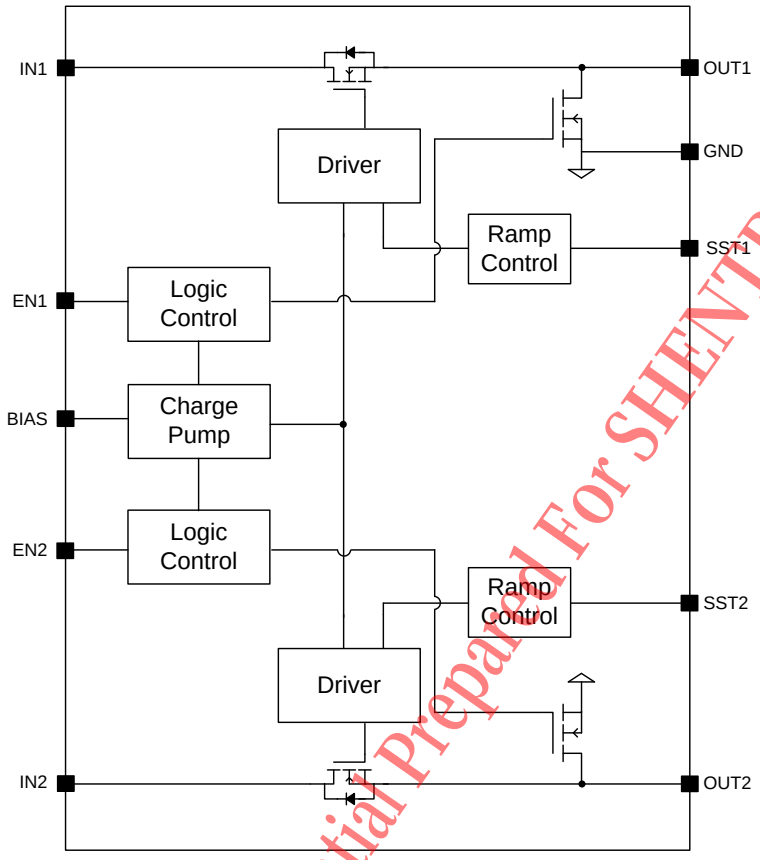


Figure2. Block Diagram

Absolute Maximum Ratings (Note 1)

IN1, IN2, OUT1, OUT2 ---------- -0.3V to 6V
SST1, SST2 ---------- -0.3V to OUT+6V
EN1, EN2, BIAS ---------- -0.3V to 6V
Power Dissipation, P_D @ T_A = 25°C, DFN3×2-14 ---------- 1.9W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 52.3°C/W
θ_{JC} ---------- 11.5°C/W
Junction Temperature Range ---------- -40°C to 125°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

IN1, IN2, OUT1, OUT2 ---------- 0.8V to V_{BIAS}
EN1, EN2 ---------- 0V to V_{BIAS}
BIAS ---------- 2.5V to 5.5V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} =V_{BIAS}= 5V, T_J = -40°C to +125°C. Typical values are at T_J = 25°C, unless otherwise specified. The values are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Test Conditions			Min	Typ	Max	Unit
Input Voltage Range	$V_{IN1,2}$				0.8		V_{BIAS}	V
BIAS Voltage Range	V_{BIAS}				2.5		5.5	V
BIAS Quiescent Current (Single Channel)	$I_{Q\_BIAS\_1}$	V_{BIAS}= $V_{IN1,2}$=V_{EN1}=5V, V_{EN2}=0V, $I_{OUT1,2}$=0A, -40°C<T_A<85°C				18	29	μA
		V_{BIAS}= $V_{IN1,2}$=V_{EN1}=2.5V, V_{EN2}=0V, $I_{OUT1,2}$=0A, -40°C<T_A<85°C				7	14	
BIAS Quiescent Current (Both Channels)	$I_{Q\_BIAS\_2}$	V_{BIAS}= $V_{IN1,2}$=$V_{EN1,2}$=5V, $I_{OUT1,2}$=0A, -40°C<T_A<85°C				20	30	μA
		V_{BIAS}= $V_{IN1,2}$=$V_{EN1,2}$=2.5V, $I_{OUT1,2}$=0A, -40°C<T_A<85°C				8	15	
BIAS Shutdown Current	I_{SHD_BIAS}	$V_{EN1,2}$=0V,$V_{OUT1,2}$=0V					2	μA
Input Shutdown Current (per Channel)	I_{SHD_IN}	$V_{EN1,2}$=0V, $V_{OUT1,2}$=0V	V_{BIAS}=5V	V_{IN}=5V		0.5	8	μA
				V_{IN}=3.3V		0.1	3	
				V_{IN}=1.8V		0.07	2	
				V_{IN}=0.8V		0.04	1	
			V_{BIAS}=2.5V	V_{IN}=2.5V		0.13	3	
				V_{IN}=1.8V		0.07	2	
				V_{IN}=1.2V		0.05	2	
				V_{IN}=0.8V		0.04	1	
Integrate FET RON (per Channel)	$R_{DS(ON)}$	V_{BIAS}=5V, V_{IN}=0.8V to 5V, I_{out}=200mA, T_A=25°C				18	25	mΩ
		V_{BIAS}=5V, V_{IN}=0.8V to 5V, I_{out}=200mA, -40°C <T_A<85°C				18	27	
		V_{BIAS}=3.3V,V_{IN}=0.8V to 3.3V, I_{out}=200mA, T_A=25°C				20	27	
		V_{BIAS}=3.3V,V_{IN}=0.8V to 3.3V, I_{out}=200mA, -40°C <T_A<85°C				20	30	
EN Turn-on Threshold	V_{EN_ON}				1.2			V
EN Turn-off Threshold	V_{EN_OFF}						0.4	V
Output Discharge Resistor	R_{DIS}					190	270	Ω
Output Voltage Rise Time	t_{RISE}	R_L=10Ω, C_L=0.1μF, C_{SST}=1nF, V_{EN}=5V	V_{IN}= V_{BIAS} =5V		1030	1750	2850	μs
			V_{IN}= 0.8V,V_{BIAS}=5V		185	365	570	
			V_{IN}= V_{BIAS} =2.5V		1310	2275	3550	
			V_{IN}=0.8V,V_{BIAS}=2.5V		450	825	1280	
Output Voltage Fall Time	t_{FALL}	R_L=10Ω, C_L=0.1μF, C_{SST}=1nF, V_{EN}=5V	V_{IN}= V_{BIAS} =5V		0.1	2	4	μs
			V_{IN}= 0.8V,V_{BIAS}=5V		0.1	2	4	
			V_{IN}= V_{BIAS} =2.5V		0.1	2	4	
			V_{IN}=0.8V,V_{BIAS}=2.5V		0.1	2	4	
Turn On Delay Time	t_{D_ON}	R_L=10Ω, C_L=0.1μF, C_{SST}=1nF, V_{EN}=5V	V_{IN}= V_{BIAS} =5V		230	460	670	μs
			V_{IN}= 0.8V,V_{BIAS}=5V		140	290	435	
			V_{IN}= V_{BIAS} =2.5V		430	850	1910	
			V_{IN}=0.8V,V_{BIAS}=2.5V		320	650	1120	
Turn Off Delay Time	t_{D_OFF}	R_L=10Ω, C_L=0.1μF, C_{SST}=1nF, V_{EN}=5V	V_{IN}= V_{BIAS} =5V		1	6	12	μs
			V_{IN}= 0.8V,V_{BIAS}=5V		1	6	12	
			V_{IN}= V_{BIAS} =2.5V		5	15	25	
			V_{IN}=0.8V,V_{BIAS}=2.5V		5	15	25	

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Device is mounted on a 2x2 FR-4 substrate PCB, 2OZ copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Exposed pad of DFN3×2-14 packages is the case position for θ_{JC} measurement.

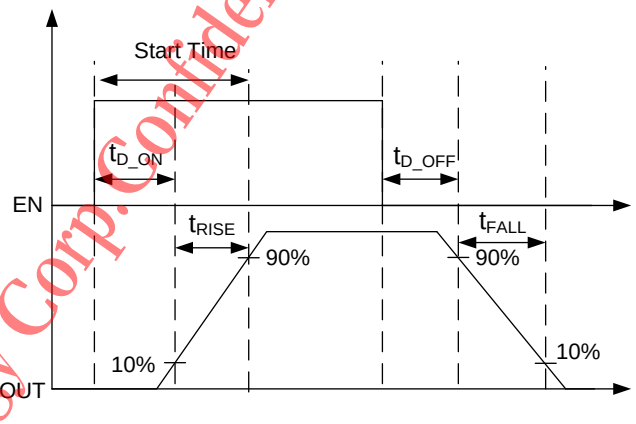
Note 3: The device is not guaranteed to function outside its operating conditions.

Note4. Recommended Soft-start Time Program Table

Condition: RISE TIME (μs) 10% - 90%, CL = 0.1μF, CIN = 1μF, RL = 10Ω, TYPICAL VALUES at 25°C, V_{BIAS} = 5V, 25V X7R 10% CERAMIC CAP, under different V_{IN}.					
SST cap (pF)	5V	3.3V	1.8V	1.5V	1.2V
0	210	154	104	93	81
220	555	385	231	209	178
470	1022	680	406	342	272
1000	1764	1208	714	616	488
2200	3808	2536	1450	1260	1024
4700	8200	5568	3192	2768	2296

Recommended Formula for C_{SST} & Soft-start slew rate Calculation:

$$\frac{dV}{dt} = \frac{2.56}{C_{SST}(pF) + 145(pF)} (V/us),$$

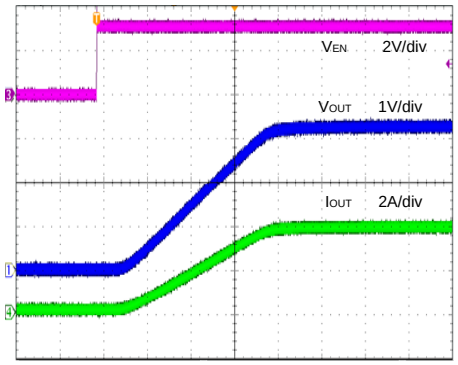


A capacitor to GND on the SSTx pins sets the slew rate for each channel. To ensure desired performance, a capacitor with a minimum voltage rating of 25 V should be used on the SSTx pin.
(The equation below accounts for 10% to 90% measurement on VOUT).

Typical Performance Characteristic

Startup from Enable

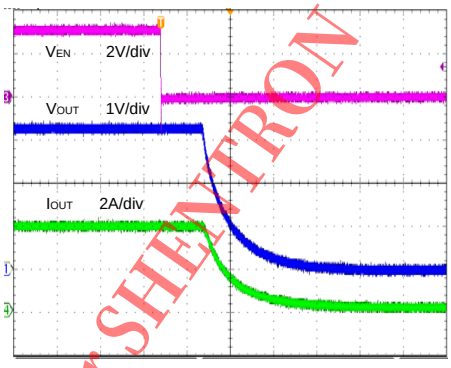
(VBIAS=VIN=3.3V, Io=4A)



Time (800μs/div)

Shutdown from Enable

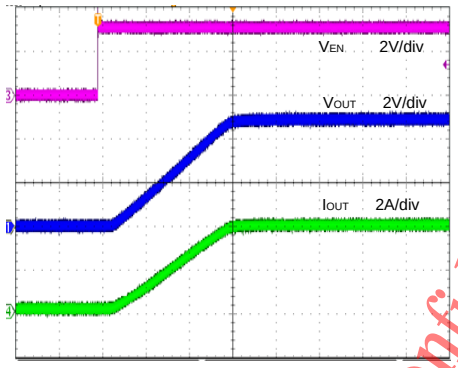
(VBIAS=VIN=3.3V, Io=4A)



Time (10μs/div)

Startup from Enable

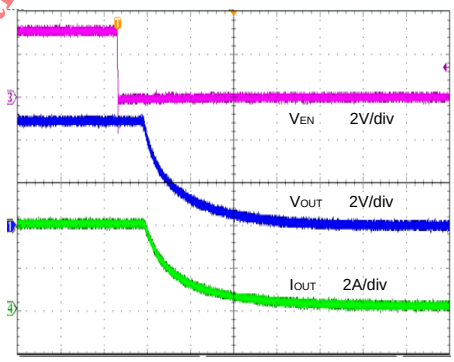
(VBIAS=VIN=5V, Io=4A)



Time (800μs/div)

Shutdown from Enable

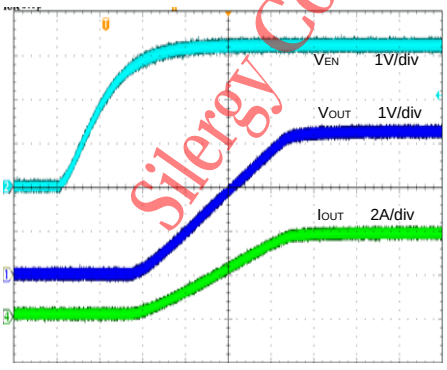
(VBIAS=VIN=3.3V, Io=4A)



Time (10μs/div)

Startup from BIAS

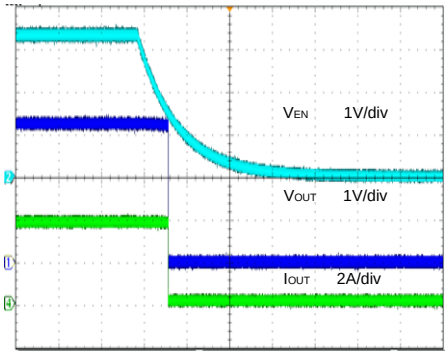
(VBIAS=VIN=3.3V, Io=4A)



Time (800μs/div)

Shutdown from BIAS

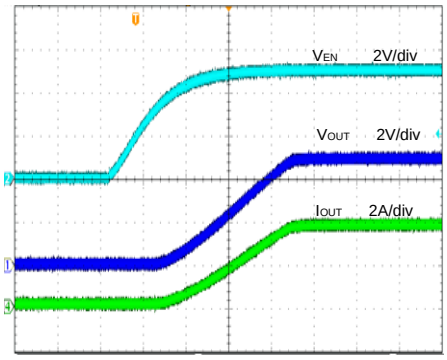
(VBIAS=VIN=3.3V, Io=4A)



Time (100ms/div)

Startup from BIAS

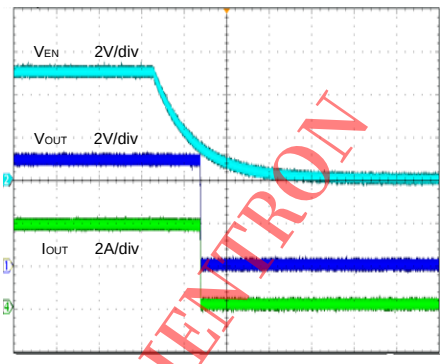
(VBIAS=VIN=5V, Io=4A)



Time (800μs/div)

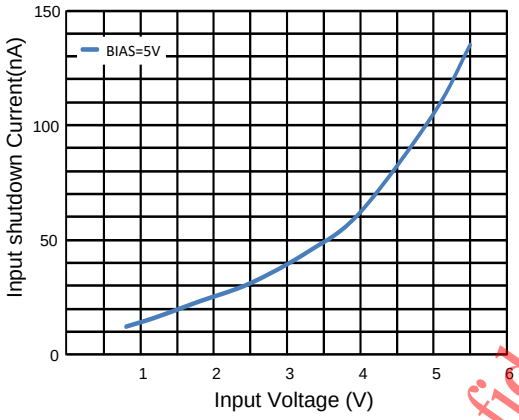
Shutdown from BIAS

(VBIAS=VIN=5V, Io=4A)

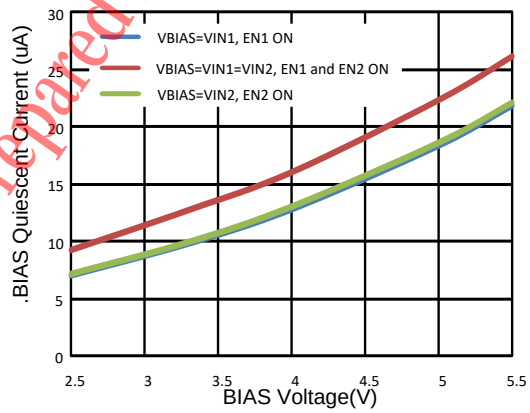


Time (100ms/div)

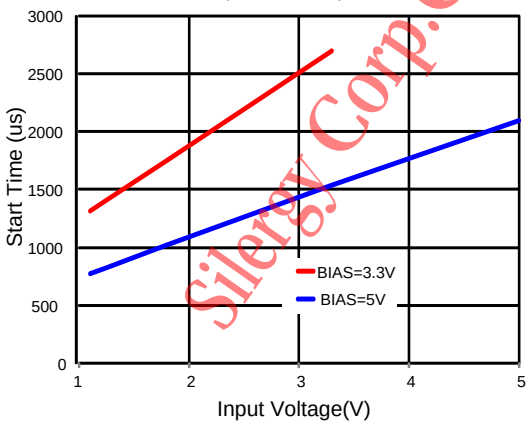
Input shutdown Current(per Channel) vs. Input Voltage



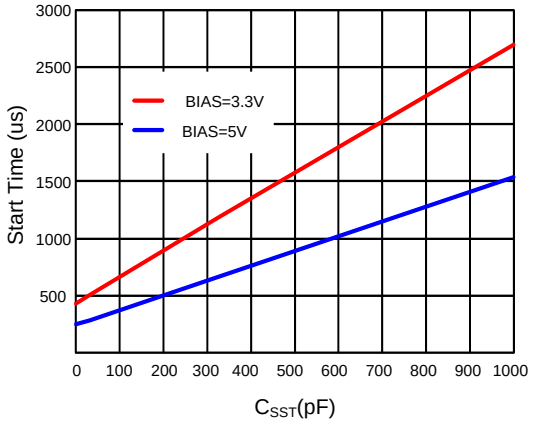
BIAS Quiescent Current vs. BIAS Voltage

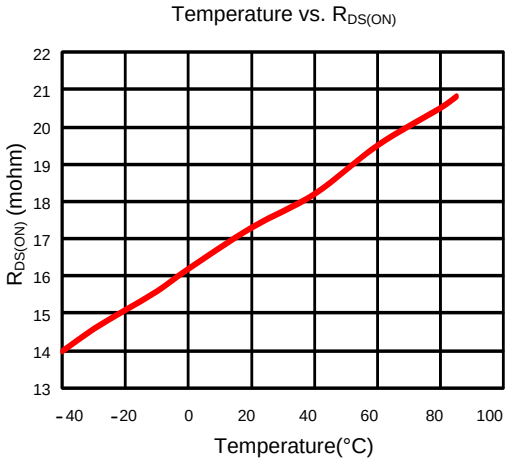


Start Time Vs. Input Voltage (C_{SST}=NULL)



Start Time vs. CT (V_{IN}=3.3V)





Applications Information

Operation

SQ24026 is a dual-channel 6A load switch. Extremely low $R_{DS(ON)}$ of the integrated two N-channel FETs help to reduce power loss during the normal operation. Programmable soft-start time controls the slew rate of the output voltage during start-up and minimizes the inrush current. Independent enable control allows the complicated system sequencing control. Integrated a discharge resistor for quick output discharge when switch turns off.

SQ24026 along with a small DFN3×2-14 package provides small PCB area application and better thermal performance.

EN ON/OFF Control

The EN pins control the state of the switches. Asserting EN high enables the switch. EN is active high and has a low threshold, making it capable of interfacing with low-voltage signals. This pin cannot be left floating and must be tied either high or low for proper functionality.

Input Capacitor

For most applications, bypass INx to GND with a 10μF ceramic capacitor as close as possible to the device. If the power source has significant inductance due to long lead length, the input capacitor clamps the overshoot due to LC tank circuit.

V_{IN} and V_{BIAS} Voltage Range

For optimal R_{ON} performance, make sure $V_{IN} \leq V_{BIAS}$. The device will still be functional if $V_{IN} > V_{BIAS}$ but the R_{ON} may exceed typical value listed in Electrical Characteristics.

Soft-start Time Program

Connect a capacitor from SST pins to GND to control the slew rate of the output voltage at power-on. This pin can be left floating to obtain a predetermined slew rate (minimum T_{SST}) on the output. Equation governing soft start time is shown below:

$$SR_{OUT} = \frac{2.56}{C_{SST}(pF)+145(pF)}(v/\mu s)$$

$$t_{RISE} = 0.8 \times \frac{V_{IN}}{SR_{OUT}}(\mu s)$$

PCB Layout Guide

For best performance of the SQ24026, the following guidelines must be strictly followed:

1) Keep all power trace as short and wide as possible. And it is desirable to use 2-layer or 4-layer board for thermal performance and better capability of current flow. At least 6 vias are suggested to put around each power pin to distribute current to different PCB layer. These power pins include VIN and OUT.

2) Place input/output and BIAS capacitor close to the IC for better transient performance.

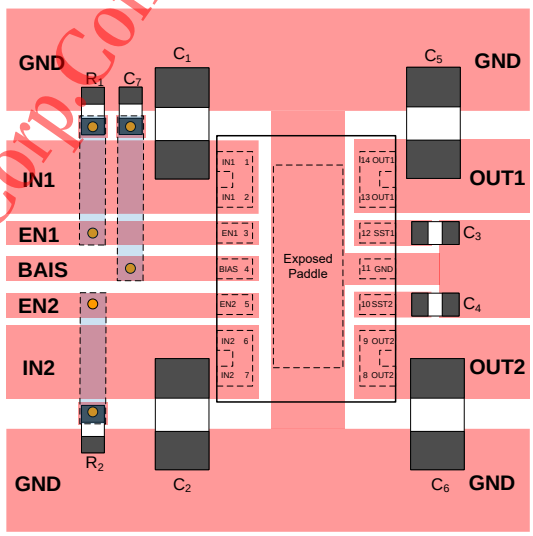
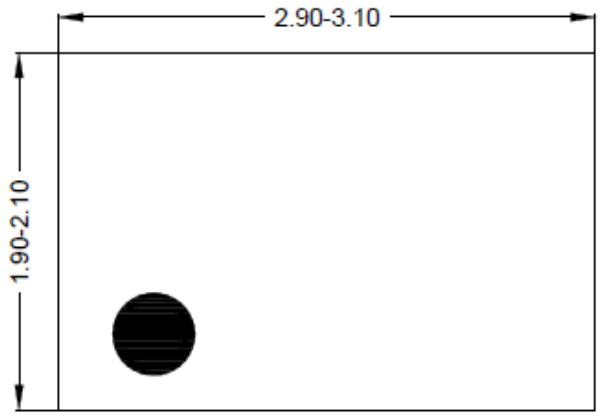
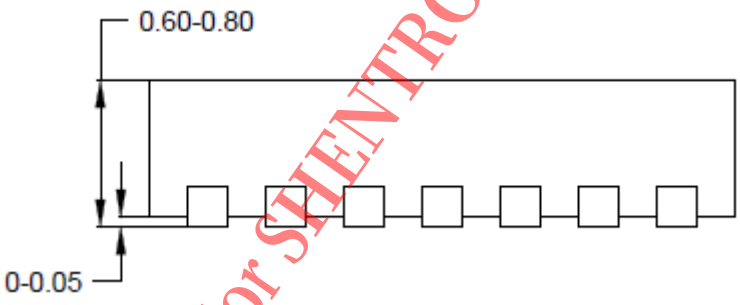


Figure3. PCB Layout Suggestion

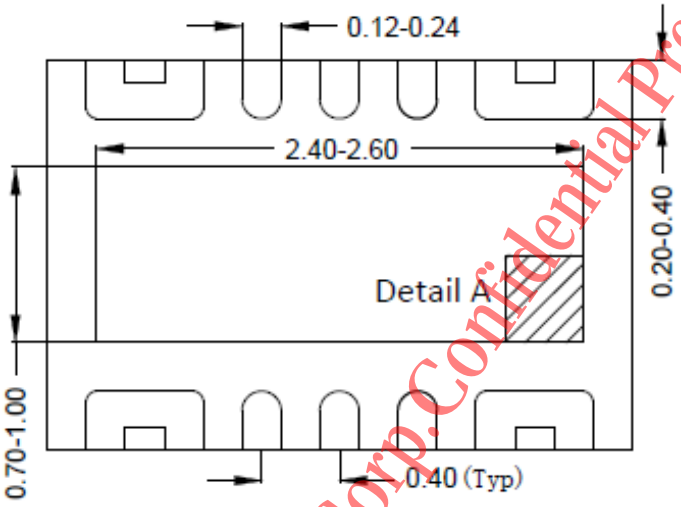
DFN3×2-14 Package Outline Drawing



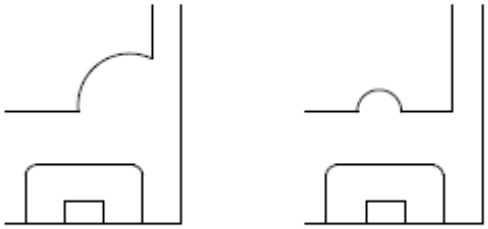
Top View



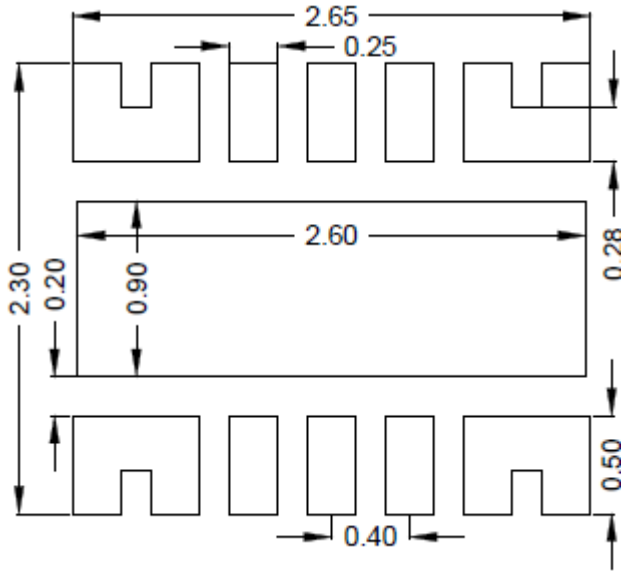
Side View



Bottom View



Detail A
Pin1 Identifier: two options



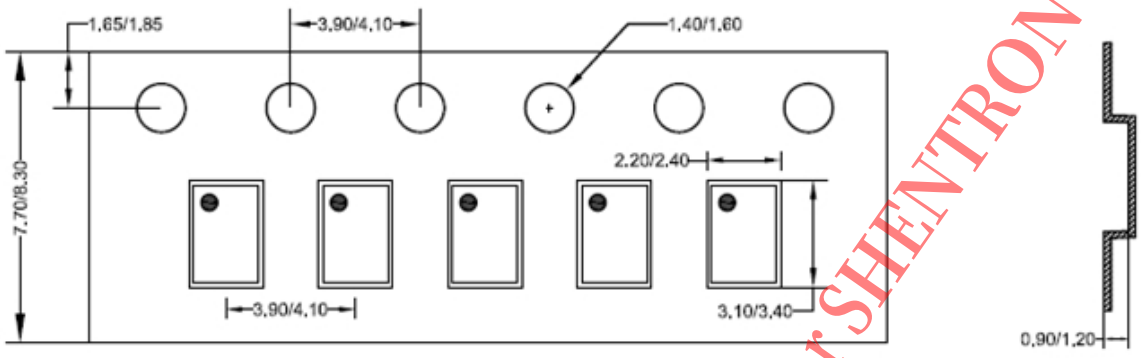
Recommended PCB layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

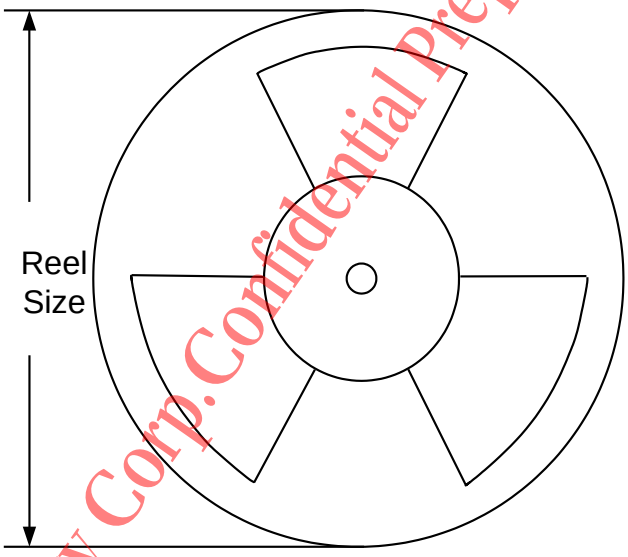
1. Taping orientation

DFN3×2



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel (pcs)
DFN3×2-14	8	4	7"	400	160	3000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Dec.28, 2021	Revision 0.9A	Update the taping spec (Pin 1 is on the upper left.)
Jan.15, 2021	Revision 0.9	Initial Release

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