1. Features

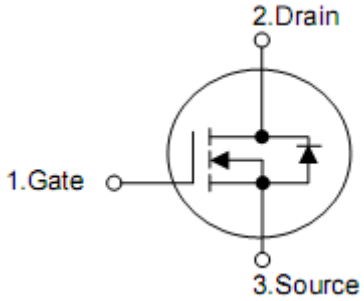
- SGT MOSFET technology
- Proprietary New Trench Technology
- $R_{DS(ON)}$=18.5mΩ(typ.)@V_{GS}=10V
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

2. Applications

- Hard Switching and High Speed Circuit
- Motor Control
- UPS

3. Pin configuration

TO-220



Pin	Function
1	Gate
2	Drain
3	Source

4. Ordering Information

Part Number	Package	Brand
KCP3525A	TO-220	KIA

5. Absolute maximum ratings

T_C= 25 ºC, unless otherwise specified

Parameter		Symbol	Ratings	Unit
Drain-to-Source Voltage [1]		V_{DSS}	250	V
Gate-to-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current	Tc=25 ºC	I_D	70	A
	Tc=100 ºC	I_D	48	A
Pulsed Drain Current at V_{GS}=10V [2]		I_{DM}	280	A
Single Pulse Avalanche Energy L=10mH		EAS	2000	mJ
Peak Diode Recovery dv/dt		dv/dt	5.0	V/ns
Power Dissipation		P_D	250	W
Derating Factor above 25°C		P_D	2	W/°C
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds		T_L T_{PAK}	300 260	ºC
Operating and Storage Temperature Range		T_J&T_{STG}	-55 to 150	ºC

Caution: Stresses greater than those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device.

6. Thermal characteristics

Parameter	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.5	ºC/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62	° C/W

7. Electrical characteristics

T_J=25°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	250	-	-	V
Drain-to-Source Leakage Current	I_{DSS}	V_{DS}=250V, V_{GS}=0V	-	-	1	uA
		V_{DS}=200V,T_J=125°C	-	-	100	uA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain-to-Source ON Resistance [3]	$R_{DS(ON)}$	V_{GS}=10V, I_D=35A	-	18.5	20	mΩ
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=250uA	2.5	-	4.5	V
Input Capacitance	C_{iss}	V_{GS}=0V,V_{DS}=125V, f=1.0MHZ	-	6850	-	pF
Reverse Transfer Capacitance	C_{rss}		-	5	-	
Output Capacitance	C_{oss}		-	320	-	
Total Gate Charge	Q_g	V_{DD}=125V,I_D=40A, V_{GS}=10V	-	78	-	nC
Gate-to-Source Charge	Q_{gs}		-	34	-	
Gate-to-Drain (Miller) Charge	Q_{gd}		-	10	-	
Turn-on Delay Time	$t_{d(ON)}$	V_{DD}=125V, I_D=40A, R_G=4.7Ω,V_{GS}= 10V	-	36	-	nS
Rise Time	t_{rise}		-	15	-	
Turn-Off Delay Time	$t_{d(OFF)}$		-	42	-	
Fall Time	t_{fall}		-	10	-	
Continuous Source Current	I_{SD}	Integral PN-diode in MOSFET	-	-	70	A
Pulsed Source Current	I_{SM}		-	-	280	A
Forward Voltage	V_{SD}	I_S=50A, V_{GS}=0V	-	-	1.2	V
Reverse recovery time	t_{rr}	I_F=40A, diF/dt=100A/μs	-	232	-	ns
Reverse recovery charge	Q_{rr}		-	991	-	uC

Note:
1) T_J=+25°C to +150°C
2) Repetitive rating; pulse width limited by maximum junction temperature.
3) Pulse width≤380μs; duty cycle≤2%.

8. Test circuits and waveforms

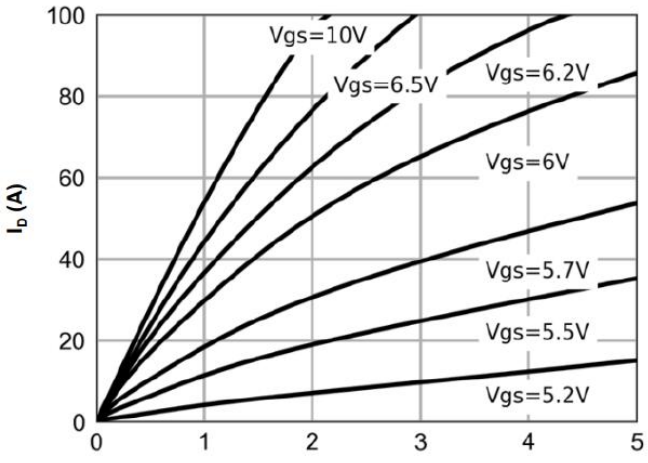


Figure 1: On-Region Characteristics

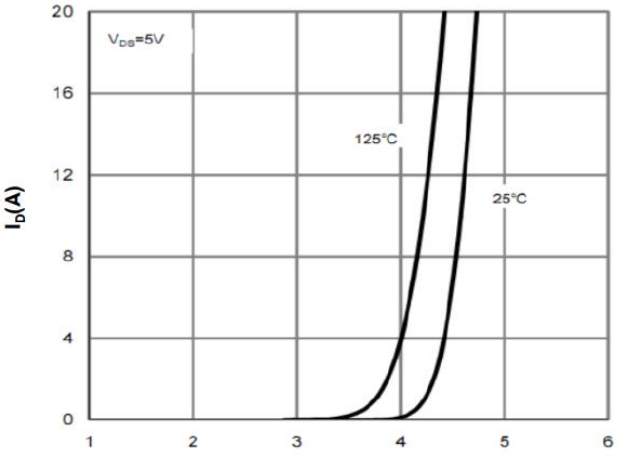


Figure 2: Transfer Characteristics

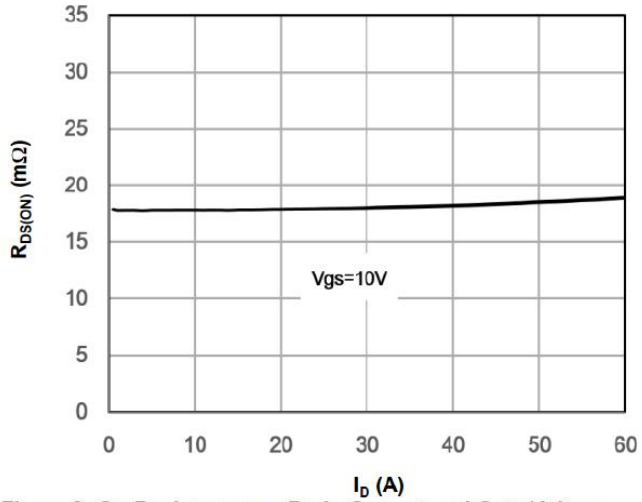


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

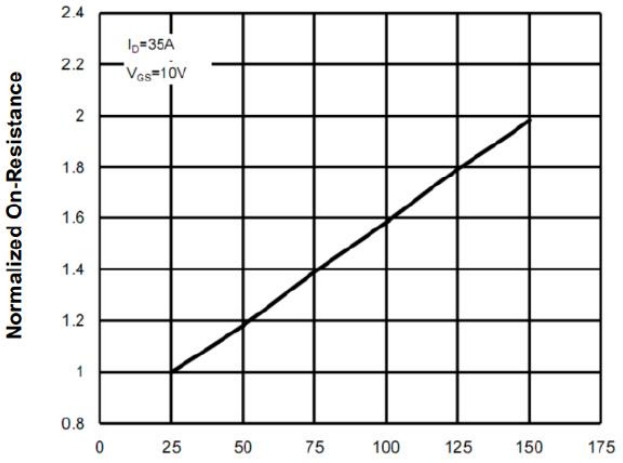


Figure 4: On-Resistance vs. Junction Temperature

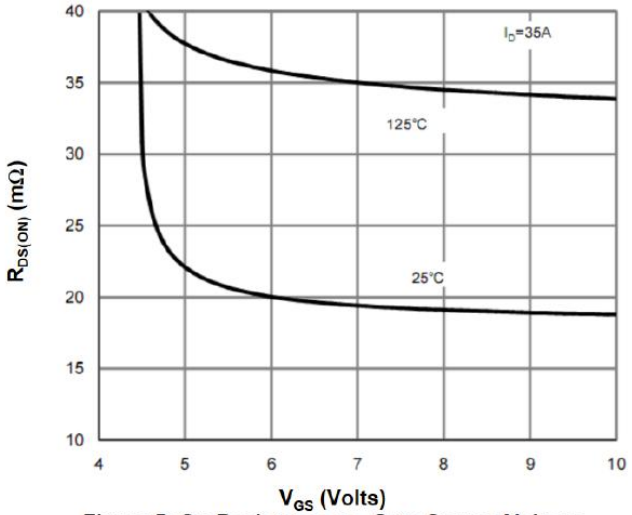


Figure 5: On-Resistance vs. Gate-Source Voltage

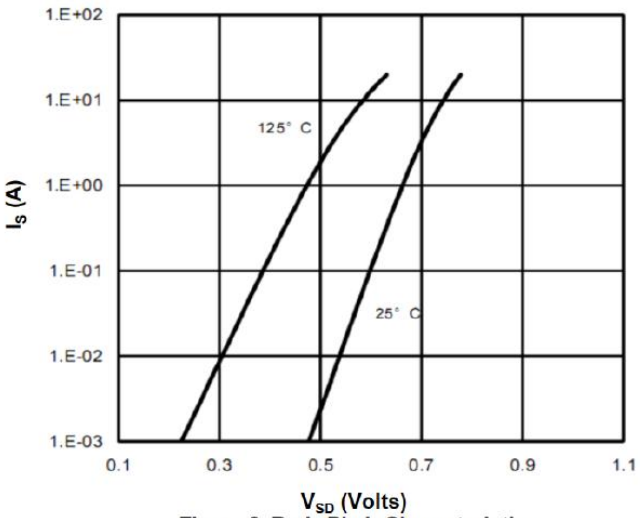


Figure 6: Body-Diode Characteristics

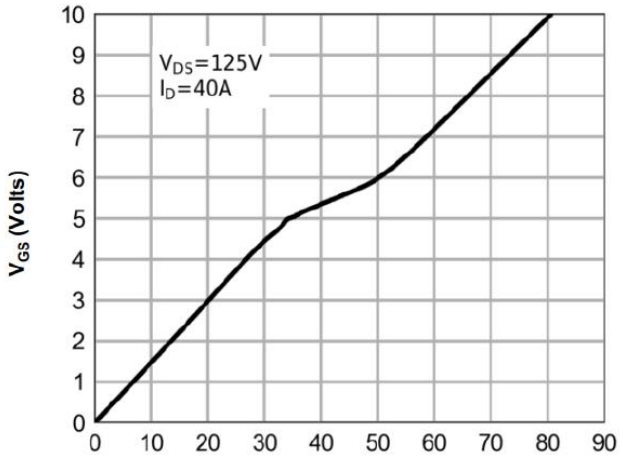


Figure 7: Gate-Charge Characteristics

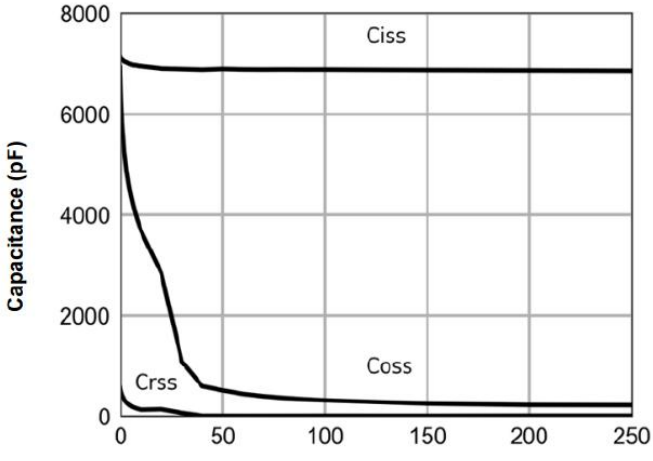


Figure 8: Capacitance Characteristics

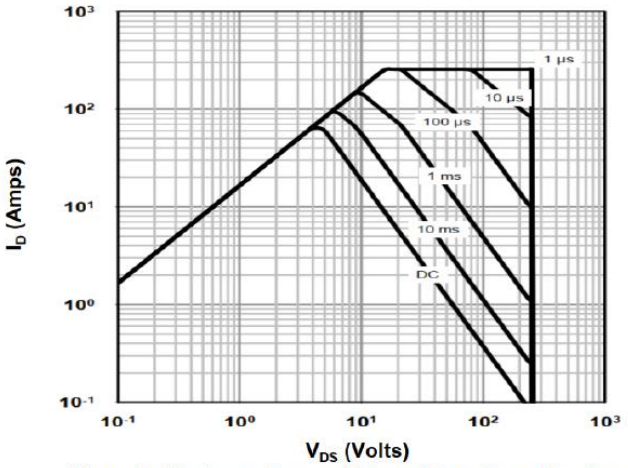


Figure 9: Maximum Forward Biased Safe Operating Area

9. Test Circuits and Waveforms

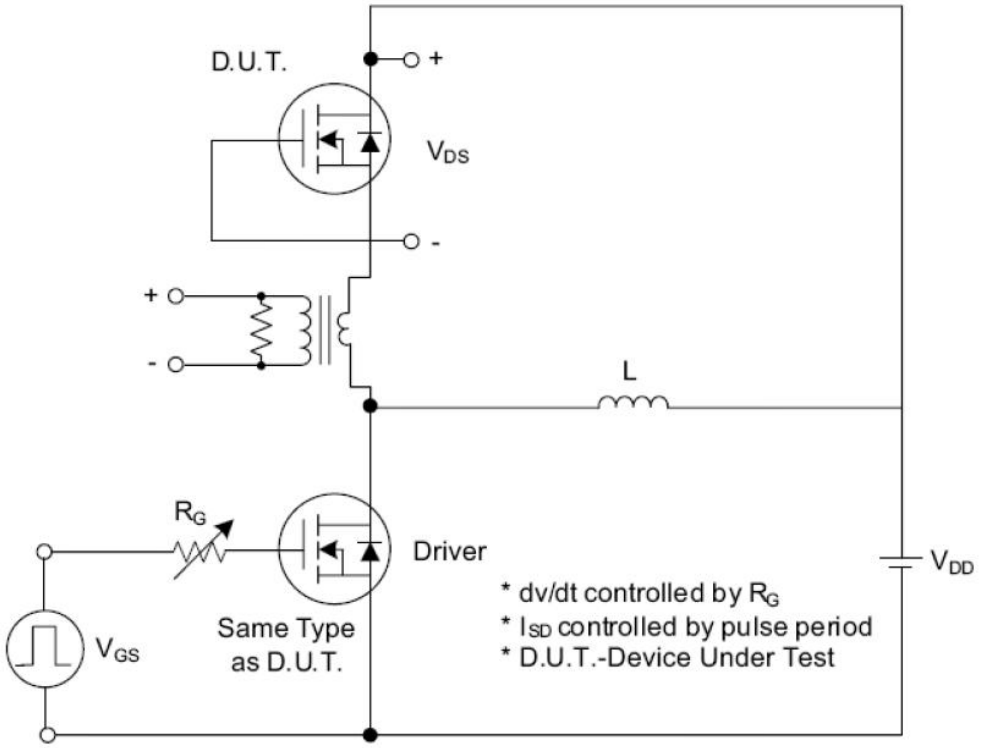


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

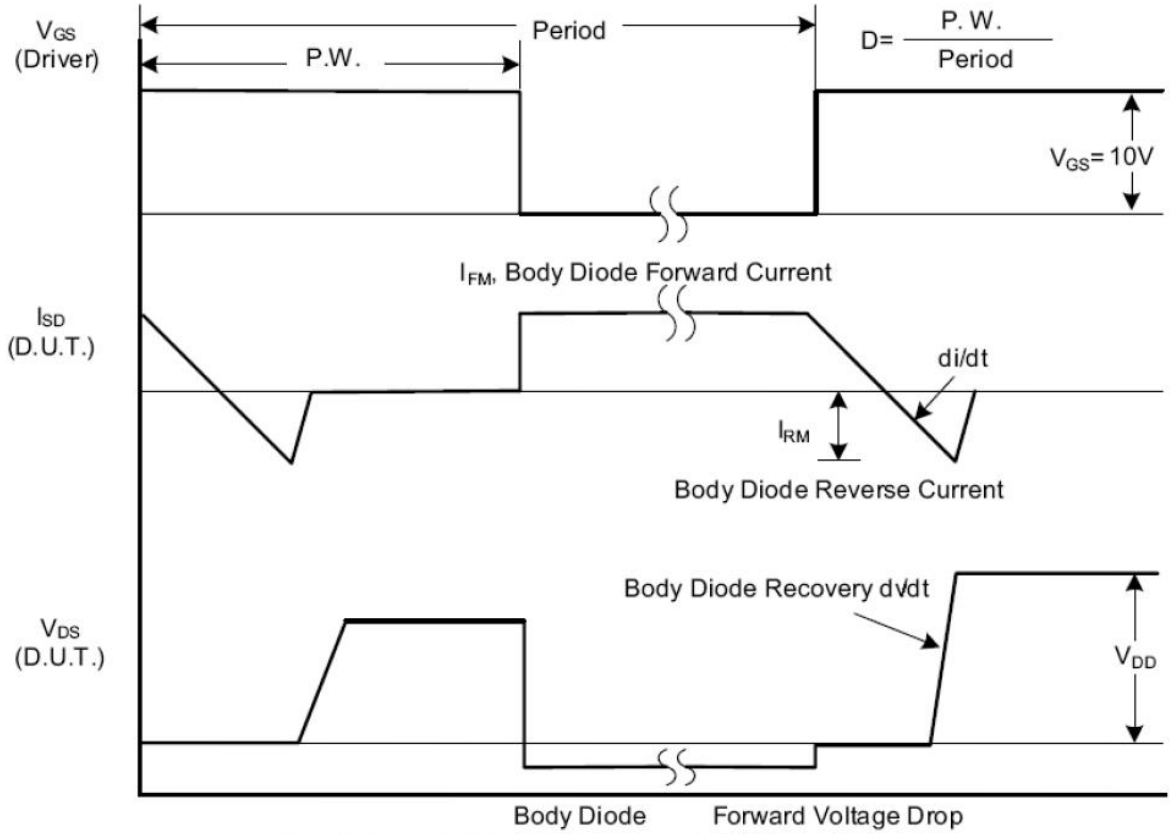


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

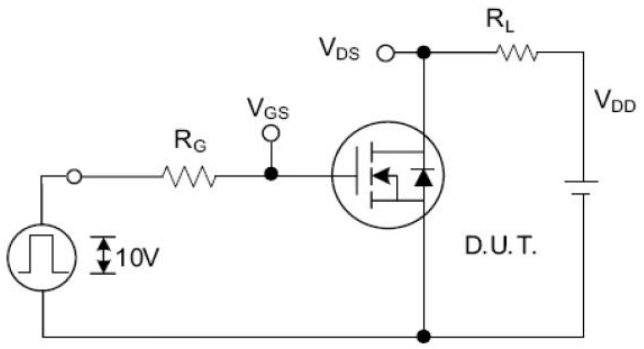


Fig. 2.1 Switching Test Circuit

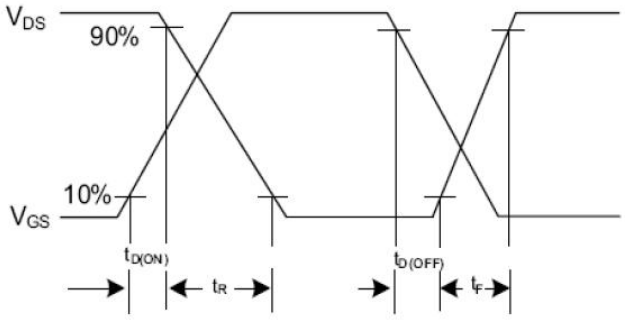


Fig. 2.2 Switching Waveforms

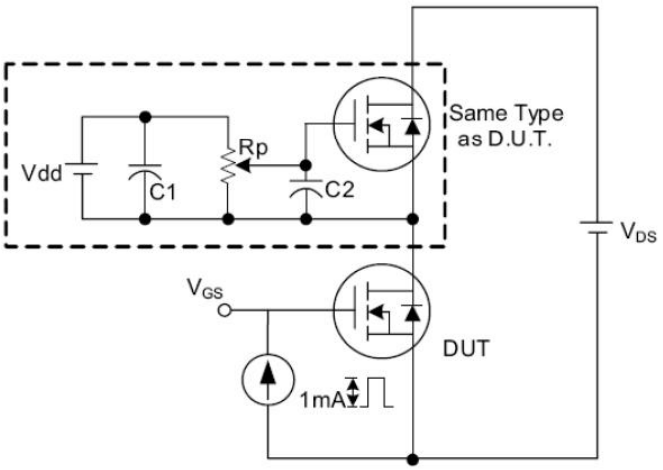


Fig. 3 . 1 Gate Charge Test Circuit

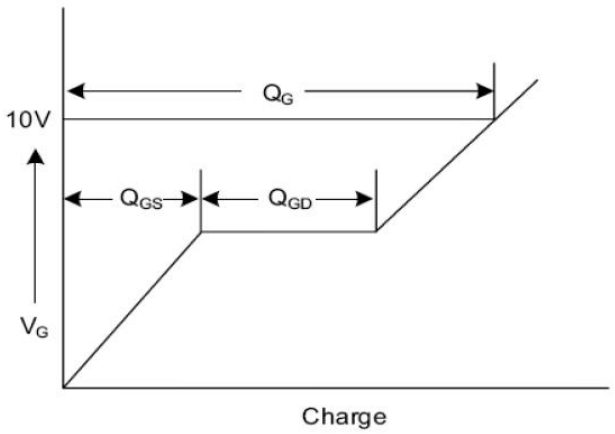


Fig. 3 . 2 Gate Charge Waveform

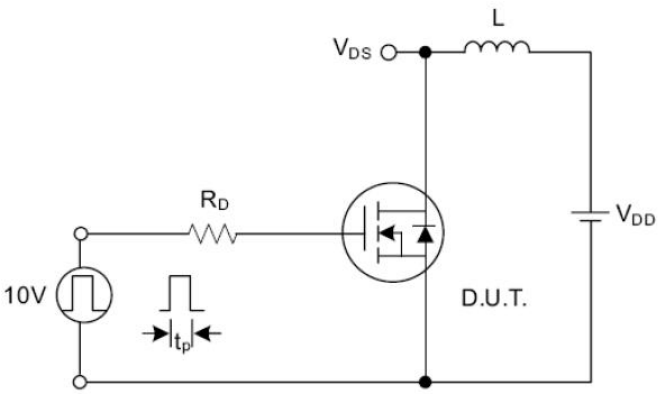


Fig. 4.1 Unclamped Inductive Switching Test Circuit

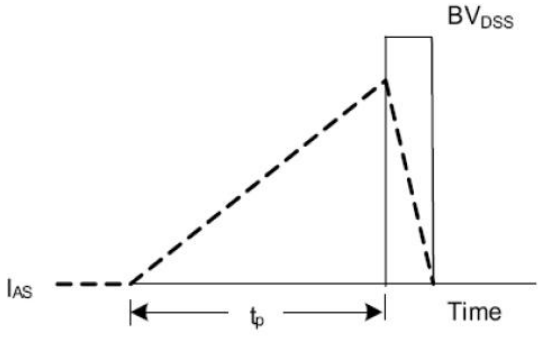


Fig. 4.2 Unclamped Inductive Switching Waveforms