1. Features

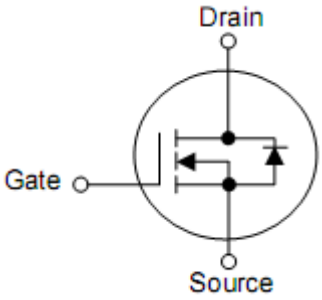
- Uses advanced SGT technology
- Device Rating V_{DS}=40V, I_D=260A
- $R_{DS(ON)}$=1.1mΩ (typ.) @ V_{GS}=10V
- Proprietary High Density Trench Technology
- RoHS Compliant & Halogen-Free

2. Application

- Battery Management System
- Load Switch
- Brushless DC Motor Control

3. Pin configuration

TOLL-8



Pin	Function
1	Gate
9	Drain
2,3,4,5,6,7,8	Source

4. Ordering Information

Part Number	Package	Brand
KCT1704A	TOLL-8	KIA

5. Absolute maximum ratings

T_C=25 ºC unless otherwise specified

Parameter		Symbol	Ratings	Unit
Drain-to-Source Voltage		V_{DS}	40	V
Gate-Source voltage		V_{GS}	±20	V
Continuous Drain Current, V_{GS}@10V [1]	T_C=25 ºC	I_D	260	A
	T_C=100 ºC	I_D	169	A
Pulsed Drain Current [2]		I_{DM}	1052	A
Power Dissipation [4]	T_C=25 ºC	P_D	164	W
Power Dissipation	T_C=100 ºC	P_D	2.55	W
Single Pulsed Avalanche Energy [3]		E_{AS}	551	mJ
Junction & Storage Temperature Range		T_J& T_{STG}	-55 to 150	ºC

6. Thermal characteristics

Parameter	Symbol	Ratings	Units
Thermal resistance, Junction-case [1]	$R_{\theta JC}$	0.76	ºC/W
Junction-to-Ambient (mounted on 1 inch square PCB)	$R_{\theta JA}$	49	ºC/W

7. Electrical characteristics

(T_C=25°C, unless otherwise notes)

Parameter	Symbol	Test Condition	Value			Unit
			min.	typ.	max.	
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	40	-	-	V
Zero gate voltage drain current	I_{DSS}	V_{DS}=40V,V_{GS}=0V	-	-	1	μA
		V_{DS}=40V, T_C=55°C	-	-	100	μA
Gate-source leakage current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	1.0	-	2.4	V
Drain-source on-state resistance 2)	$R_{DS(on)}$	V_{GS}=10V, I_D=60A	-	1.1	1.6	mΩ
		V_{GS}=4.5V, I_D=20A	-	1.43	-	mΩ
Transconductance	g_{fs}	V_{DS}=5V,I_D=50A	-	225	-	S
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=20V, f=100KHz	-	8200	-	pF
Output Capacitance	C_{oss}		-	1500	-	
Reverse Transfer Capacitance	C_{rss}		-	1450	-	
Gate Total Charge	Q_g	V_{GS}=10V, V_{DS}=20V, I_D=50A	-	210	-	nC
Gate-Source charge	Q_{gs}		-	22	-	
Gate-Drain charge	Q_{gd}		-	75	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=20V, I_D=50A, V_{GS}=10V, R_G=5Ω	-	50	-	ns
Rise time	tr		-	175	-	
Turn-off delay time	$t_{d(off)}$		-	300	-	
Fall time	t_f		-	250	-	
Gate resistance	R_G	—	-	0.7	-	Ω
Maximum Continuous Drain to Source Diode Forward Current 1),5)	I_S	—	-	188	-	A
Maximum Pulsed Drain to Source Diode Forward Current 2),5)	I_{SM}	—	-	1052	-	A
Body Diode Forward Voltage	V_{SD} 2)	V_{GS}=0V, I_S=50A T_J=25°C	-	0.78	-	V

Note:
1) The data tested by surface mounted on one inch2 FR-4 board with 2OZ copper.
2) The data tested by pulsed, pulse width≤300us, duty cycle≤2%.
3) The EAS data shows Max. rating. The test condition is V_{DD}=25V, V_{GS}=10V, R_g=25Ω, L=0.1mH, I_{AS}=104.98A.
4) The power dissipation is limited by 150°C junction temperature.
5) The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

8. Typical Characteristics

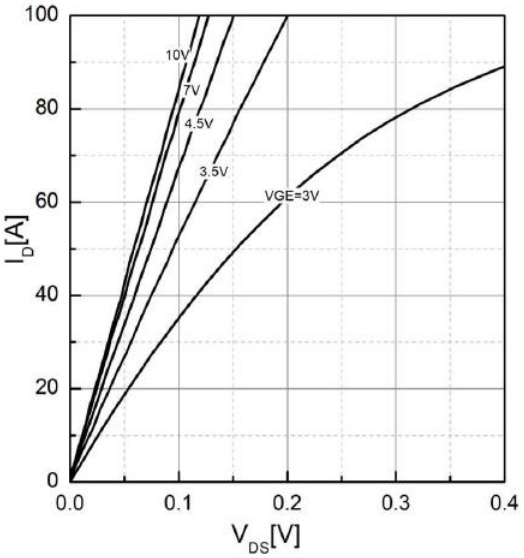


Figure 1. Output Characteristics TJ=25℃

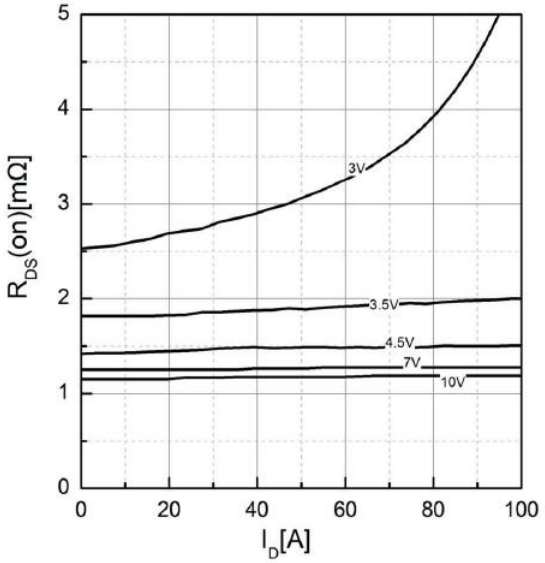


Figure 2. Drain-source on resistance TJ=25℃

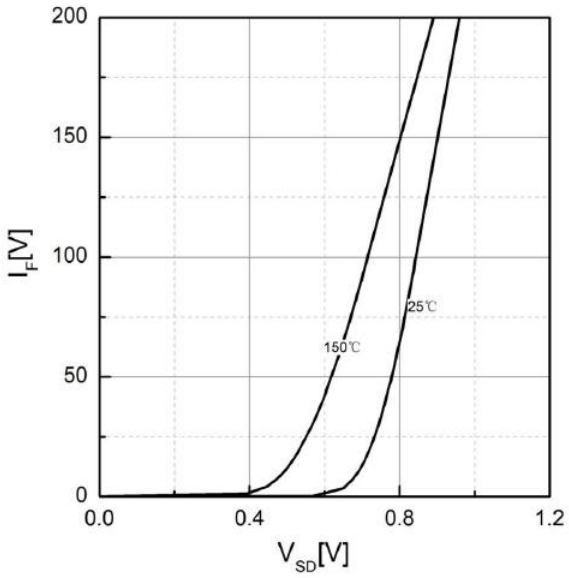


Figure 3. Forward characteristics of body diode

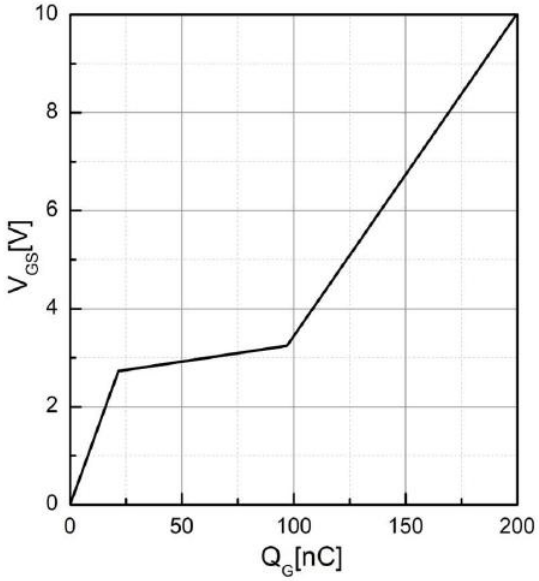


Figure 4. Gate Charge Characteristics

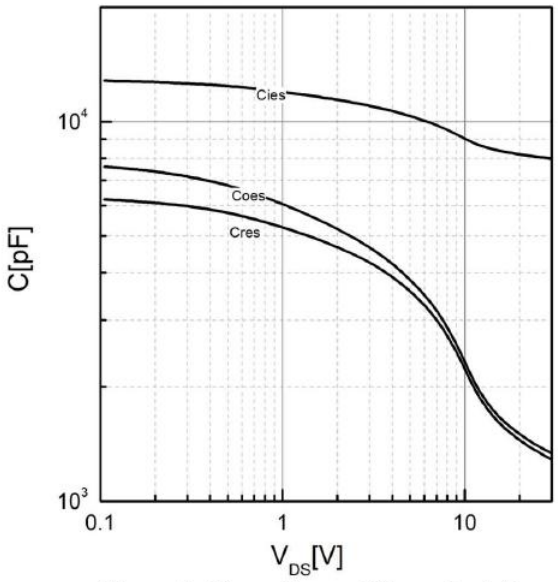


Figure 5. Capacitance Characteristics

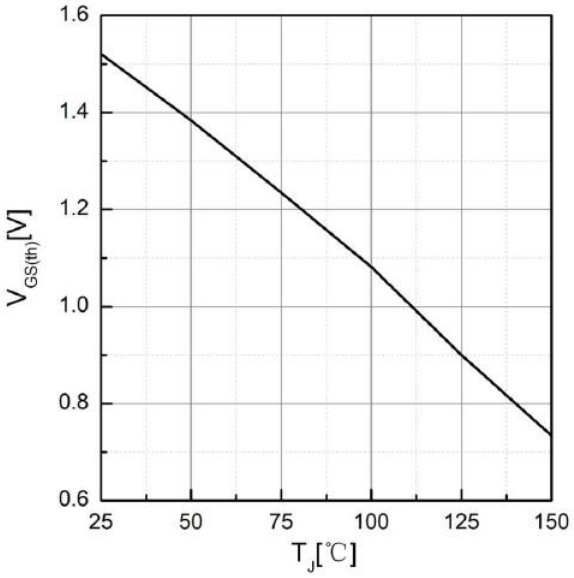


Figure 6. Threshold Voltage Vs. Temperature

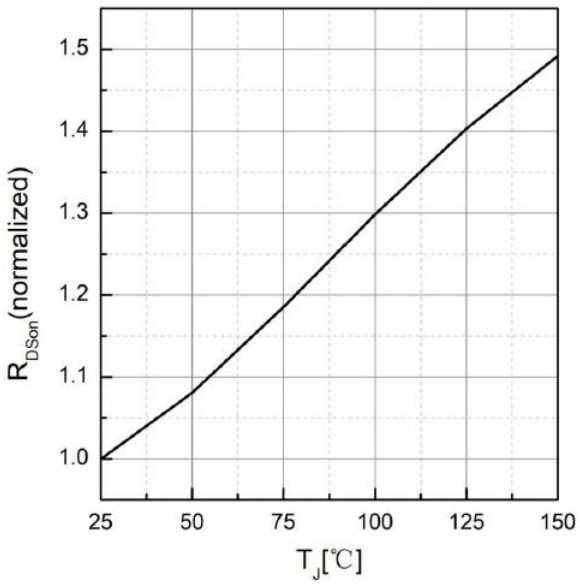


Figure 7. Drain-source on-state resistance

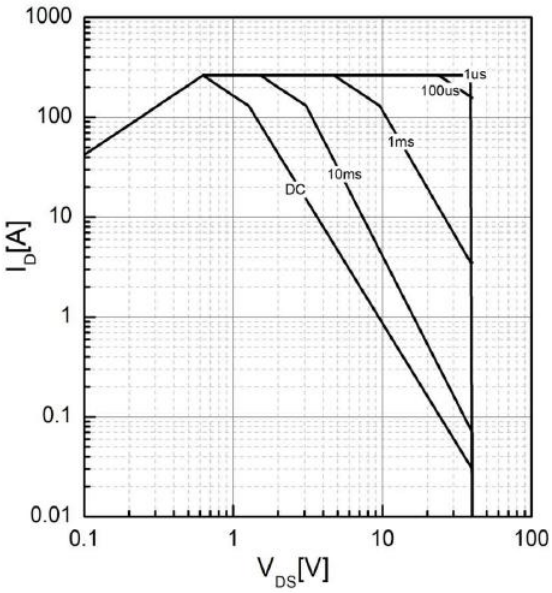


Figure 8. Maximum Safe Operating Area

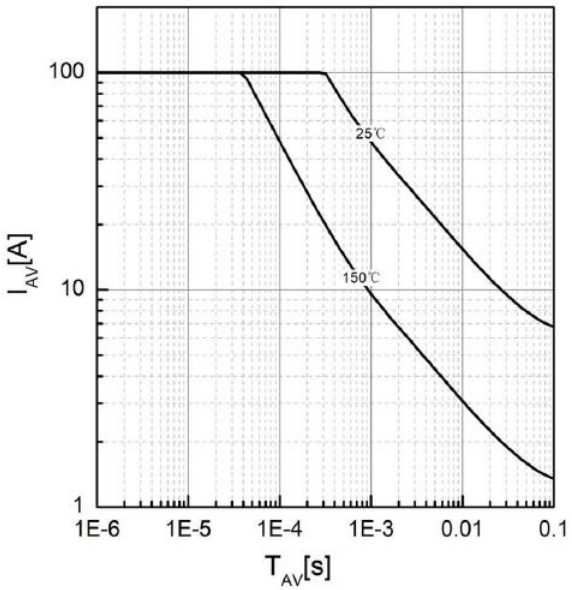


Figure 9. Avalanche characteristics

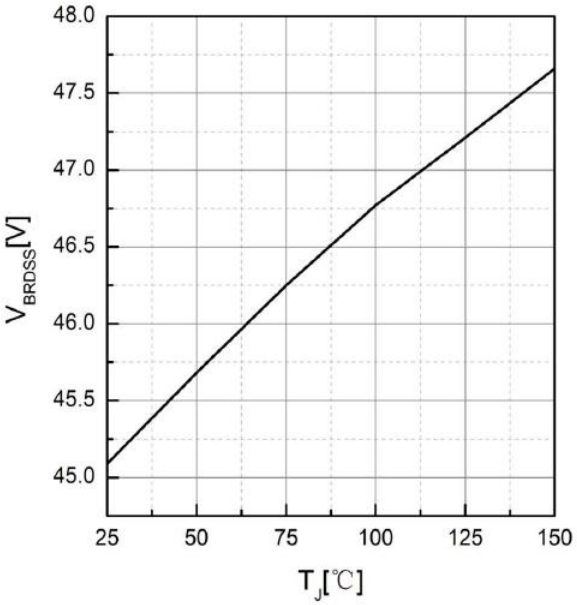


Figure 10. Drain-source breakdown voltage

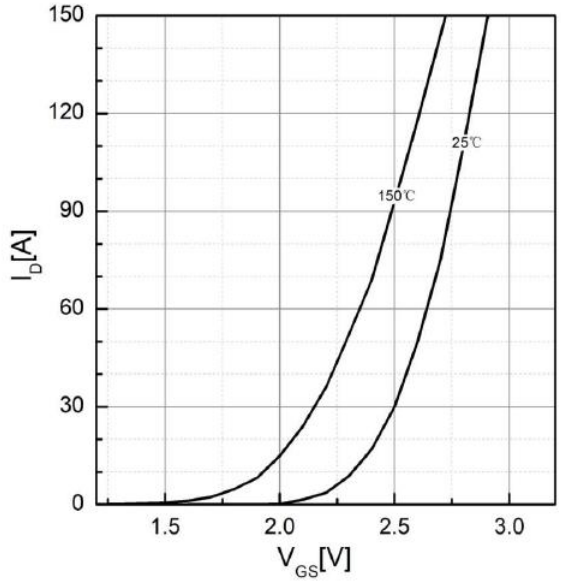


Figure 11. Transfer characteristics

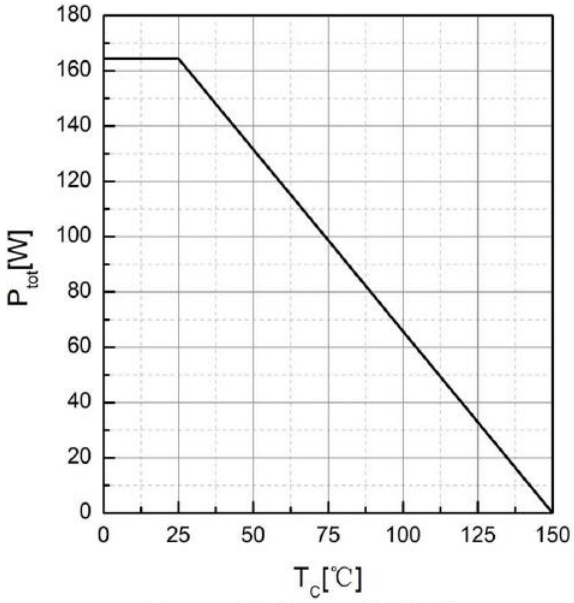


Figure 12. Power dissipation

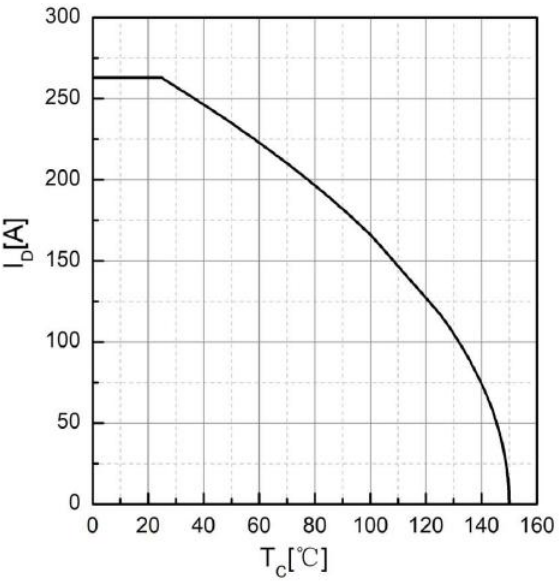


Figure 13. Drain current

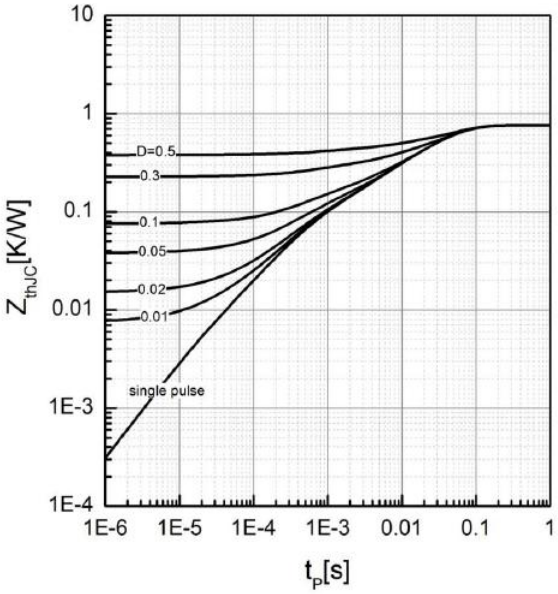


Figure 14. Effective Transient Thermal Impedance

9. Test Circuit & Waveform

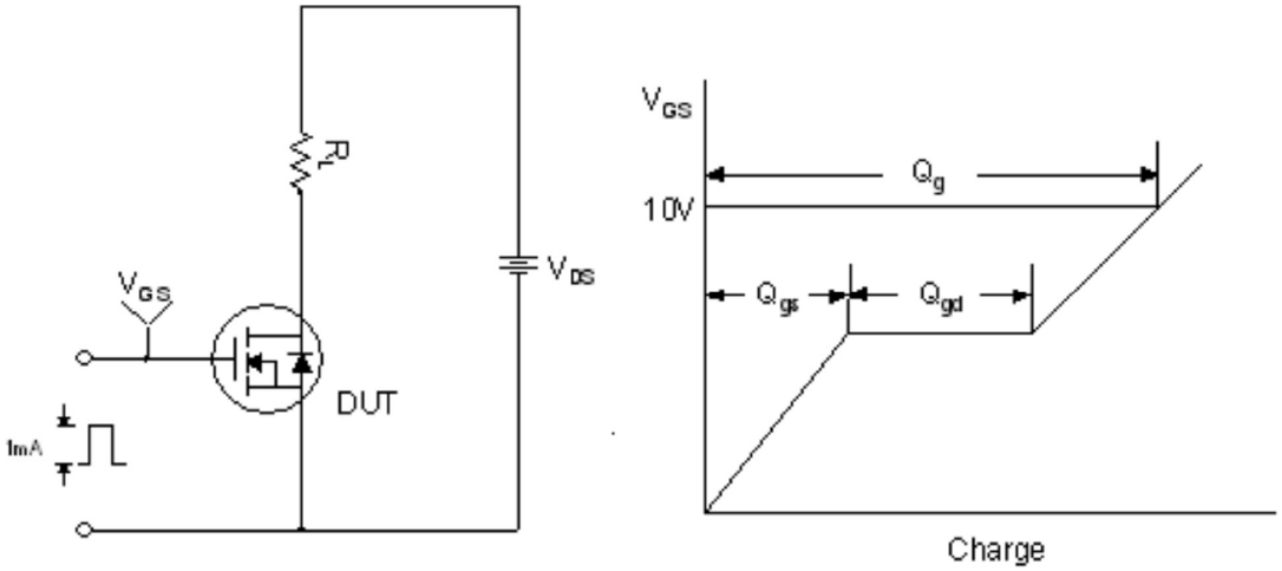


Figure 15. Gate Charge Test Circuit & Waveform

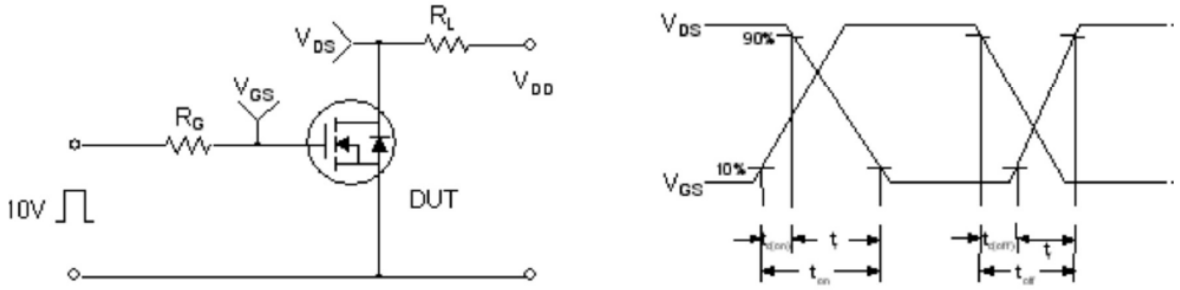


Figure 16. Resistive Switching Test Circuit & Waveforms

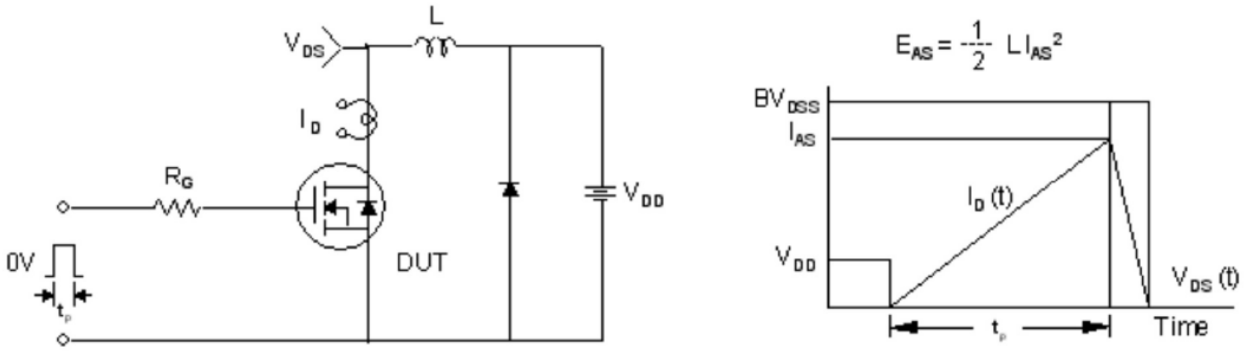
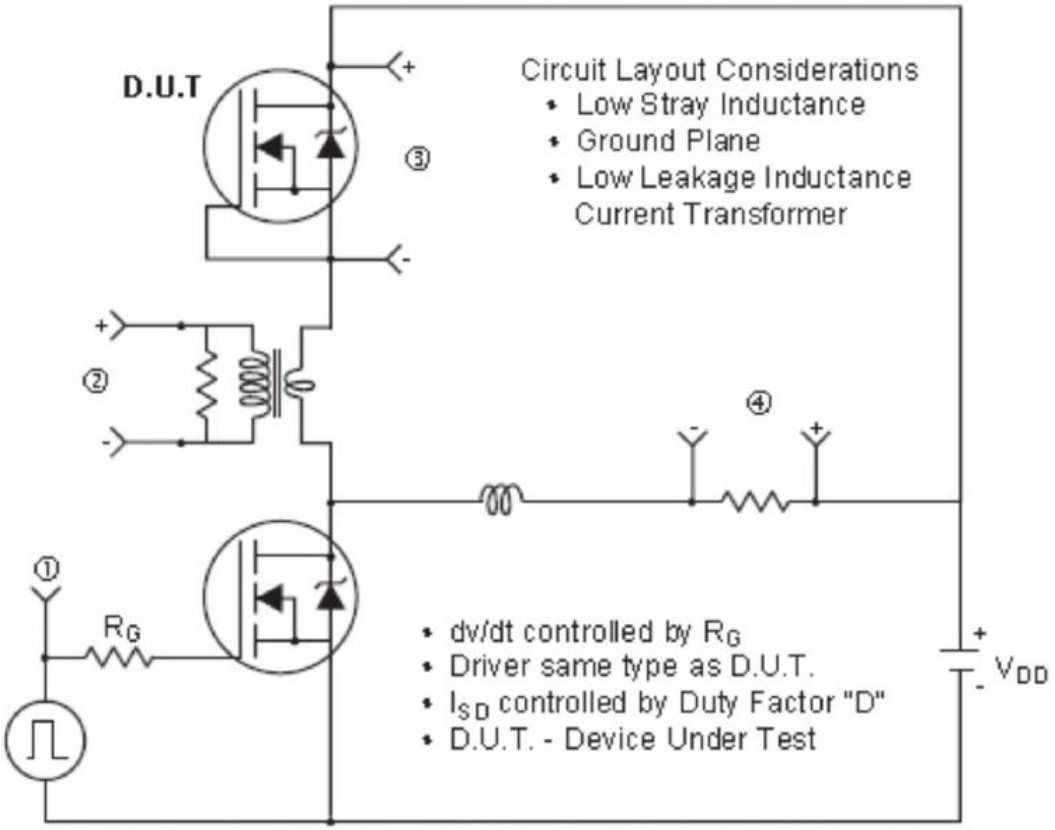
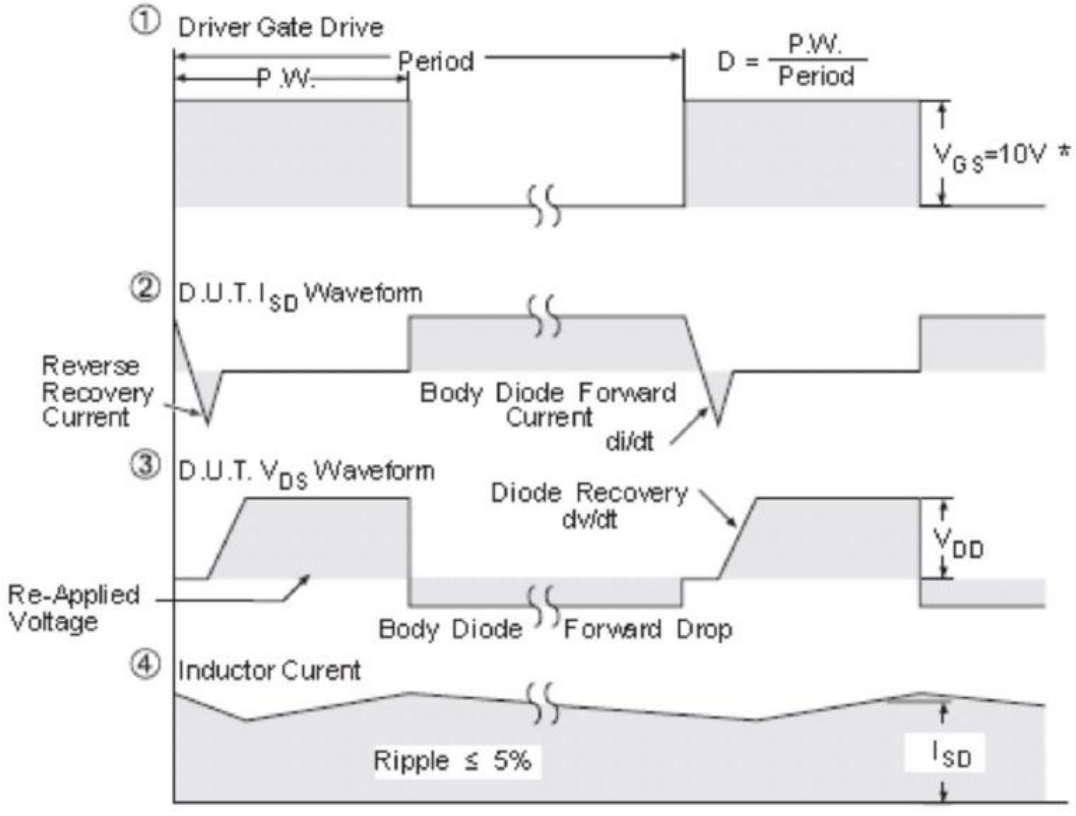


Figure 17. Unclamped Inductive Switching Test Circuit & Waveforms





* V_{GS} = 5V for Logic Level Devices