

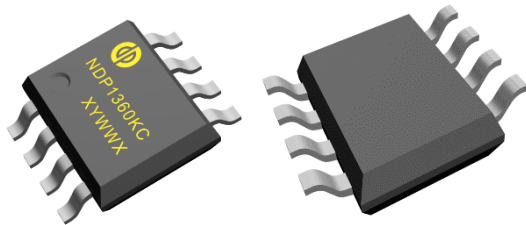
6A,30V High Efficiency Synchronous Step-Down DC/DC Converter

Description

NDP1360KC is a high efficiency, monolithic synchronous step-down DC/DC converter utilizing a jitter frequency mode control architecture. Capable of delivering up to 6A continuous load with excellent line regulation. The device operates from an input voltage range of 7.5V to 30V and provides an adjustable output voltage from 3.3V to 25V.

The NDP1360KC features short circuit and thermal protection circuits to increase system reliability. The internal soft-start avoids input inrush current during startup.

The NDP1360KC require a minimum number of external components and a wide array of protection features to enhance reliability.



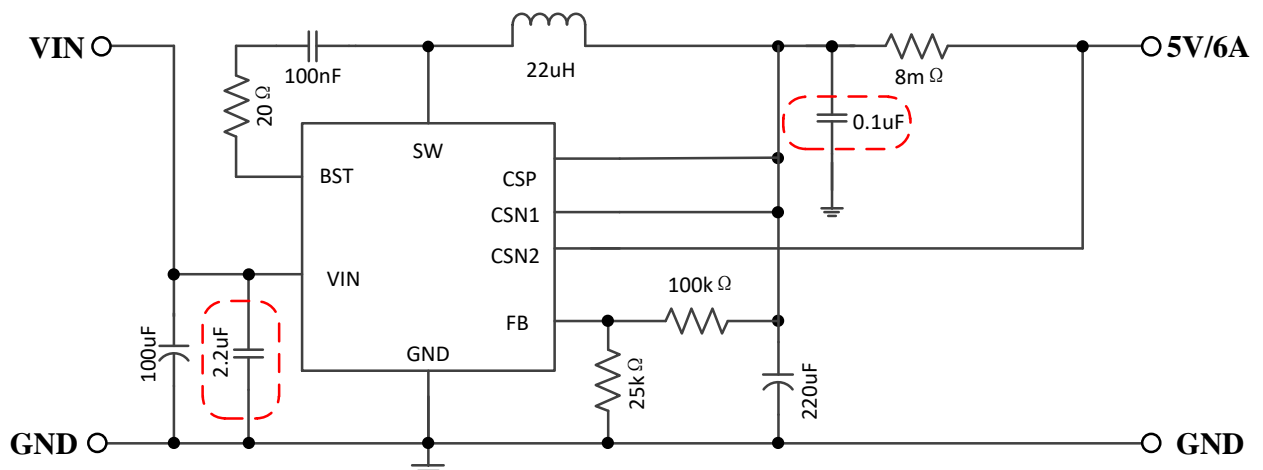
Features

- VIN Range: 7.5V to 30V
- 6A Continuous Output Current
- Up to 95% Efficiency @12V Input
- Dual-Channel CC/CV Mode Control
- Brick Wall Current Limit
- Built in Adjustable Line-Compensation
- Adjustable Output Voltages
- Output Voltage Accuracy: $\pm 2\%$
- Current Limit Accuracy: $\pm 4\text{mV}$
- Integrated $12\text{m}\Omega$ High Side Switch
- Integrated $12\text{m}\Omega$ Low Side Switch
- Fixed Frequency: 130kHz
- Burst Mode Operation at Light Load
- Internal Loop Compensation
- Internal Soft Start
- Available in SOP8 Package

Applications

- Car Charger
- Rechargeable Portable Devices
- Networking Systems

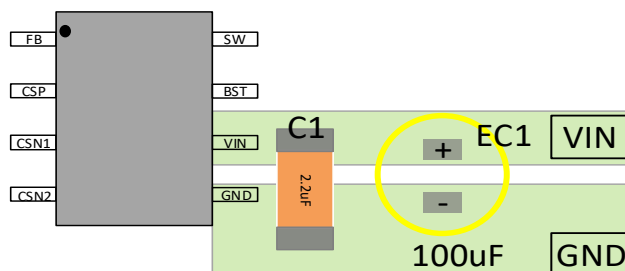
Typical Application



Note1: The ceramic capacitor for Vin should have a capacitance of 2.2μF or larger.

Note2: The ceramic capacitor for the output terminal CSP with a capacitance of 0.1μF should be placed close to the chip.

Layout Consideration

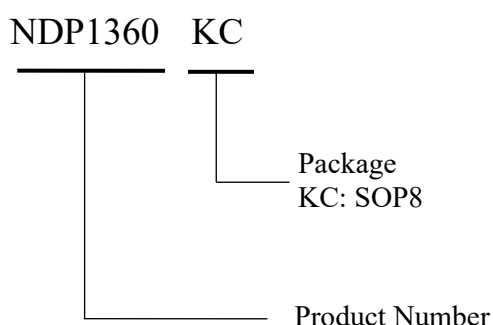


Note: C1 is as close as possible to the IC.

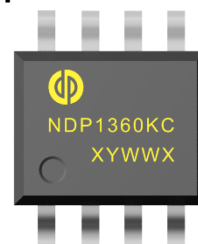
Order Information

Orderable Device	Package Type	Packing Qty/reel	MSL- Peak Temp -Floor Life	Eco Std	Marking Information
NDP1360KC	SOP8	4000	MSL3-260°C-168hrs	RoHS & Green	Refer to below

Product Naming



Top Side Marking



Y: Year (3=2023,4=2024...)
WW: Weekly (01-53)
X: Internal ID Code

Notes:

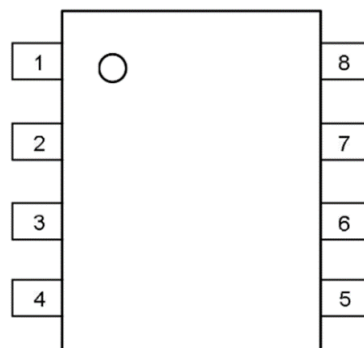
- (1) **RoHS:** Quoted from **RoHS Directive (EU) 2015/863**, Deep-Pool defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. Deep-Pool may reference these types of products as "**Pb-Free**".
- (2) **RoHS Exempt:** Deep-Pool defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- (3) **Green:** Deep-Pool defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JEDEC (**JS709C**) low halogen requirements of $\leq 1000\text{ppm}$ threshold.
- (4) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC (**J-STD-020F**) industry standard classifications, as well as the peak solder temperature of SMT and the floor life after unpacking, which customers should pay attention and strictly comply with the standard to use.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

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Pin Function and Definition

Pin	Name	Description
1	FB	Feedback of Output Voltage
2	CSP	Positive Pole of Current Sense
3	CSN1	Negative Pole1 of Current Sense1
4	CSN2	Negative Pole1 of Current Sense2
5	GND	Ground
6	VIN	Power Input
7	BST	Boot Strap
8	SW	Switching, Connected With a Inductor



Absolute Maximum Ratings (at TA = 25°C)

Characteristics	Symbol	Rating	Unit
VIN to GND		-0.3 to 33	V
SW to GND		-0.3 to VIN+0.3	V
BST to GND		-0.3 to VIN+7	V
FB to GND		-0.3 to 6.5	V
CSP, CSN1, CSN2 to GND		-0.3 to 25	V
Operating Junction Temperature	T _A	-40 to 150	°C
Storage Junction Temperature	T _{stg}	-65 to 150	°C
Thermal Resistance from Junction to case	θ _{JC}	30	°C/W
Thermal Resistance from Junction to ambient	θ _{JA}	60	°C/W

Notes:

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Recommended Operating Range

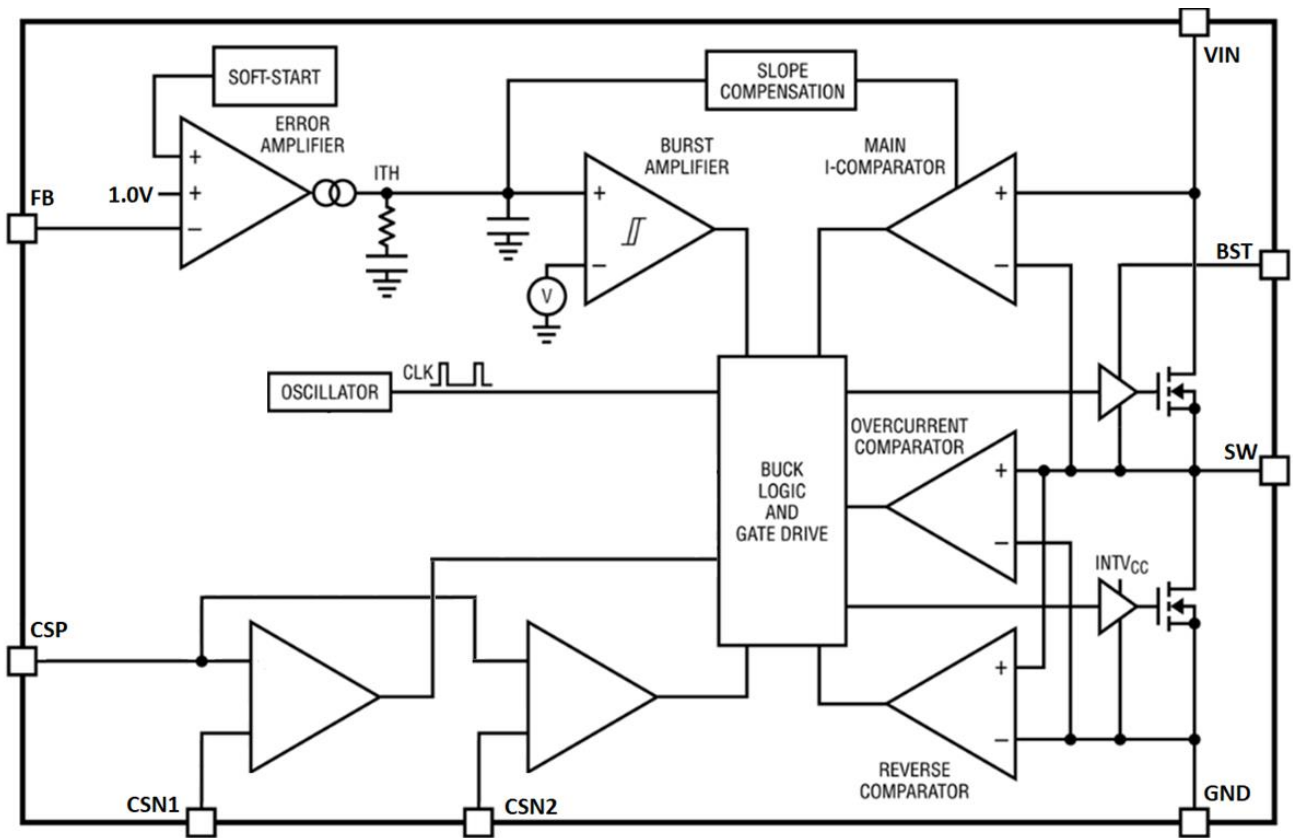
Electrical Parameter	Min	Typ	Max	Units
Input Voltage (VIN)	8		24	V
Output Voltage (VOUT)	3.3		20	V
Output Current (IOUT)			6	A
Maximum Duty Cycle (D _{MAX})			95	%

Electrical Characteristics

TJ = 25°C, VIN = 12V, unless otherwise noted.

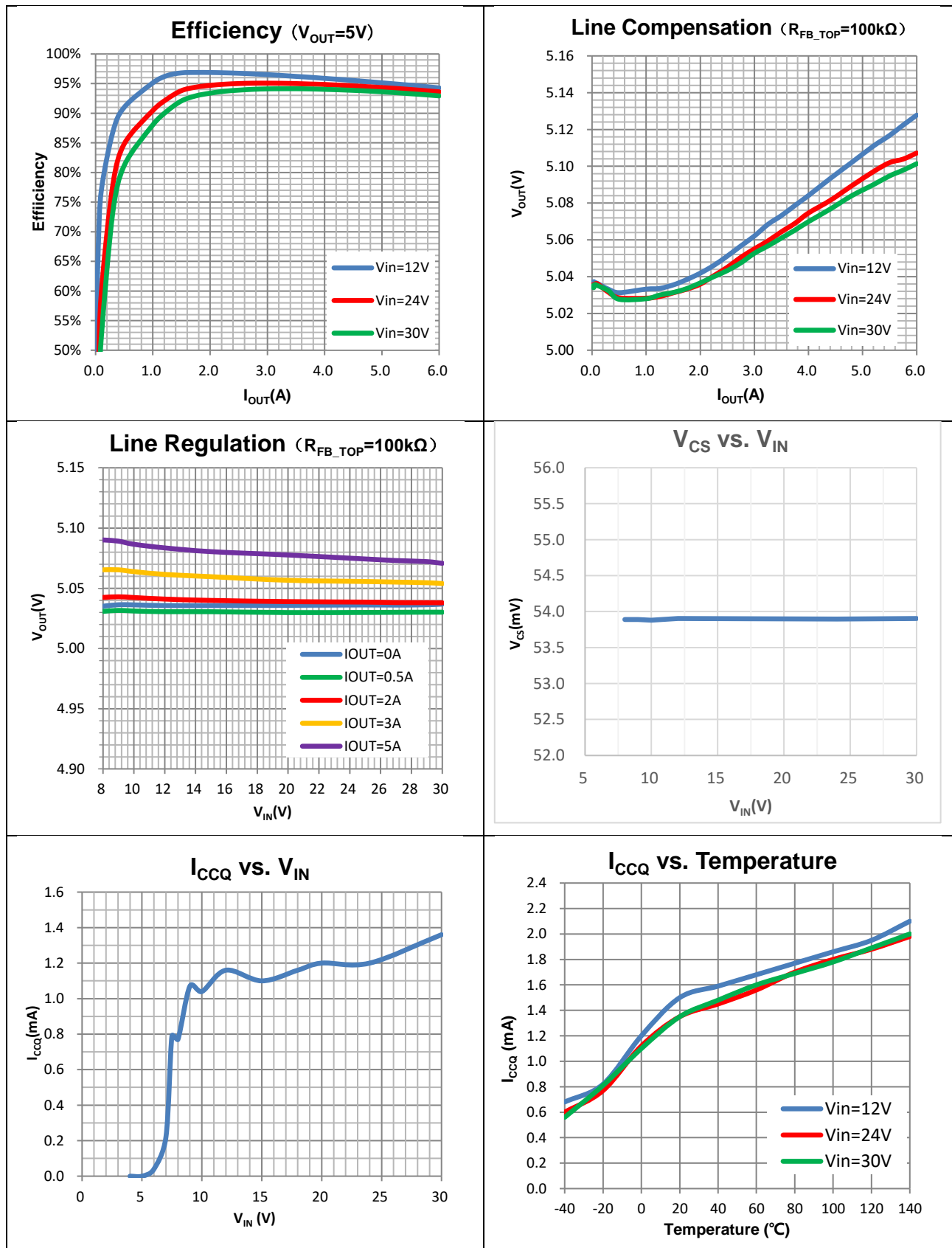
Characteristics	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage	V _{IN}		7	-	30	V
UVLO Voltage	V _{UVLO}			6.8	7	V
UVLO Hysteresis				0.8		V
Quiescent Current	I _{CCQ}	V _{FB} = 1.2V, No Switch		1300		μA
Standby Current	I _{SB}	No Load		1.7	2.2	mA
FB Reference Voltage	V _{REF}		0.985	1	1.015	V
FB Bias Current	I _{FB}				0.2	μA
Current Sense AMP	V _{CS1}	CSP-CSN1	51	55	59	mV
	V _{CS2}	CSP-CSN2	51	55	59	mV
Switching Frequency	F _{SW}		110	130	150	kHz
Maximum Duty Cycle				98		%
Minimum On-Time				250		ns
Current Limit	I _{LIMIT}		7			A
V _{OUT} Short Protect	V _{SCP}			3.0		V
Hiccup Interval	T _{HICCUP}			400		ms
Soft Start Time	T _{SS}			2		ms
R _{DS(on)} of Power MOSFET	R _{DS(on)_H}	Temperature=25°C		12		mΩ
	R _{DS(on)_L}	Temperature=25°C		12		mΩ
Thermal Regulation Temperature	T _{TR}			145		°C
Thermal shutdown Temperature	T _{SD}			165		°C
Thermal Shutdown Hysteresis Temperature	T _{SH}			30		°C

Block Diagram

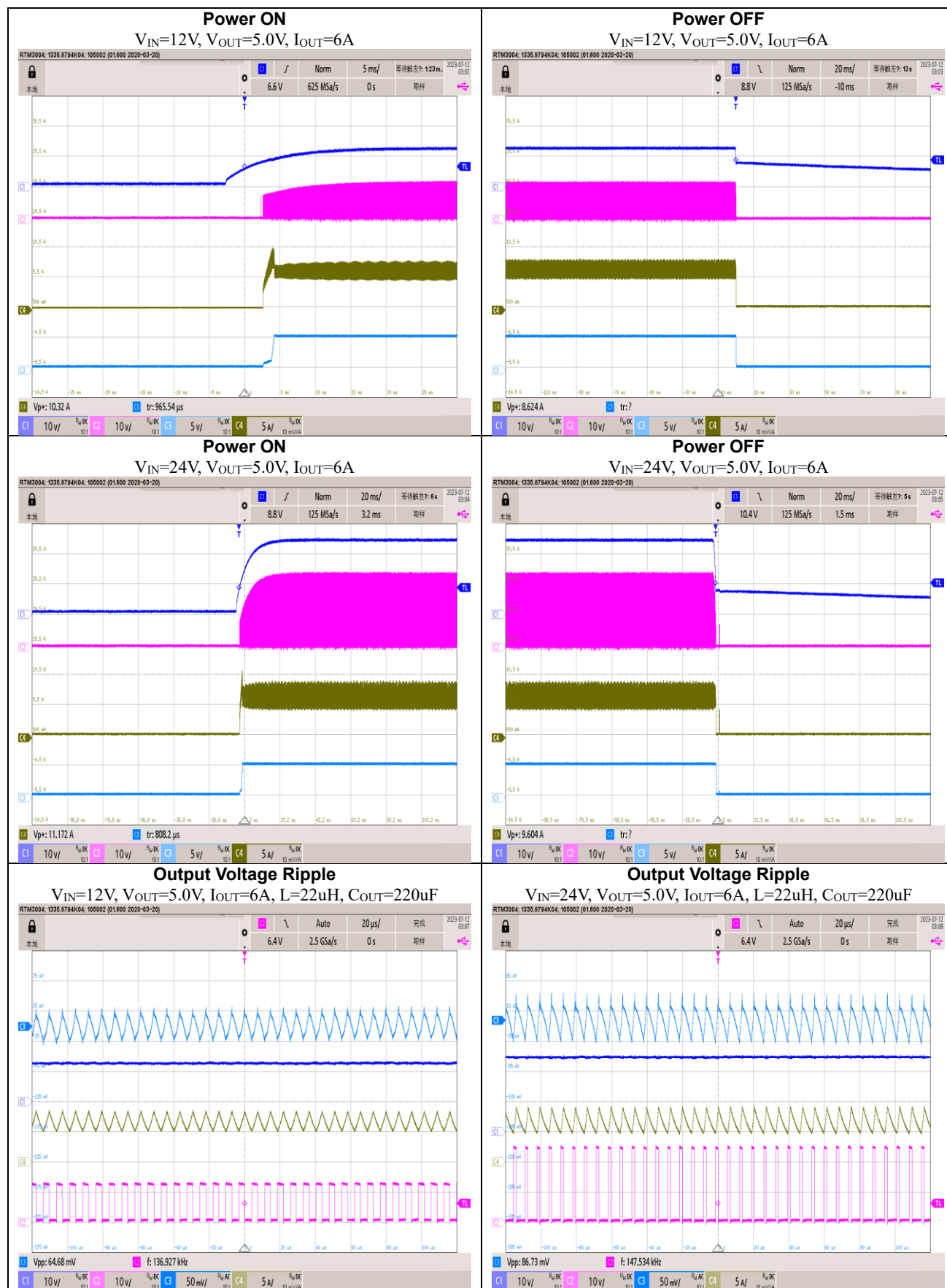


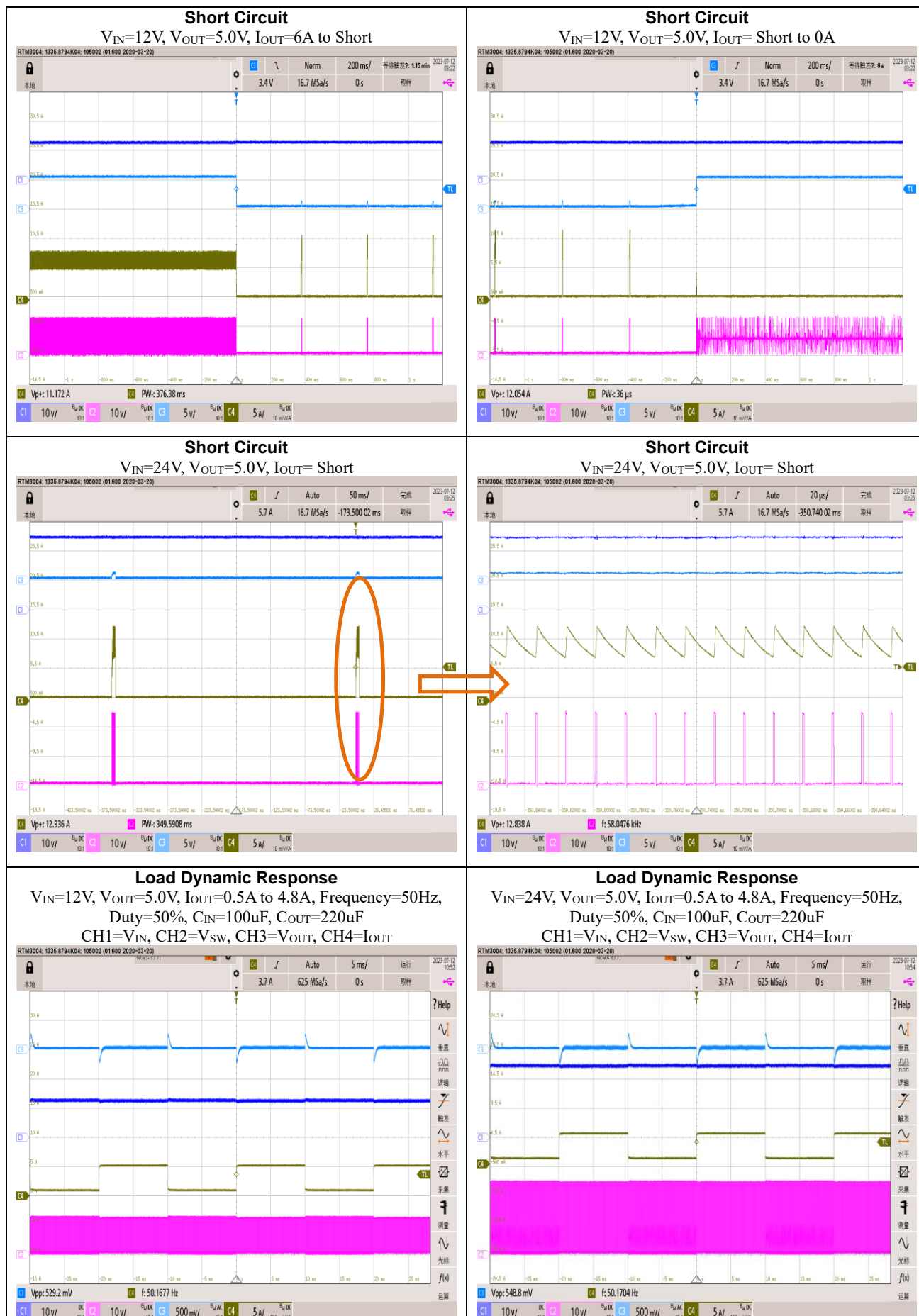
Typical Performance Characteristics

$T_J = 25^\circ\text{C}$, $V_{IN} = 12\text{V}$, unless otherwise noted.



CH1=V_{IN}, CH2=V_{SW}, CH3=V_{OUT}, CH4=I_{SW}, unless otherwise noted.





Operational Description

The NDP1360KC is a high efficiency, monolithic, synchronous step-down DC/DC converter utilizing a jitter frequency control architecture. Average current mode control enables fast and precise control of the output current. It operates through a wide VIN range and regulates with low quiescent current. An error amplifier compares the output voltage with an internal reference voltage of 1.0V and adjusts the peak inductor current accordingly. Overvoltage and undervoltage comparators will turn off the regulator.

Main Control Loop

During normal operation, the internal top power switch (N-channel MOSFET) is turned on at the beginning of each clock cycle, causing the inductor current to increase. The sensed inductor current is then delivered to the average current amplifier, whose output is compared with a saw-tooth ramp. When the voltage exceeds the Vduty voltage, the PWM comparator trips and turns off the top power MOSFET. After the top power MOSFET turns off, the synchronous power switch (N-channel MOSFET) turns on, causing the inductor current to decrease. The bottom switch stays on until the beginning of the next clock cycle, unless the reverse current limit is reached and the reverse current comparator trips. In closed-loop operation, the average current amplifier creates an average current loop that forces the average sensed current signal to be equal to the internal ITH voltage. Note that the DC gain and compensation of this average current loop is automatically adjusted to maintain an optimum current-loop response. The error amplifier adjusts the ITH voltage by comparing the divided-down output voltage (VFB) with a 1.0V reference voltage. If the load current changes, the error amplifier adjusts the average inductor current as needed to keep the output voltage in regulation.

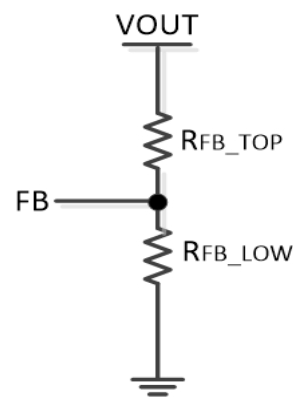
Low Current Operation

The discontinuous-conduction modes (DCMs) are available to control the operation of the NDP1360KC at low currents. Burst Mode operation automatically switch from continuous operation to the Burst Mode operation when the load current is low.

Constant Voltage Output

NDP1360KC presets the FB voltage (V_{REF}) to 1V. The Output can be set by extra resistance.

$$V_{OUT} = V_{REF} * \frac{R_{FB_TOP} + R_{FB_LOW}}{R_{FB_LOW}}$$



Cable Drop Compensation

Due to the resistive of charger's output Cable, The NDP1360KC built in a simple user programmable cable voltage drop compensation using the impedance at the FB pin. Choose the proper resistance values for charger's output cable as show in Table 1:

R_{FB_TOP} is the upper resistor the resistors divider net

R_{FB_LOW} is the lower resistor the resistors divider net

R_{FB_TOP} (kΩ)	R_{FB_LOW} (kΩ)	Typ Cable Drop Compensation (mV)
100	25	75
160	39	250
360	91	570
470	120	750
820	200	1400
1200	300	2000

Table 1

Applications Information

Input Capacitor (C_{IN}) Selection

The input capacitance C_{IN} is needed to filter the square wave current at the drain of the top power MOSFET. To prevent large voltage transients from occurring, a low ESR input capacitor sized for the maximum RMS current should be used. The maximum RMS current is given by:

$$I_{RMS} \cong I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where:

$$I_{RMS} \cong I_{OUT}/2.$$

This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

Output Capacitor (C_{OUT}) Selection

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output ripple, ΔV_{OUT} , is determined by:

$$\Delta V_{OUT} < \Delta I_L \left(\frac{1}{8 \cdot f \cdot C_{OUT}} + ESR \right)$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling

requirements. Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface mount packages. Special polymer capacitors are very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics and small footprints.

Inductor Selection

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \frac{V_{OUT}}{F * L} \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right)$$

Lower ripple current reduces power losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a trade-off between component size, efficiency and operating frequency. A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \frac{V_{OUT}}{F * \Delta I_{L(MAX)}} \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right)$$

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value, but is very dependent on the inductance selected. As the inductance or frequency increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper

losses will increase. Copper losses also increase as frequency increases. Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard”, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements. New designs for surface mount inductors are available from Coilcraft, Toko, Vishay, NEC/Tokin, TDK and Würth Elektronik.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement.

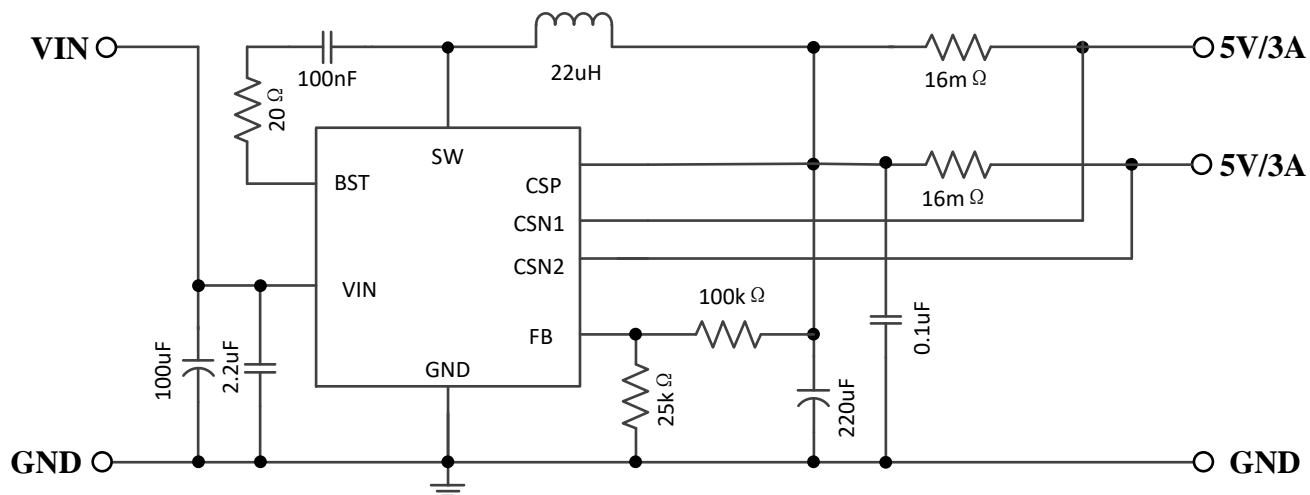
Percent efficiency can be expressed as: % Efficiency = $100\% - (\text{Loss1} + \text{Loss2} + \dots)$ where Loss1, Loss2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, three main sources usually account for most of the losses in NDP1360KC circuits: 1) I^2R losses, 2) switching and biasing losses, 3) other losses.

Thermal Conditions

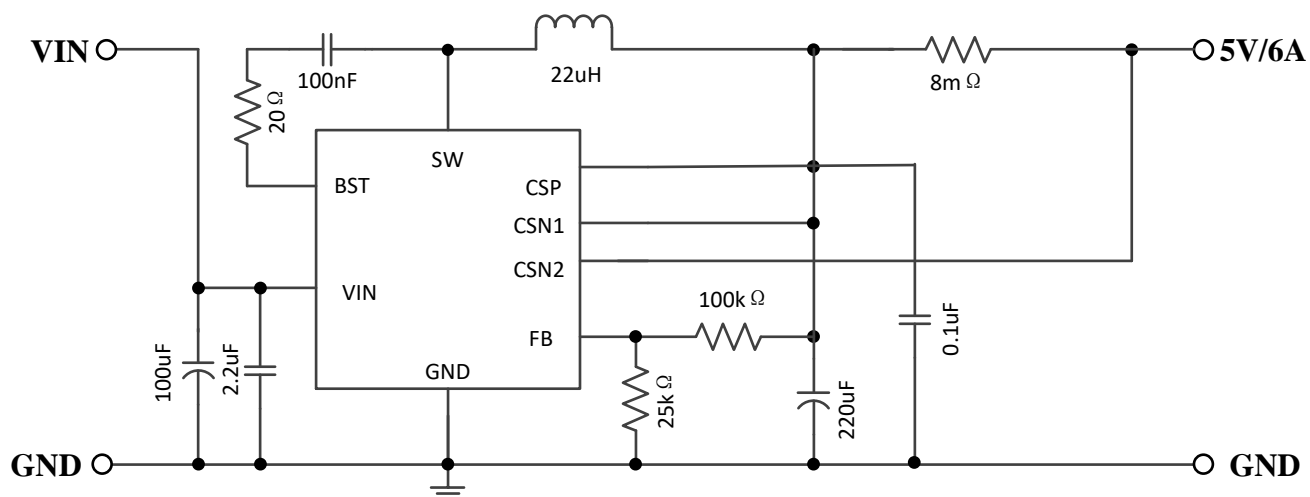
In a majority of applications, the NDP1360KC does not dissipate much heat due to its high efficiency and low thermal resistance. However, in applications where the NDP1360KC is running at high ambient temperature, high VIN, and maximum output current load, the heat dissipated may exceed the maximum junction temperature of the part.

If the junction temperature reaches approximately 160°C, both power switches will be turned off until the temperature drops about 20°C cooler to avoid the NDP1360KC from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. If the application calls for a higher ambient temperature and/or higher switching frequency, care should be taken to reduce the temperature rise of the part by using a heat sink or forced air flow.

Typical Applications

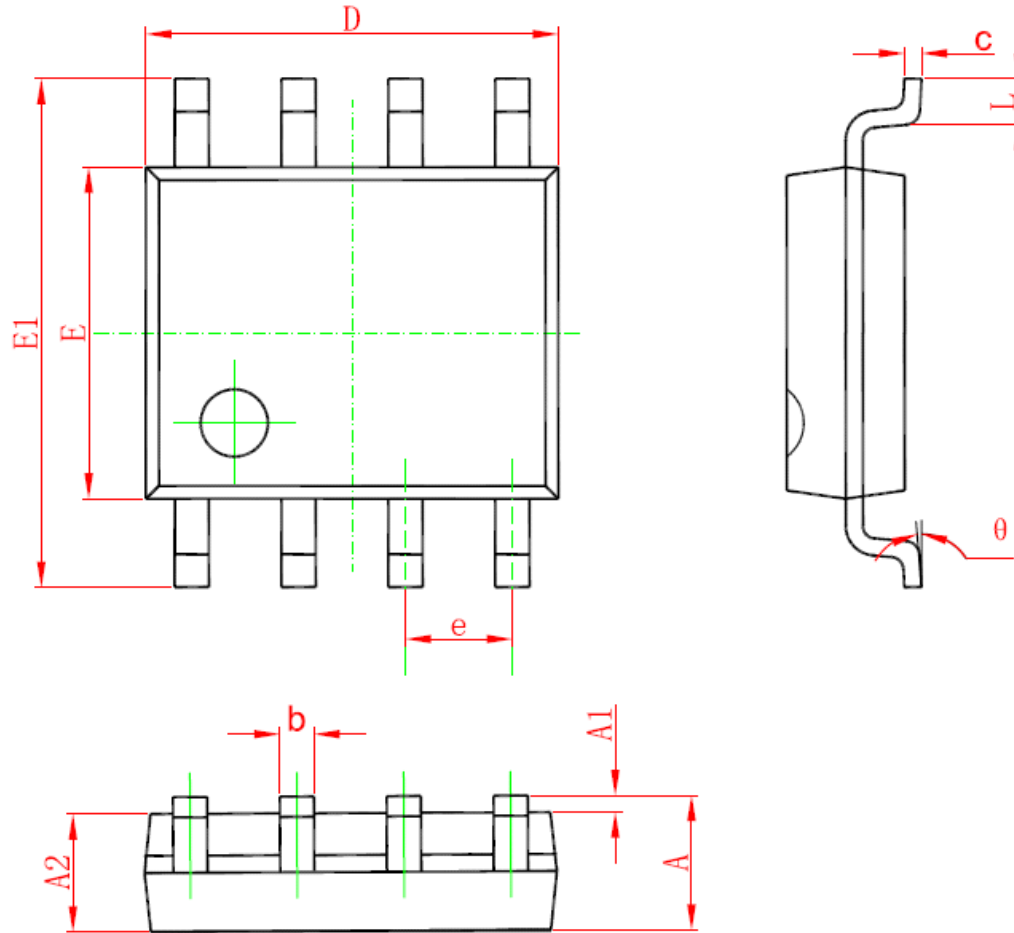


Dual Channel Application



Single Channel Application

Package Outline Drawing



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.150	0.185	0.203
E	3.800	4.000	0.15	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.05 (BSC)	

Notes

1. Use millimeters as the primary measurement
2. Dimensioning and tolerances conform to ASME Y14.5M. – 1994
3. These dimensions do not include mold flash or protrusions.
4. Mold flash or protrusions shall not exceed 0.15mm

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