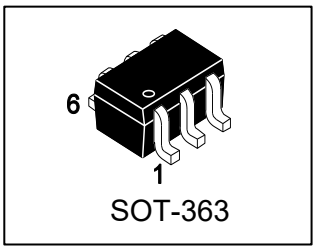
N-Channel 50V,0.2A ,ESD Protection, N-MOSFET

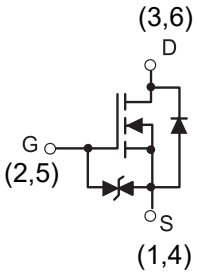
FEATURES

- $R_{DS(ON)} \leqq 3.5\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leqq 4\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

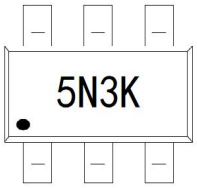


APPLICATIONS

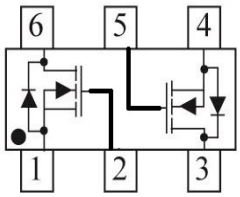
- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter



MARKING



Pin configuration (Top view)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		**Symbol**	**5 secs**	**Steady State**	**Unit**
Drain-Source Voltage		V_{DS}	50		V
Gate-Source Voltage		V_{GS}	±20		
Continuous Drain Current (T_J = 150°C)[b]	T_A = 25°C	I_D	0.25	0.2	mA
	T_A = 85°C		0.2	0.1	
Pulsed Drain Current[a]		I_{DM}	800		
Continuous Source Current (diode conduction)[b]		I_S	200	150	
Maximum Power Dissipation[b] for SOT363	T_A = 25°C	P_D	250	200	mW
	T_A = 85°C		150	120	
Thermal Resistance, Junction–to–Ambient		RΘJA	633		°C/W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150		°C

Notes
d. Pulse width limited by maximum junction temperature.
e. Surface Mounted on FR4 Board.

N-Channel 50V (D-S) MOSFET, ESD Protection

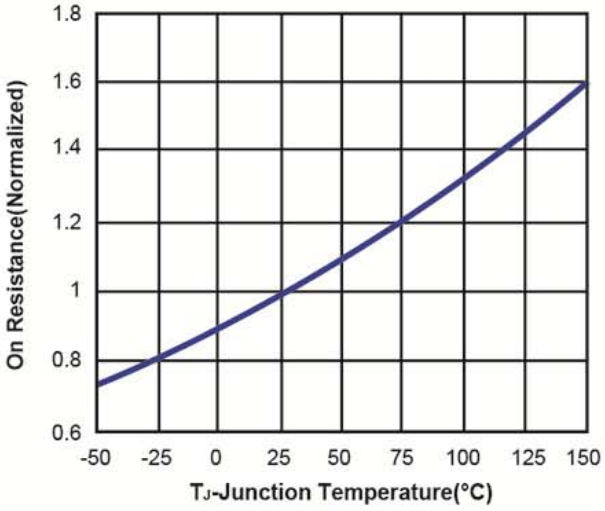
Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	yp	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	50			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=1mA	0.6		1.5	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±10	μA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=50V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance[a]	V_{GS}=10V, I_D=200mA		2.5	3.5	Ω
		V_{GS}=4.5V, I_D=200mA		3.1	4	
V_{SD}	Diode Forward Voltage	I_S=0.44A, V_{GS}=0V		0.8	1.4	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=25V, V_{GS}=10V, I_D=0.22A		4.7		nC
Qgs	Gate urce Charge			1.7		
Qgd	ate-Drain Charge			0.8		
Ciss	Input Capacitance	V_{DS}=25V, V_{GS}=0V, f=1MHZ		33		pf
Coss	Output Capacitance			25		
Crss	Reverse Transfer Capacitance			13		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=5V, R_L =500Ω, V_{GEN}=5V,R_G=10Ω		10.1		ns
t_r	Turn-On Rise Time			7.3		
$t_{d(off)}$	Turn-Off Delay Time			31.3		
t_f	Turn-Off Fall Time			28.2		

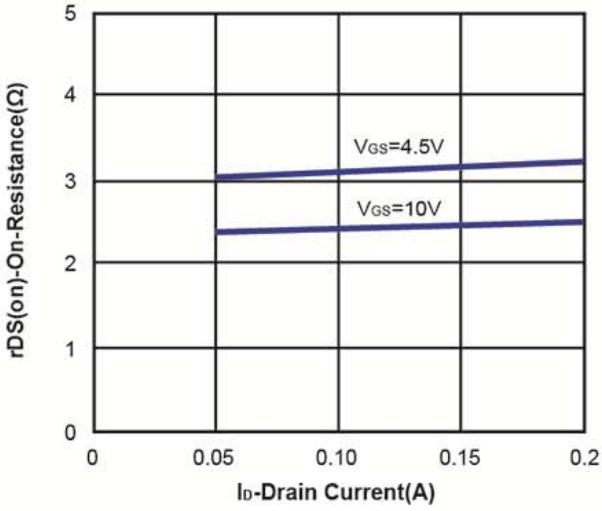
Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Titan mos reserves the right to improve product design, functions and reliability without notice.

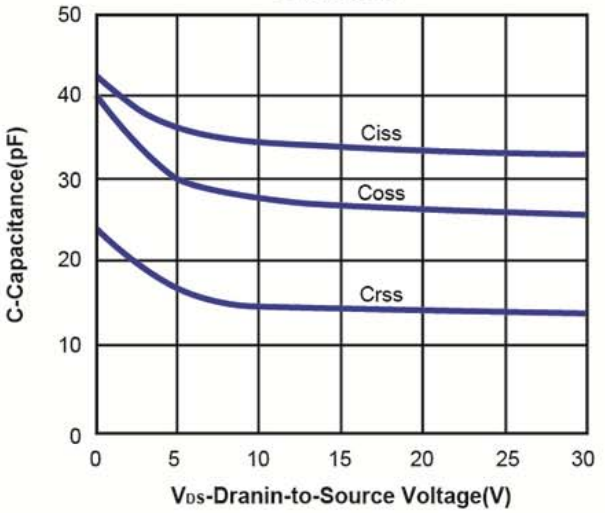
On Resistance vs. Junction Temperature



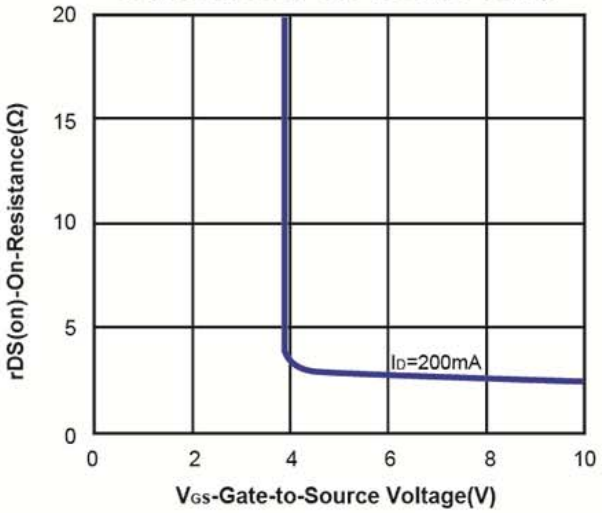
On Resistance vs. Drain Current



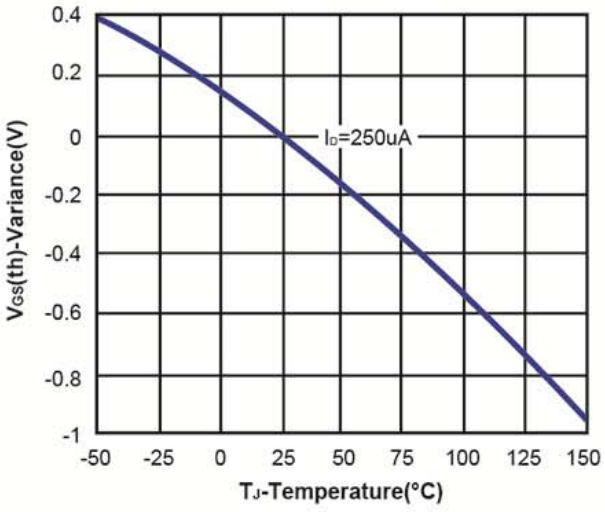
Capacitance



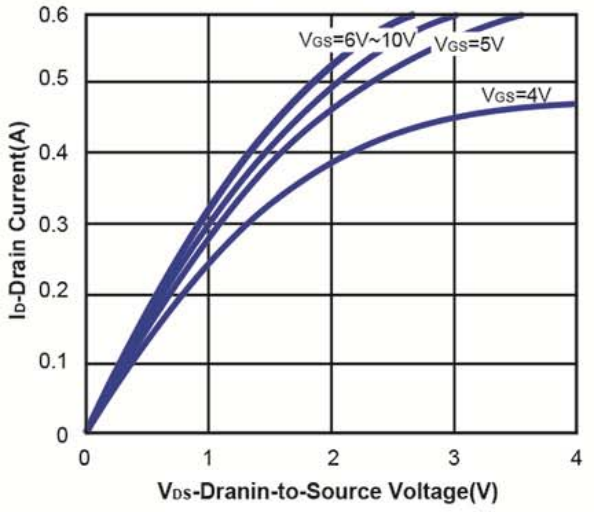
On Resistance vs. Gate-to-Source Voltage



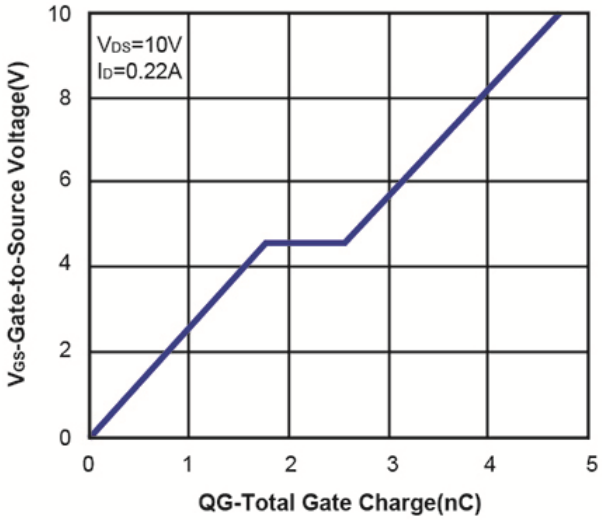
Threshold Voltage



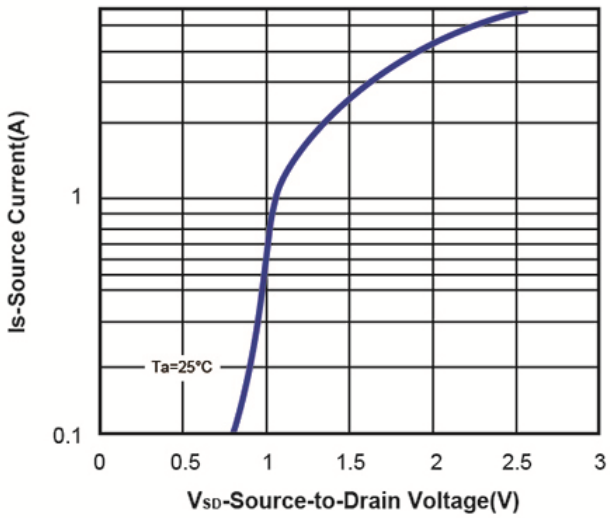
On-Region Characteristics



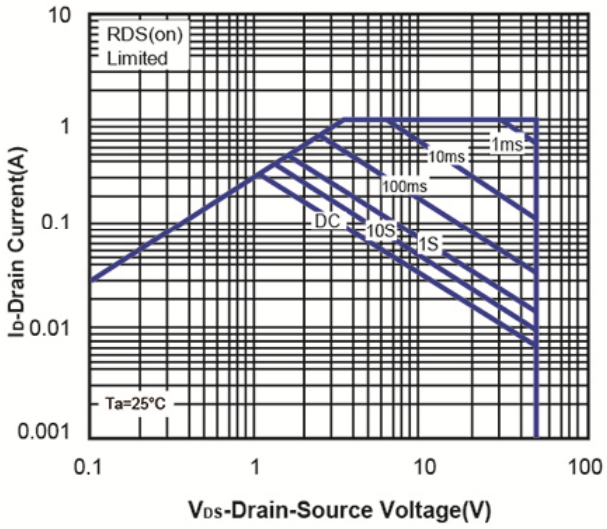
Gate Charge



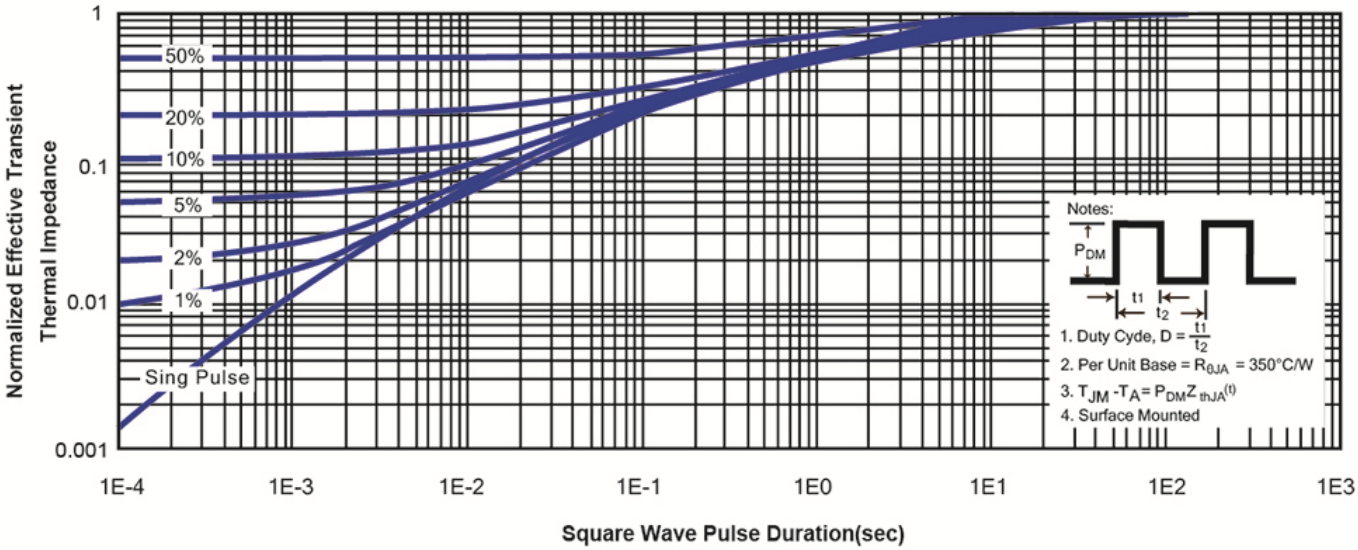
Body-diode characteristics



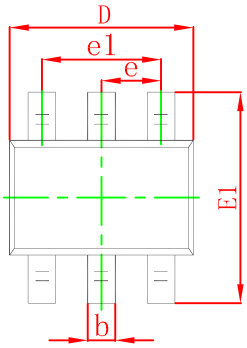
Maximum Forward Biased Safe Operating Area

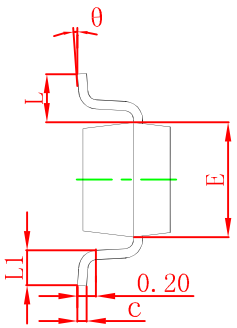


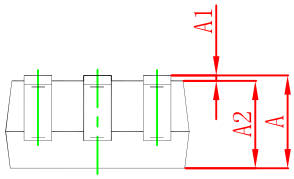
Normalized Thermal Transient Impedance, Junction-to-Ambient



SOT-363 Package Outline Dimensions

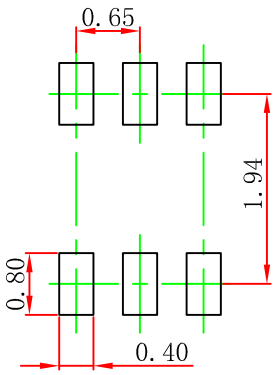






Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.100	0.150	0.004	0.006
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.400	0.085	0.094
e	0.650 TYP		0.026 TYP	
e1	1.200	1.400	0.047	0.055
L	0.525 REF		0.021 REF	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

SOT-363 Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.