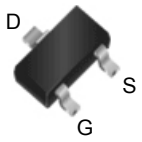
N-Channel 50V,ESD Protection, N-MOSFET

FEATURES

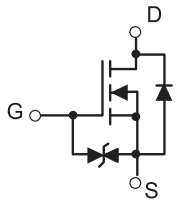
- $R_{DS(ON)} \leqq 3.5\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leqq 4\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability



SOT-523

APPLICATIONS

- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		**Symbol**	**5 secs**	**Steady State**	**Unit**
Drain-Source Voltage		V_{DS}	50		V
Gate-Source Voltage		V_{GS}	±20		
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	250	200	mA
	T_A = 85°C		200	100	
Pulsed Drain Current[a]		I_{DM}	1000		
Continuous Source Current (diode conduction)		I_S	275	250	
Maximum Power Dissipation for SOT523	T_A = 25°C	P_D	275	250	mW
	T_A = 85°C		160	140	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150		°C

Notes
Pulse width limited by maximum junction temperature.
Surface Mounted on FR4 Board.

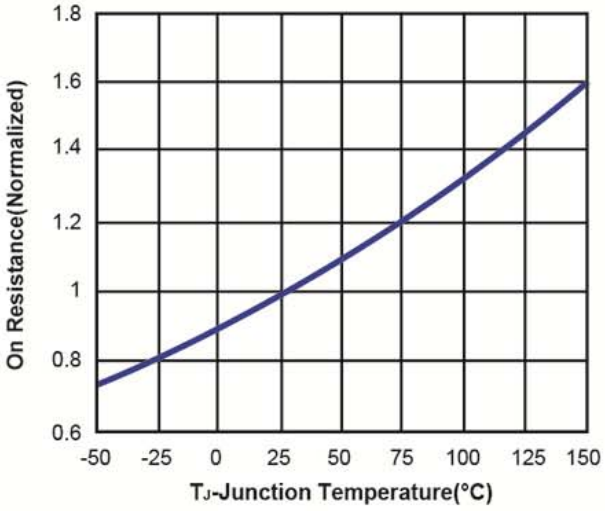
N-Channel 50V (D-S) MOSFET, ESD Protection

Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

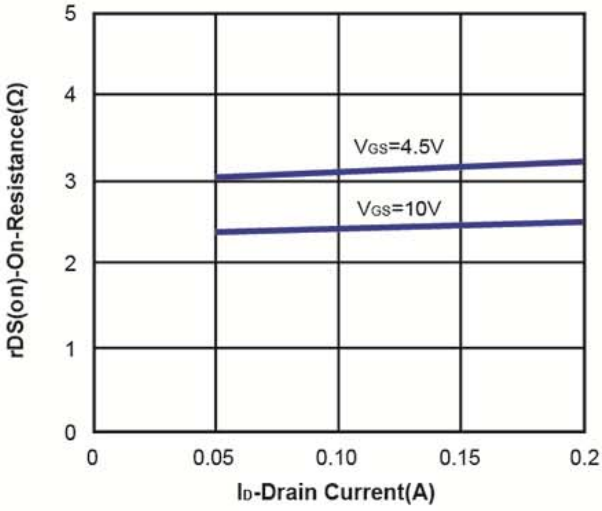
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	50			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=1mA	0.6		1.5	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±10	μA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=50V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance[a]	V_{GS}=10V, I_D=200mA		2.5	3.5	Ω
		V_{GS}=4.5V, I_D=200mA		3.1	4	
V_{SD}	Diode Forward Voltage	I_S=0.44A, V_{GS}=0V		0.8	1.4	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=25V, V_{GS}=10V, I_D=0.22A		4.7		nC
Qgs	Gate urce Charge			1.7		
Qgd	ate-Drain Charge			0.8		
Ciss	Input Capacitance	V_{DS}=25V, V_{GS}=0V, f=1MHZ		33		pf
Coss	Output Capacitance			25		
Crss	Reverse Transfer Capacitance			13		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=5V, R_L=500Ω, V_{GEN}=5V,R_G=10Ω		10.1		ns
t_r	Turn-On Rise Time			7.3		
$t_{d(off)}$	Turn-Off Delay Time			31.3		
t_f	Turn-Off Fall Time			28.2		

Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

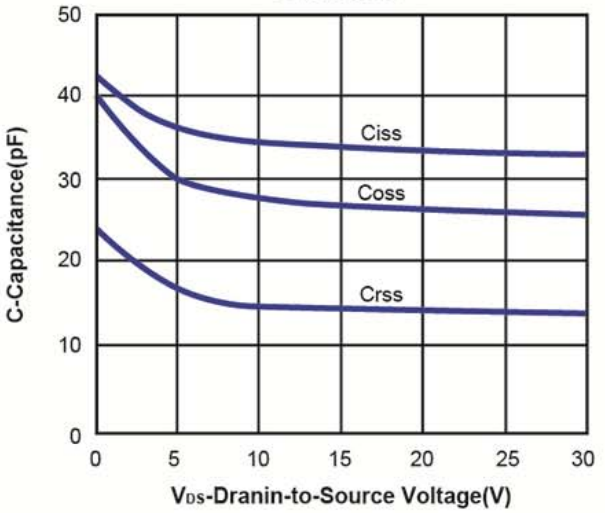
On Resistance vs. Junction Temperature



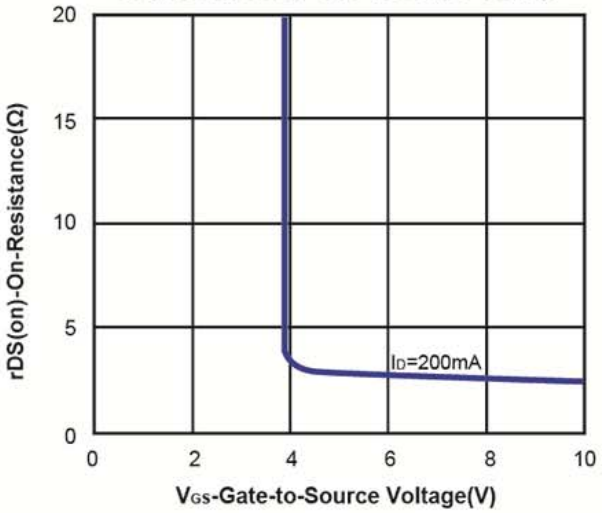
On Resistance vs. Drain Current



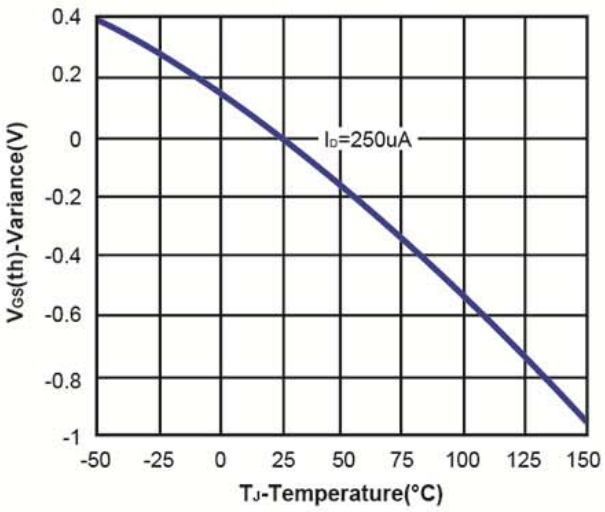
Capacitance



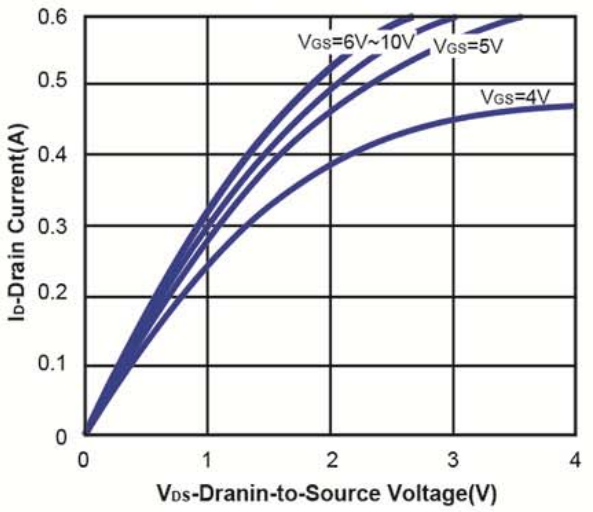
On Resistance vs. Gate-to-Source Voltage



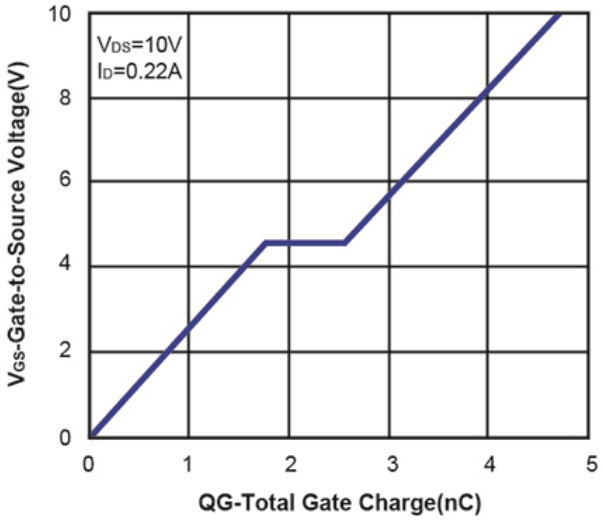
Threshold Voltage



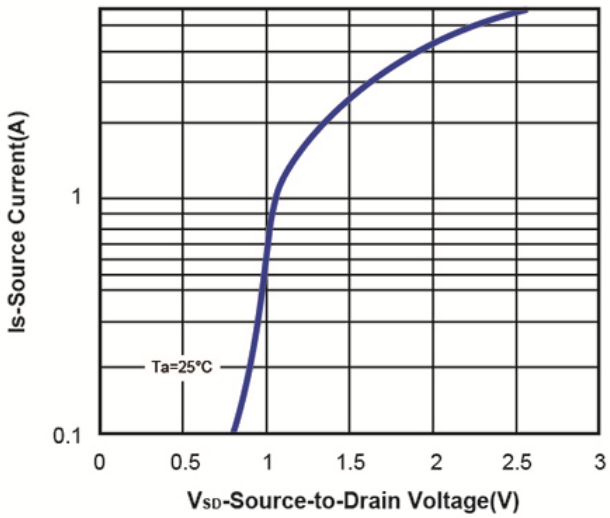
On-Region Characteristics



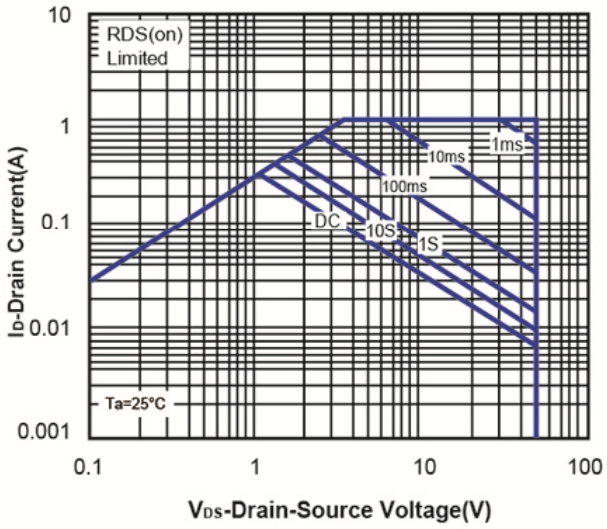
Gate Charge



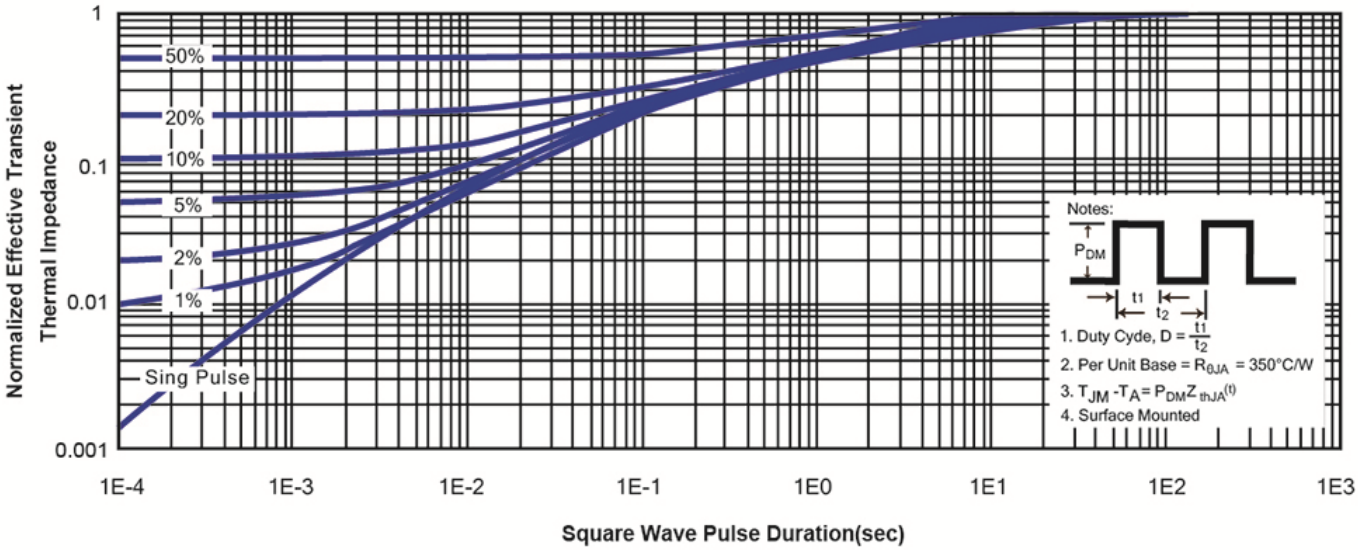
Body-diode characteristics



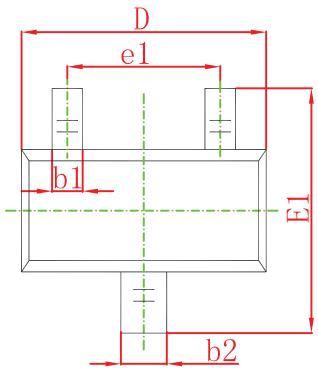
Maximum Forward Biased Safe Operating Area

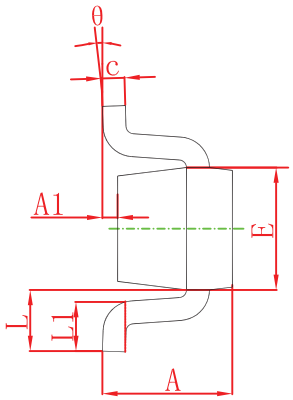


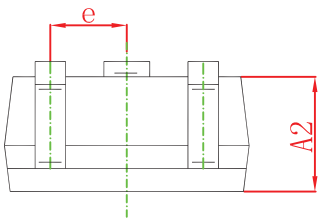
Normalized Thermal Transient Impedance, Junction-to-Ambient



SOT-523 Package Outline Dimensions

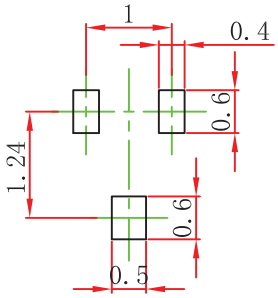






Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.900	0.028	0.035
A1	0.000	0.100	0.000	0.004
A2	0.700	0.800	0.028	0.031
b1	0.150	0.250	0.006	0.010
b2	0.250	0.350	0.010	0.014
c	0.100	0.200	0.004	0.008
D	1.500	1.700	0.059	0.067
E	0.700	0.900	0.028	0.035
E1	1.450	1.750	0.057	0.069
e	0.500 TYP.		0.020 TYP.	
e1	0.900	1.100	0.035	0.043
L	0.400 REF.		0.016 REF.	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

SOT-523 Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.