

100V N-Channel Power MOSFET

Description

MDT19N10L, the uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications

KEY CHARACTERISTICS

- ① $V_{DS}=100V, I_D=19A$
 $R_{DS(ON)} < 90m\Omega @ V_{GS}=10V$
 $R_{DS(ON)} < 115m\Omega @ V_{GS}=4.5V$
- ② High density cell design for lower R_{dson}
- ③ Fully characterized avalanche voltage and current
- ④ Good stability and uniformity with high EAS
- ⑤ Excellent package for good heat dissipation

APPLICATIONS

- ① Power switching application
- ② Hard switched and High frequency circuits
- ③ Uninterruptible power supply

ORDERING INFORMATION

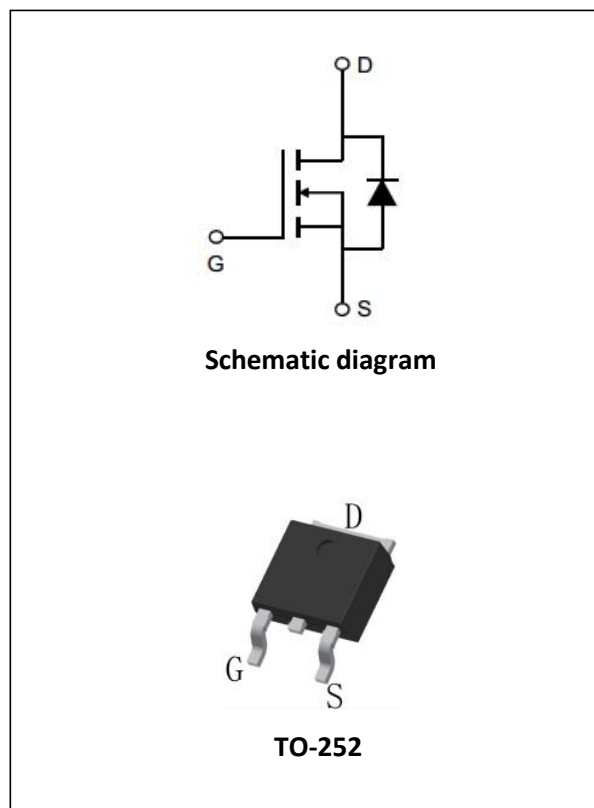
Ordering Codes	Package	Product Code	Packing
MDT19N10L	TO-252	MDT19N10L	Reel

Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	19	A
Drain Current-Pulsed (Note 1)	I_{DM}	50	A
Maximum Power Dissipation($T_c=25^\circ C$)	P_D	31	W
Single pulse avalanche energy (Note 2)	E_{AS}	21	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	4.8	$^\circ C/W$
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Electrical Characteristics (TA=25℃ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1	1.8	2.4	V
Drain-Source On-State Resistance ^(Note 3)	R _{DS(ON)}	V _{GS} =10V, I _D =5A	-	80	90	mΩ
		V _{GS} =4.5V, I _D =5A		90	115	
Forward Transconductance	g _{FS}	V _{DS} =25V, I _D =3.6A	-	5	-	S
Dynamic Characteristics						
Input Capacitance	C _{ISS}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz	-	680	-	pF
Output Capacitance	C _{OSS}		-	110	-	pF
Reverse Transfer Capacitance	C _{RSS}		-	85	-	pF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =50V, I _D =5A, V _{GS} =10V, R _{GEN} =2.5Ω	-	10	-	nS
Turn-on Rise Time	t _r		-	7	-	nS
Turn-Off Delay Time	t _{d(off)}		-	34	-	nS
Turn-Off Fall Time	t _f			9	-	nS
Total Gate Charge	Q _g	V _{DS} =80V, I _D =3A V _{GS} =10V	-	16	-	nC
Gate-Source Charge	Q _{GS}		-	4	-	nC
Gate-Drain Charge	Q _{gd}		-	5	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _S =19A	-	-	1.2	V

Notes:

- 1.Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2.EAS condition : T_j=25℃, V_{DD}=50V, V_{GS}=10V, L=0.5mH, R_g=25Ω
- 3.Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
- 4.Guaranteed by design, not subject to production.

Characteristics Curves

Figure 1 Output Characteristics

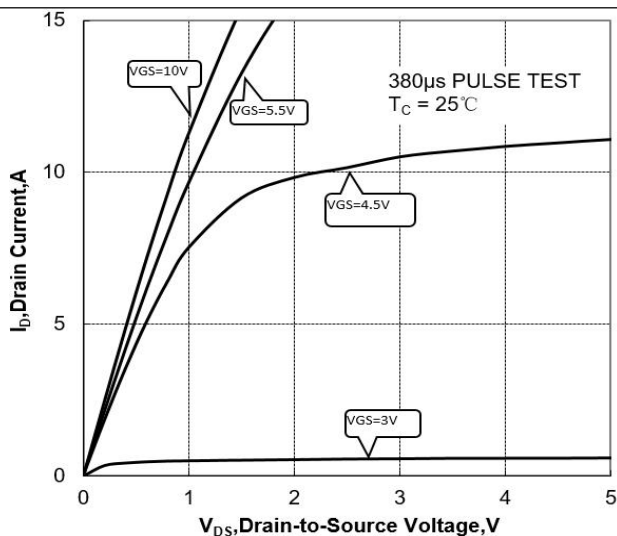


Figure 2 Transfer Characteristics

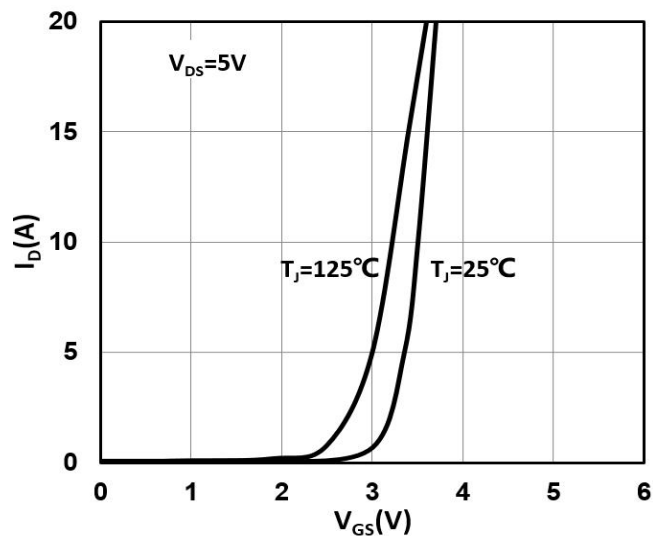


Figure 3 On-Resistance vs. I_D and V_{GS}

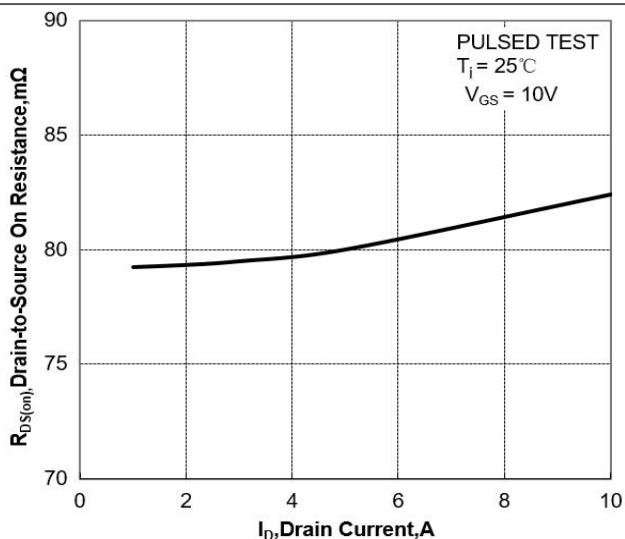


Figure 4 On-Resistance vs. Junction Temperature

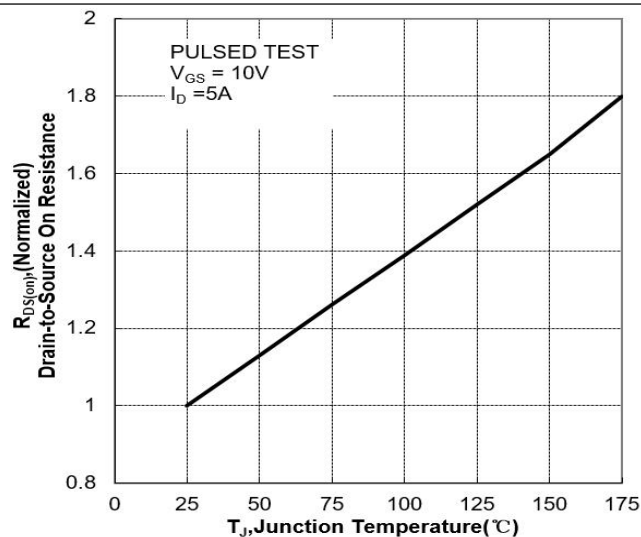


Figure 5 On-Resistance vs. V_{GS}

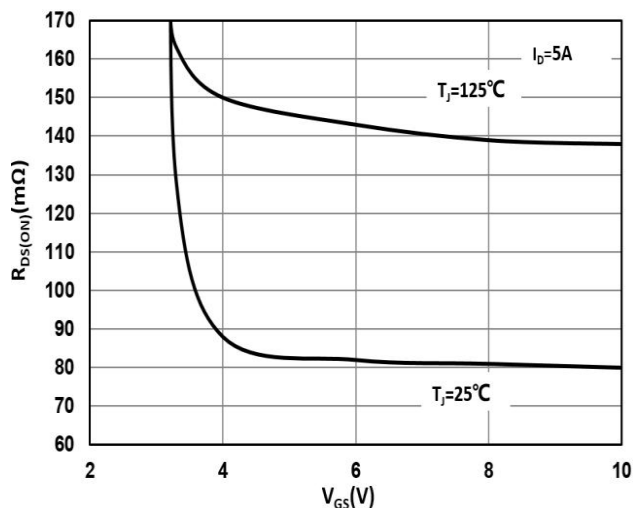


Figure 6 Body Diode Forward Voltage

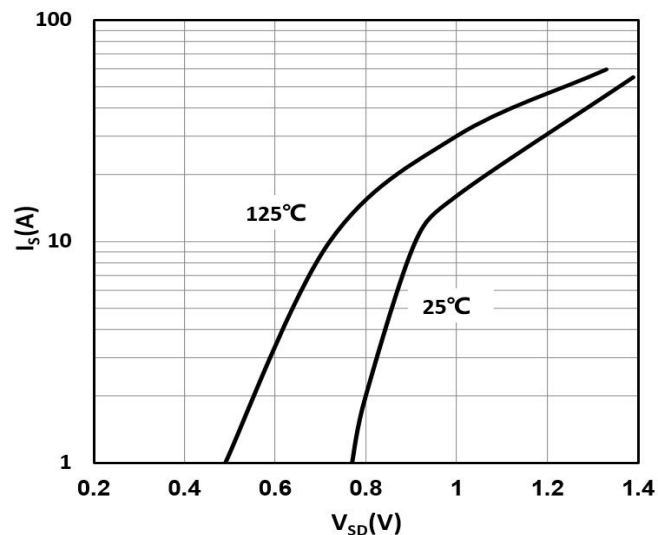


Figure 7 Gate-Charge Characteristics

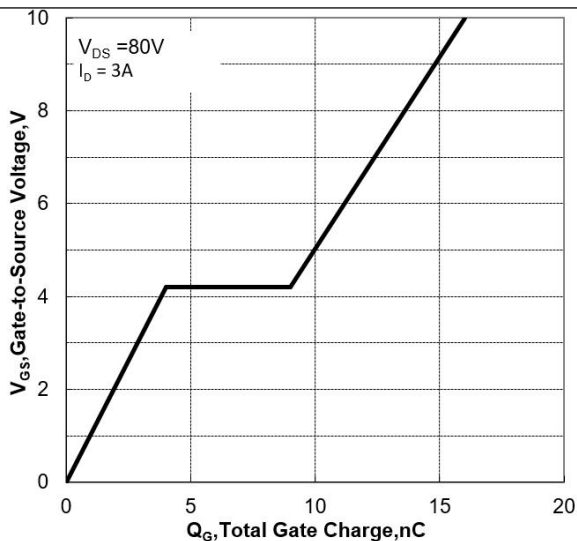


Figure 8 Capacitance Characteristics

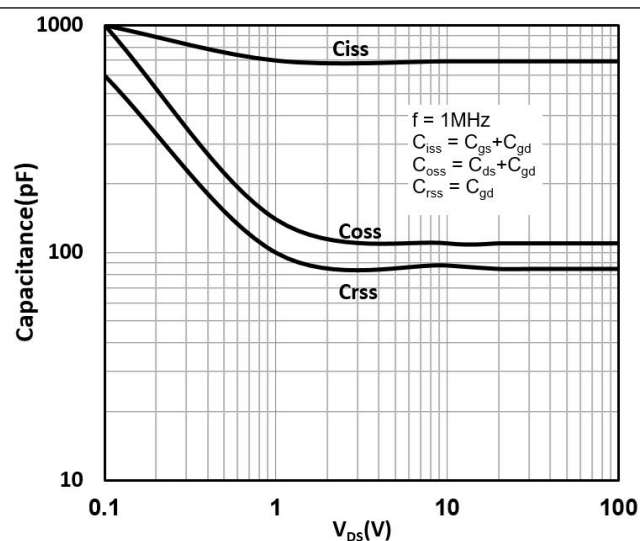


Figure 9 Maximum Forward Biased Safe Operation Area

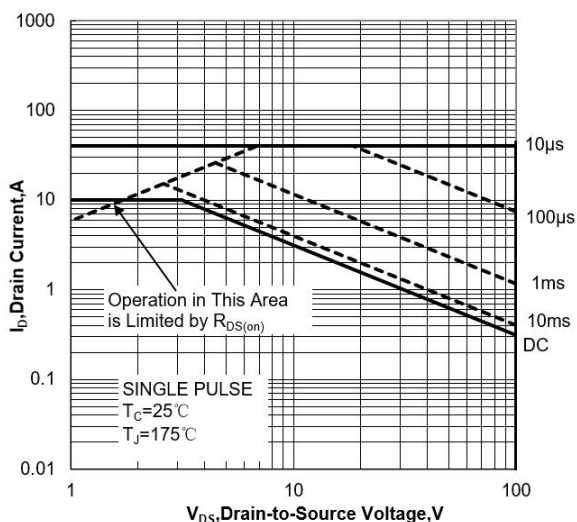


Figure 10 Single Pulse Power Rating Junction-to-Ambient

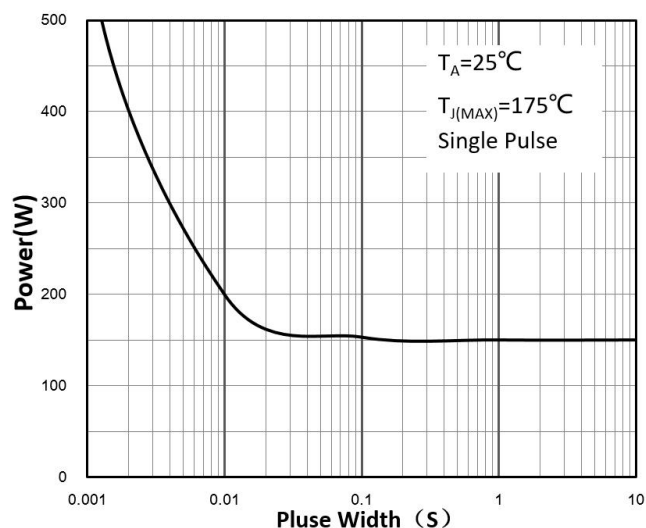
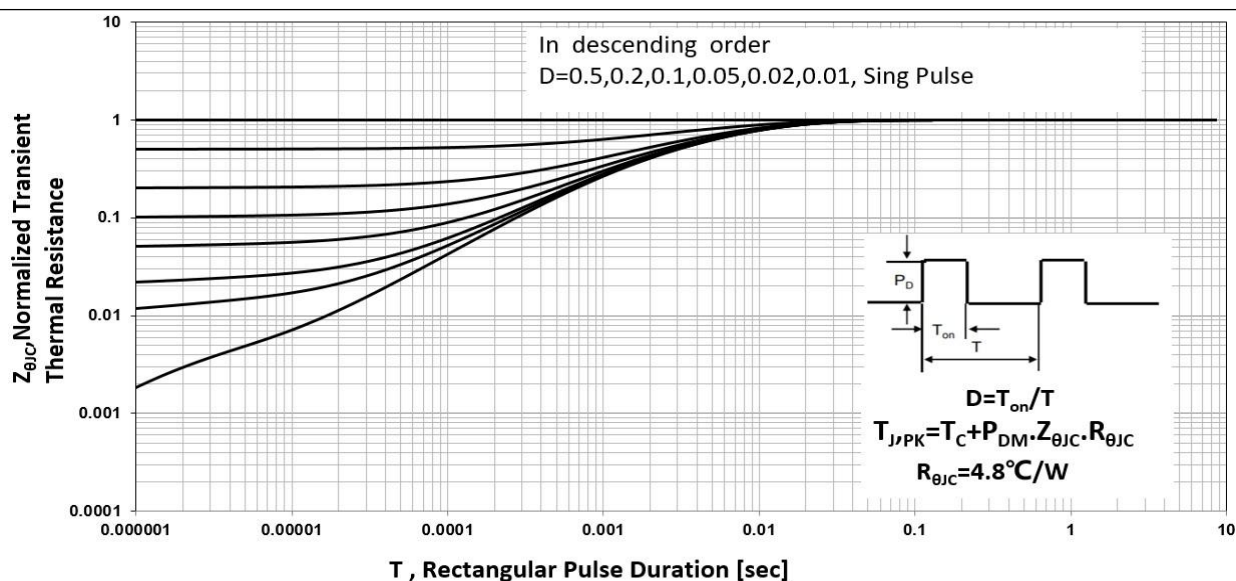
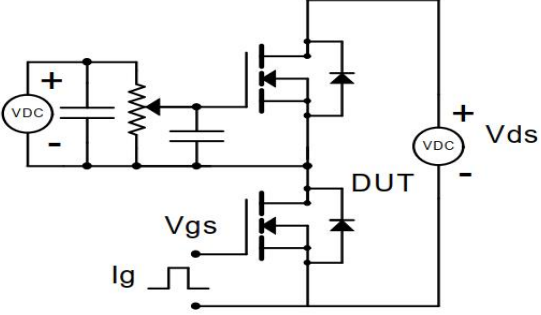
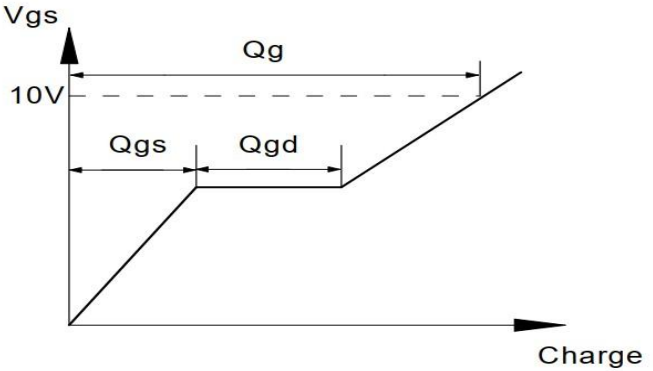
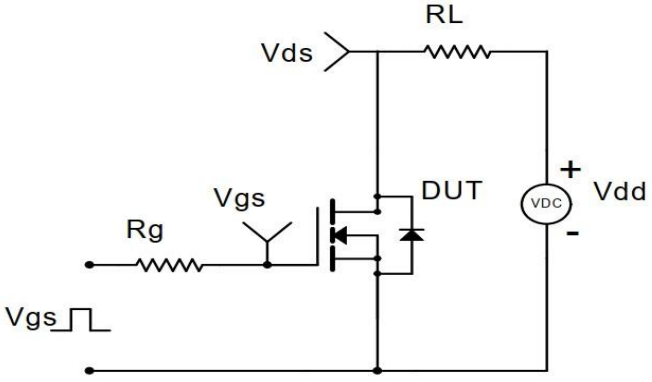
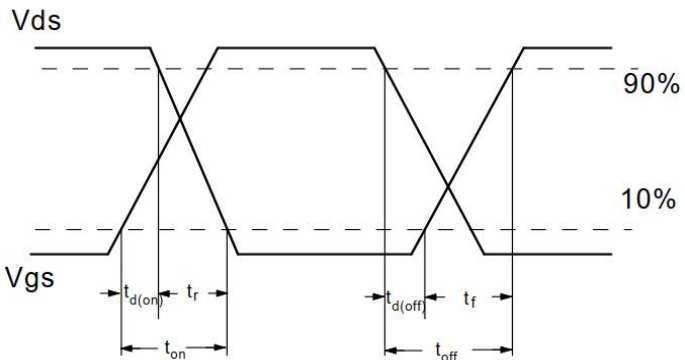
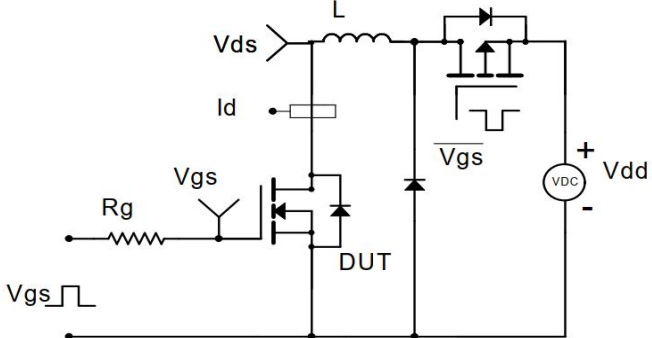
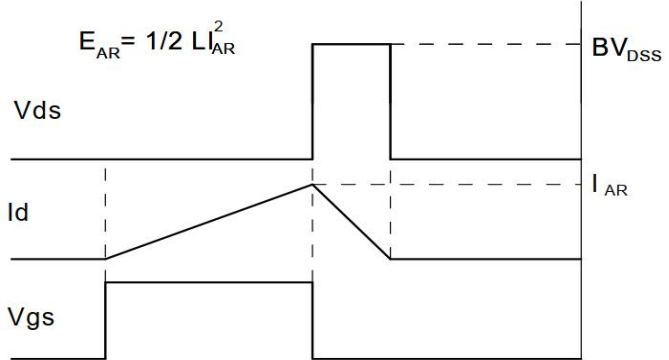
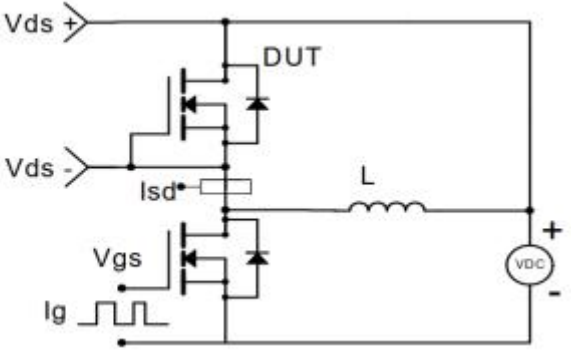
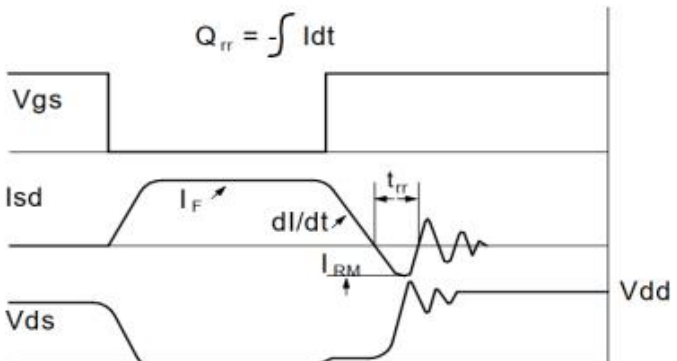


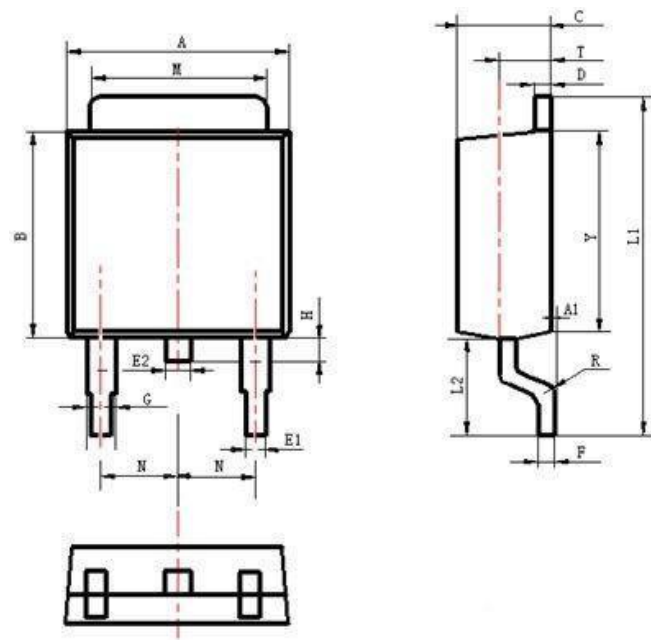
Figure 11 Normalized Maximum Transient Thermal Impedance



Test Circuit and Waveform

Gate Charge Test Circuit	Gate Charge Test Waveform
 The diagram shows a MOSFET (DUT) with its gate connected to a pulse generator (Vgs) through a gate resistor (Rg). The drain is connected to a load resistor (RL) and a DC voltage source (Vds). The source is connected to ground. A current source (Ig) is connected to the gate.	 The waveform shows the gate voltage (Vgs) versus charge (Qg). The gate voltage rises from 0V to 10V. The total gate charge is Qg. The gate charge is divided into three regions: Qgs (gate-source charge), Qgd (gate-drain charge), and Qg (total gate charge).
Resistive Switching Test Circuit	Resistive Switching Test Waveforms
 The diagram shows a MOSFET (DUT) with its gate connected to a pulse generator (Vgs) through a gate resistor (Rg). The drain is connected to a load resistor (RL) and a DC voltage source (Vdd). The source is connected to ground.	 The waveforms show the drain voltage (Vds) and gate voltage (Vgs) versus time. The gate voltage (Vgs) is a square wave. The drain voltage (Vds) is a trapezoidal wave. The switching times are defined as: t_{d(on)} (delay time), t_r (rise time), t_{d(off)} (delay time), t_f (fall time), t_{on} (on time), and t_{off} (off time). The Vds levels are marked at 90% and 10%.
Unclamped Inductive Switching (UIS) Test Circuit	Unclamped Inductive Switching (UIS) Test Waveforms
 The diagram shows a MOSFET (DUT) with its gate connected to a pulse generator (Vgs) through a gate resistor (Rg). The drain is connected to an inductor (L) and a DC voltage source (Vdd). The source is connected to ground. A diode is connected in parallel with the inductor.	 The waveforms show the drain voltage (Vds), drain current (Id), and gate voltage (Vgs) versus time. The gate voltage (Vgs) is a square wave. The drain current (Id) is a triangular wave. The drain voltage (Vds) is a trapezoidal wave. The energy stored in the inductor is given by the equation: $E_{AR} = \frac{1}{2} L I_{AR}^2$. The Vds levels are marked at BV_{DSS} and I_{AR}.
Diode Recovery Test Circuit	Diode Recovery Test Waveforms
 The diagram shows a MOSFET (DUT) with its gate connected to a pulse generator (Vgs) through a gate resistor (Rg). The drain is connected to an inductor (L) and a DC voltage source (Vdd). The source is connected to ground. A diode is connected in parallel with the inductor.	 The waveforms show the gate voltage (Vgs), drain current (Id), and drain voltage (Vds) versus time. The gate voltage (Vgs) is a square wave. The drain current (Id) is a triangular wave. The drain voltage (Vds) is a trapezoidal wave. The reverse recovery time (t_{rr}) is defined as the time from the end of the forward current to the point where the reverse current is equal to I_{RM}. The equation for reverse recovery charge is: $Q_{rr} = \int Idt$.

Package Description



Items	Values(mm)	
	MIN	MAX
A	6.30	6.90
A1	0	0.13
B	5.70	6.30
C	2.10	2.50
D	0.30	0.60
E1	0.60	0.90
E2	0.70	1.00
F	0.30	0.60
G	0.70	1.20
L1	9.60	10.50
L2	2.70	3.10
H	0.60	1.00
M	5.10	5.50
N	2.09	2.49
R	0.3	
T	1.40	1.60
Y	5.10	6.30

TO-252 Package



迈诺斯科技

MDT19N10L

NOTE:

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. Please do not exceed the absolute maximum ratings of the device when circuit designing.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. MOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. Shenzhen Minos reserves the right to make changes in this specification sheet and is subject to change without prior notice.

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