

## 100V N-Channel Power MOSFET

### Description

MDT12N10L, the uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge. It can be used in a wide variety of applications

### KEY CHARACTERISTICS

- ①  $V_{DS}=100V, I_D=12A$   
 $R_{DS(ON)} < 110m\Omega @ V_{GS}=10V$   
 $R_{DS(ON)} < 120m\Omega @ V_{GS}=4.5V$
- ② High density cell design for lower  $R_{dson}$
- ③ Fully characterized avalanche voltage and current
- ④ Good stability and uniformity with high EAS
- ⑤ Excellent package for good heat dissipation

### APPLICATIONS

- ① Power switching application
- ② Hard switched and High frequency circuits
- ③ Uninterruptible power supply

### ORDERING INFORMATION

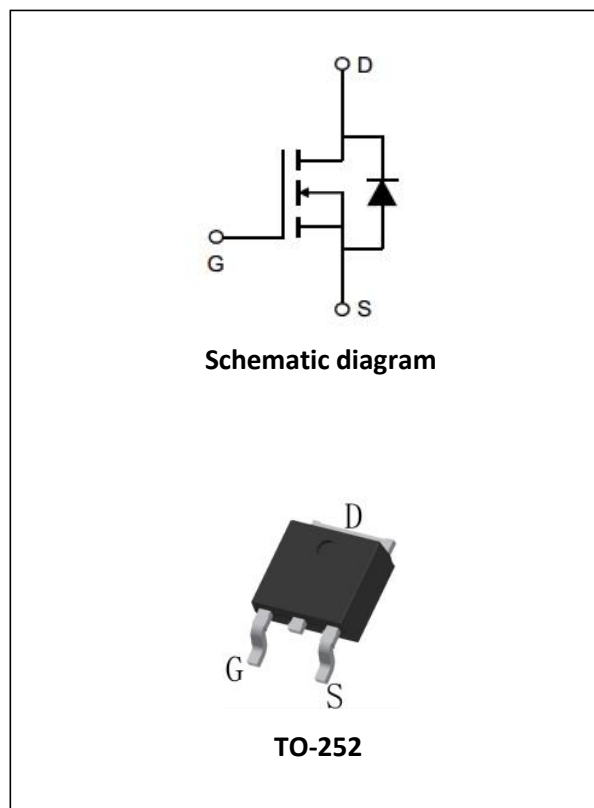
| Ordering Codes | Package | Product Code | Packing |
|----------------|---------|--------------|---------|
| MDT12N10L      | TO-252  | MDT12N10L    | Reel    |

### Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

| Parameter                                         | Symbol         | Limit      | Unit       |
|---------------------------------------------------|----------------|------------|------------|
| Drain-Source Voltage                              | $V_{DS}$       | 100        | V          |
| Gate-Source Voltage                               | $V_{GS}$       | $\pm 20$   | V          |
| Drain Current-Continuous                          | $I_D$          | 12         | A          |
| Drain Current-Pulsed <sup>(Note 1)</sup>          | $I_{DM}$       | 40         | A          |
| Maximum Power Dissipation( $T_c=25^\circ C$ )     | $P_D$          | 31         | W          |
| Single pulse avalanche energy <sup>(Note 2)</sup> | $E_{AS}$       | 21         | mJ         |
| Operating Junction and Storage Temperature Range  | $T_J, T_{STG}$ | -55 To 175 | $^\circ C$ |

### Thermal Characteristic

|                                     |                 |     |              |
|-------------------------------------|-----------------|-----|--------------|
| Thermal Resistance,Junction-to-Case | $R_{\theta JC}$ | 4.8 | $^\circ C/W$ |
|-------------------------------------|-----------------|-----|--------------|



## Electrical Characteristics (TA=25℃ unless otherwise noted)

| Parameter                                            | Symbol              | Condition                                                                                 | Min | Typ | Max  | Unit |
|------------------------------------------------------|---------------------|-------------------------------------------------------------------------------------------|-----|-----|------|------|
| Off Characteristics                                  |                     |                                                                                           |     |     |      |      |
| Drain-Source Breakdown Voltage                       | BV <sub>DSS</sub>   | V <sub>GS</sub> =0V I <sub>D</sub> =250μA                                                 | 100 | -   | -    | V    |
| Zero Gate Voltage Drain Current                      | I <sub>DSS</sub>    | V <sub>DS</sub> =100V, V <sub>GS</sub> =0V                                                | -   | -   | 1    | μA   |
| Gate-Body Leakage Current                            | I <sub>GSS</sub>    | V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V                                                | -   | -   | ±100 | nA   |
| On Characteristics                                   |                     |                                                                                           |     |     |      |      |
| Gate Threshold Voltage                               | V <sub>GS(th)</sub> | V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA                                  | 1   | 1.8 | 2.4  | V    |
| Drain-Source On-State Resistance <sup>(Note 3)</sup> | R <sub>DS(ON)</sub> | V <sub>GS</sub> =10V, I <sub>D</sub> =5A                                                  | -   | 90  | 110  | mΩ   |
|                                                      |                     | V <sub>GS</sub> =4.5V, I <sub>D</sub> =5A                                                 |     | 110 | 120  |      |
| Forward Transconductance                             | g <sub>FS</sub>     | V <sub>DS</sub> =25V, I <sub>D</sub> =3.6A                                                | -   | 5   | -    | S    |
| Dynamic Characteristics                              |                     |                                                                                           |     |     |      |      |
| Input Capacitance                                    | C <sub>ISS</sub>    | V <sub>DS</sub> =25V, V <sub>GS</sub> =0V,<br>f=1.0MHz                                    | -   | 680 | -    | pF   |
| Output Capacitance                                   | C <sub>OSS</sub>    |                                                                                           | -   | 110 | -    | pF   |
| Reverse Transfer Capacitance                         | C <sub>rss</sub>    |                                                                                           | -   | 85  | -    | pF   |
| Switching Characteristics <sup>(Note 4)</sup>        |                     |                                                                                           |     |     |      |      |
| Turn-on Delay Time                                   | t <sub>d(on)</sub>  | V <sub>DD</sub> =50V, I <sub>D</sub> =5A,<br>V <sub>GS</sub> =10V, R <sub>GEN</sub> =2.5Ω | -   | 10  | -    | nS   |
| Turn-on Rise Time                                    | t <sub>r</sub>      |                                                                                           | -   | 7   | -    | nS   |
| Turn-Off Delay Time                                  | t <sub>d(off)</sub> |                                                                                           | -   | 34  | -    | nS   |
| Turn-Off Fall Time                                   | t <sub>f</sub>      |                                                                                           |     | 9   | -    | nS   |
| Total Gate Charge                                    | Q <sub>g</sub>      | V <sub>DS</sub> =80V, I <sub>D</sub> =3A<br>V <sub>GS</sub> =10V                          | -   | 16  | -    | nC   |
| Gate-Source Charge                                   | Q <sub>GS</sub>     |                                                                                           | -   | 4   | -    | nC   |
| Gate-Drain Charge                                    | Q <sub>gd</sub>     |                                                                                           | -   | 5   | -    | nC   |
| Drain-Source Diode Characteristics                   |                     |                                                                                           |     |     |      |      |
| Diode Forward Voltage                                | V <sub>SD</sub>     | V <sub>GS</sub> =0V, I <sub>S</sub> =12A                                                  | -   | -   | 1.2  | V    |

### Notes:

- 1.Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2.EAS condition : T<sub>j</sub>=25℃, V<sub>DD</sub>=50V, V<sub>GS</sub>=10V, L=0.5mH, R<sub>g</sub>=25Ω
- 3.Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
- 4.Guaranteed by design, not subject to production.

## Characteristics Curves

Figure 1 Output Characteristics

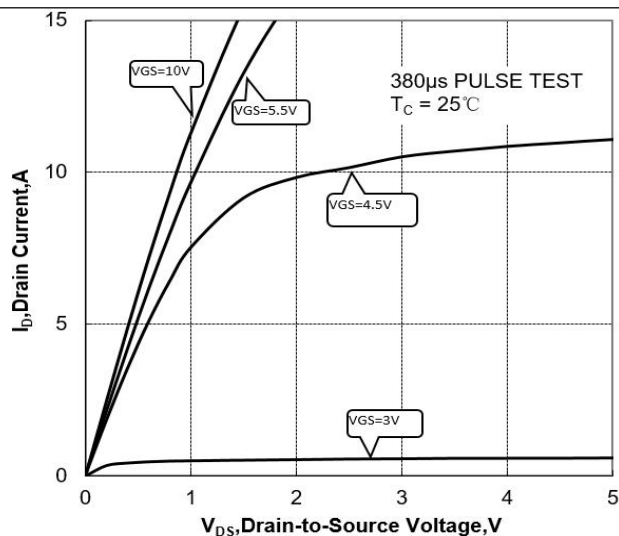


Figure 2 Transfer Characteristics

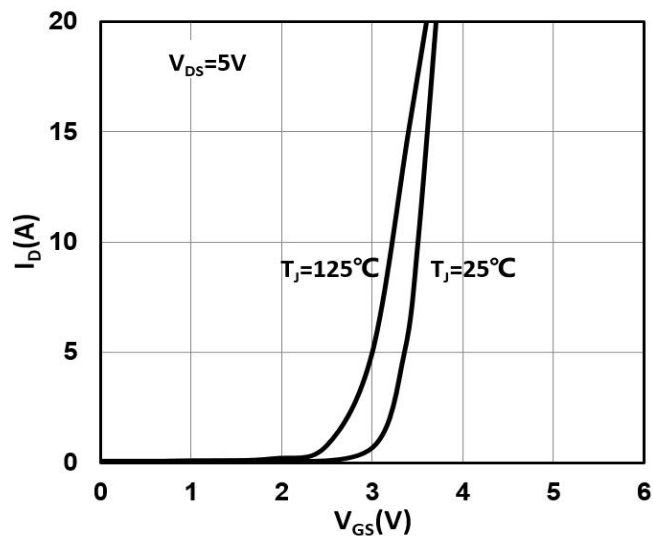


Figure 3 On-Resistance vs. ID and VGS

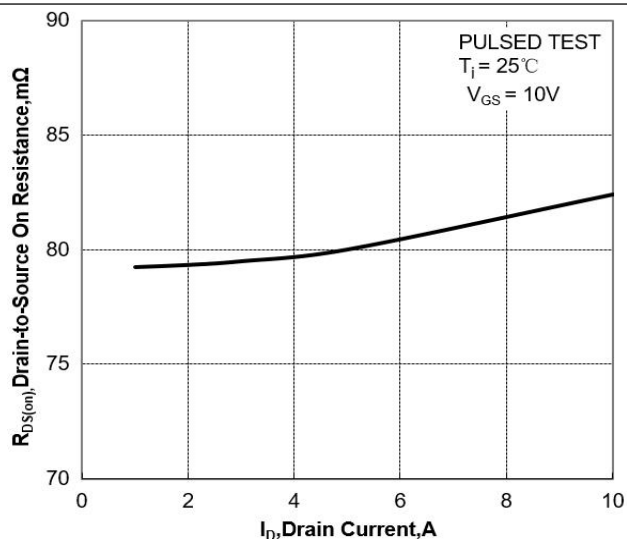


Figure 4 On-Resistance vs. Junction Temperature

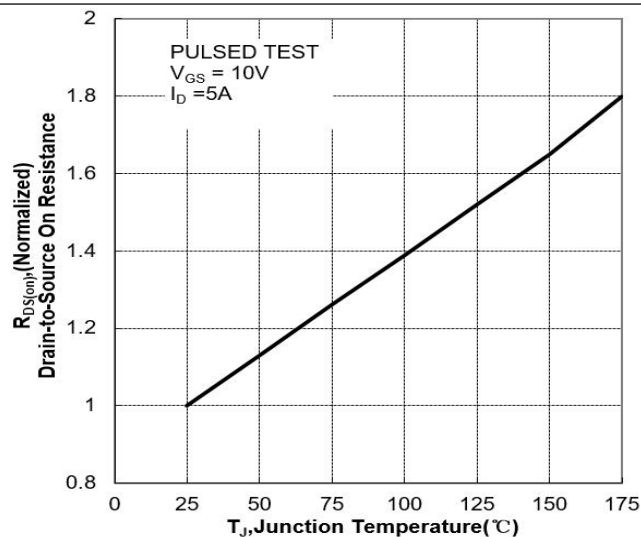


Figure 5 On-Resistance vs. VGS

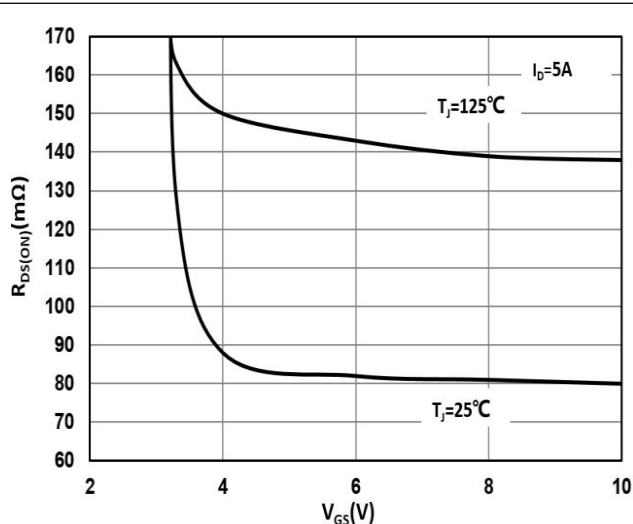


Figure 6 Body Diode Forward Voltage

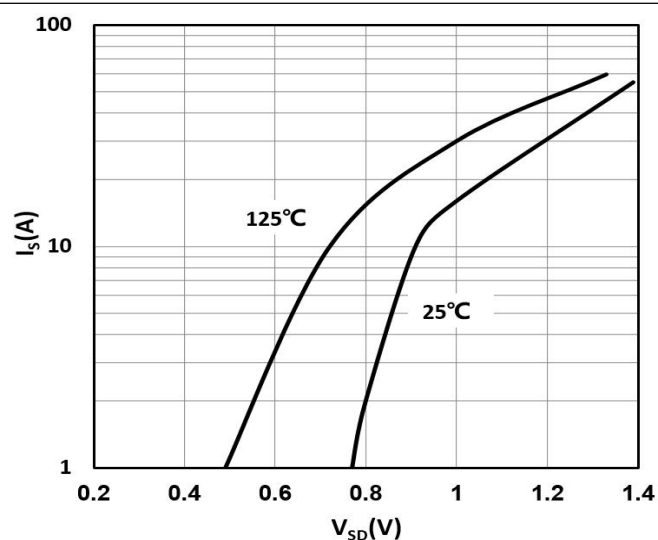


Figure 7 Gate-Charge Characteristics

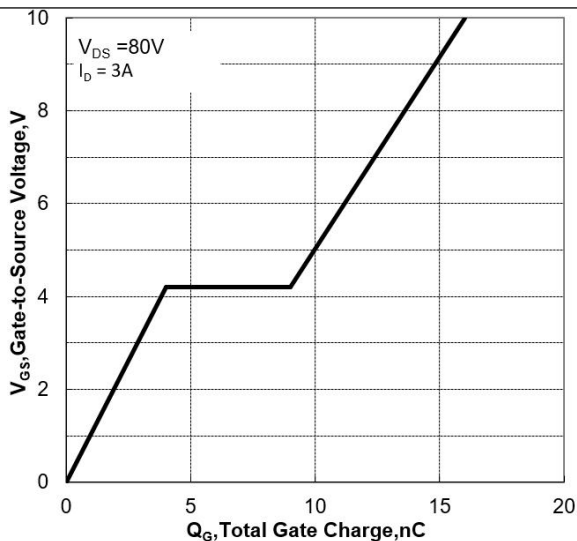


Figure 8 Capacitance Characteristics

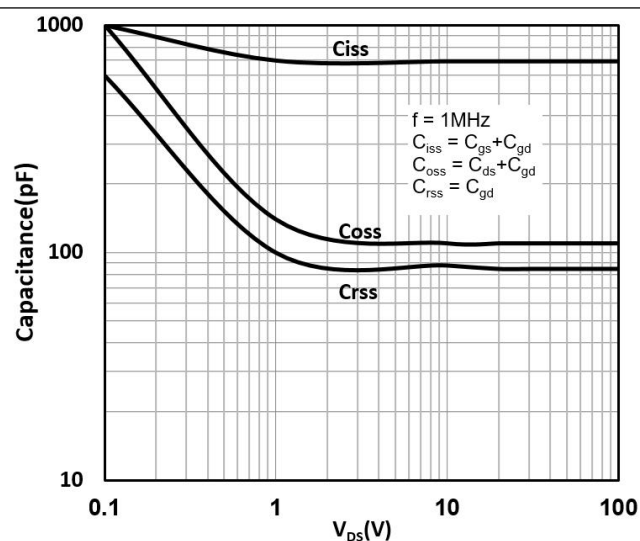


Figure 9 Maximum Forward Biased Safe Operation Area

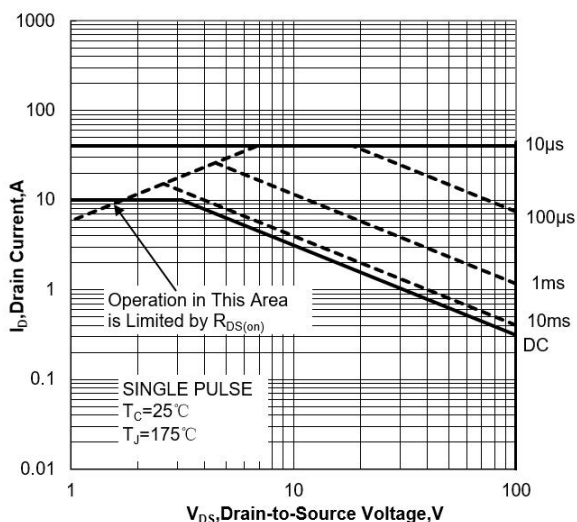


Figure 10 Single Pulse Power Rating Junction-to-Ambient

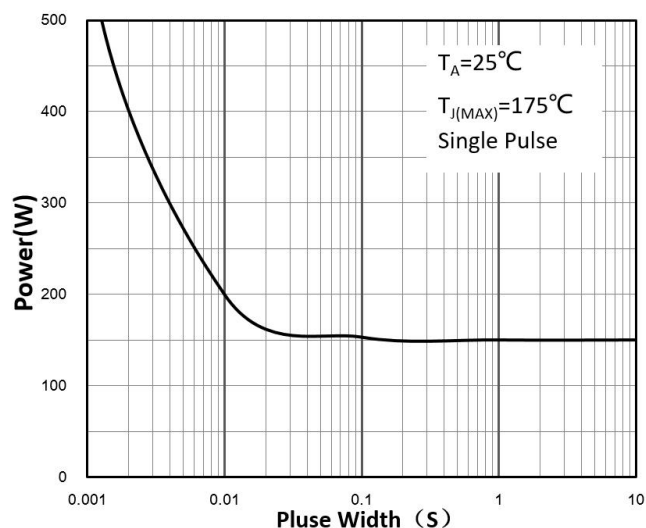
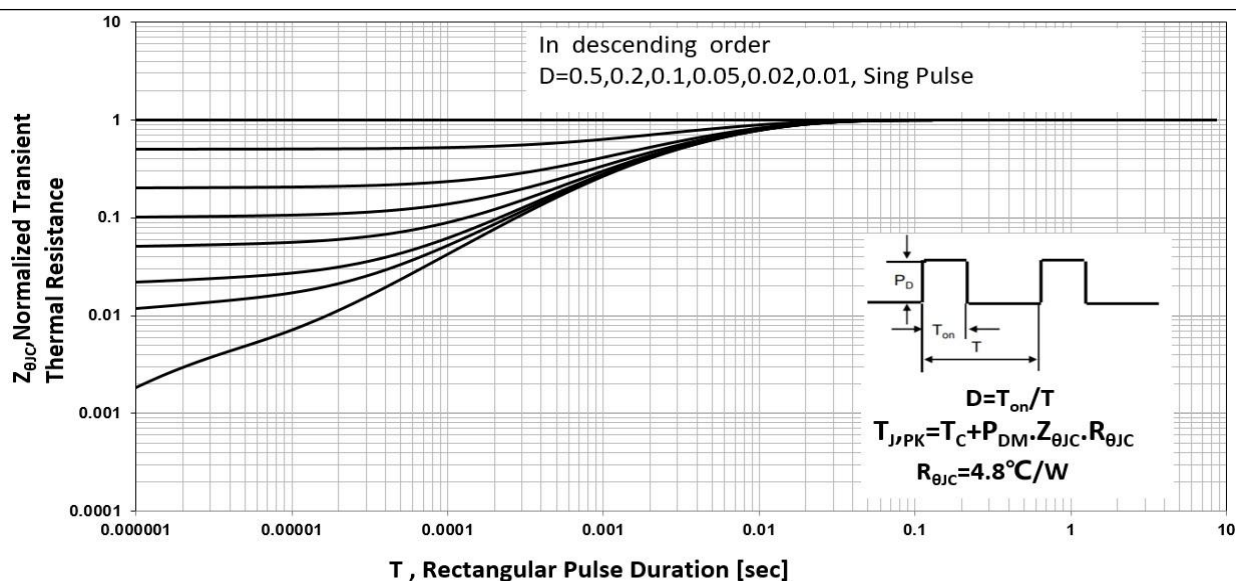
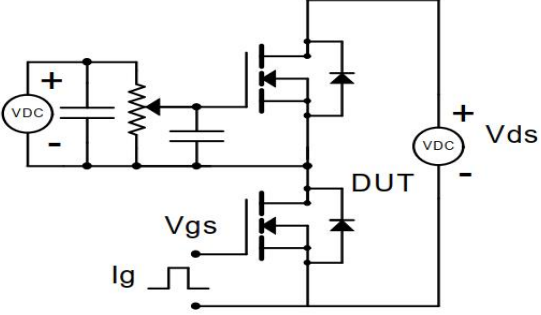
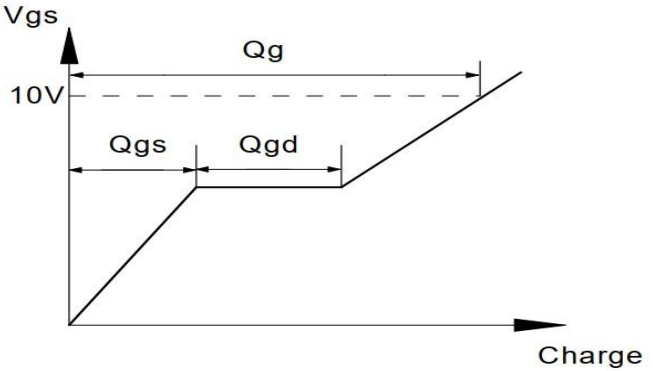
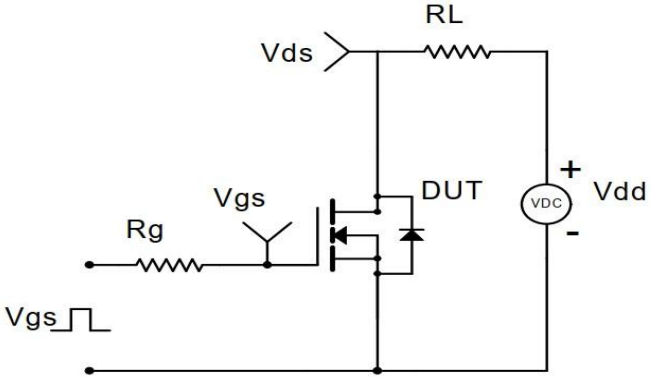
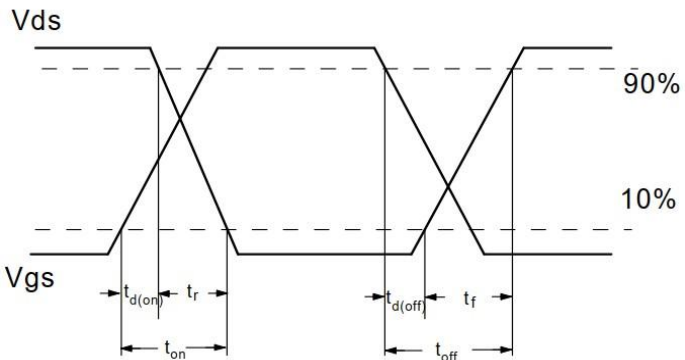
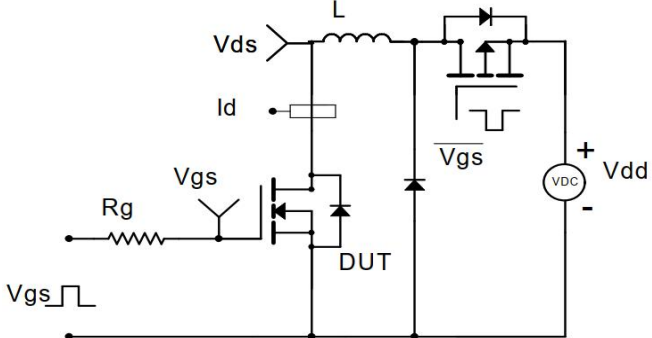
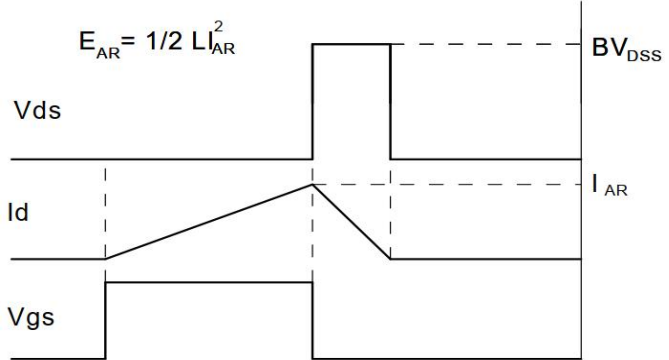
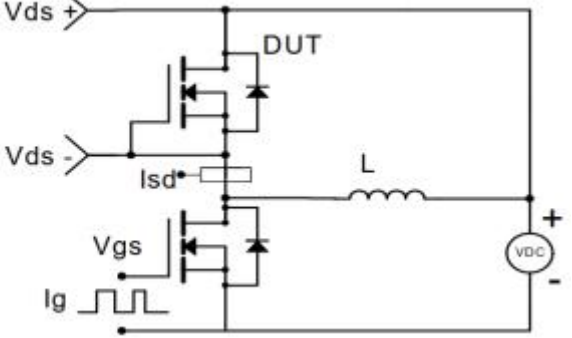
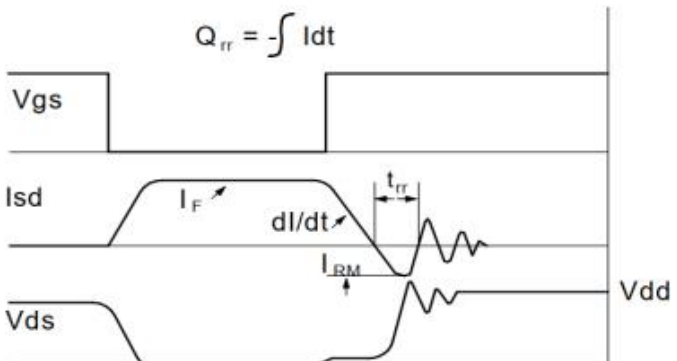


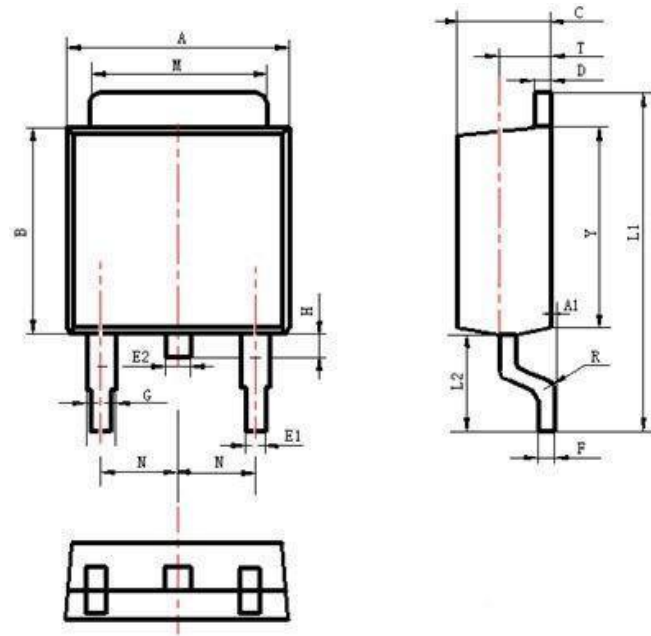
Figure 11 Normalized Maximum Transient Thermal Impedance



# Test Circuit and Waveform

| Gate Charge Test Circuit                                                                                                                                                                                                                                                                                                                                                     | Gate Charge Test Waveform                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  <p>The diagram shows a MOSFET (DUT) with its gate connected to a pulse generator (Vgs) through a gate resistor (Rg). The drain is connected to a load resistor (RL) and a DC voltage source (Vds). The source is connected to ground. A current source (Ig) is connected to the gate.</p>  |  <p>The waveform shows the gate voltage (Vgs) versus charge (Qg). The voltage rises linearly from 0V to 10V, then remains constant at 10V for a period, and finally falls linearly back to 0V. The total charge is Qg, the charge during the rising edge is Qgs, and the charge during the falling edge is Qgd.</p>                                                                                                                                   |
| Resistive Switching Test Circuit                                                                                                                                                                                                                                                                                                                                             | Resistive Switching Test Waveforms                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|  <p>The diagram shows a MOSFET (DUT) with its gate connected to a pulse generator (Vgs) through a gate resistor (Rg). The drain is connected to a load resistor (RL) and a DC voltage source (Vdd). The source is connected to ground.</p>                                                 |  <p>The waveforms show the drain voltage (Vds) and gate voltage (Vgs) versus time. The gate voltage (Vgs) is a square wave. The drain voltage (Vds) is a trapezoidal wave. The switching times are labeled: t<sub>d(on)</sub> (delay time), t<sub>r</sub> (rise time), t<sub>d(off)</sub> (delay time), t<sub>f</sub> (fall time), t<sub>on</sub> (turn-on time), and t<sub>off</sub> (turn-off time). The Vds levels are marked at 90% and 10%.</p> |
| Unclamped Inductive Switching (UIS) Test Circuit                                                                                                                                                                                                                                                                                                                             | Unclamped Inductive Switching (UIS) Test Waveforms                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|  <p>The diagram shows a MOSFET (DUT) with its gate connected to a pulse generator (Vgs) through a gate resistor (Rg). The drain is connected to an inductor (L) and a DC voltage source (Vdd). The source is connected to ground. A diode is connected in parallel with the inductor.</p>  |  <p>The waveforms show the drain voltage (Vds), drain current (Id), and gate voltage (Vgs) versus time. The gate voltage (Vgs) is a square wave. The drain current (Id) is a triangular wave. The drain voltage (Vds) is a trapezoidal wave. The energy stored in the inductor is given by the equation: <math>E_{AR} = 1/2 L I_{AR}^2</math>. The Vds levels are marked at BV<sub>DSS</sub> and I<sub>AR</sub>.</p>                                |
| Diode Recovery Test Circuit                                                                                                                                                                                                                                                                                                                                                  | Diode Recovery Test Waveforms                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|  <p>The diagram shows a MOSFET (DUT) with its gate connected to a pulse generator (Vgs) through a gate resistor (Rg). The drain is connected to an inductor (L) and a DC voltage source (Vdd). The source is connected to ground. A diode is connected in parallel with the inductor.</p> |  <p>The waveforms show the gate voltage (Vgs), drain current (Id), and drain voltage (Vds) versus time. The gate voltage (Vgs) is a square wave. The drain current (Id) is a triangular wave. The drain voltage (Vds) is a trapezoidal wave. The reverse recovery time (t<sub>rr</sub>) is labeled. The equation for reverse recovery charge is given: <math>Q_{rr} = \int Idt</math>. The Vds levels are marked at Vdd and I<sub>RM</sub>.</p>     |

## Package Description



| Items | Values(mm) |       |
|-------|------------|-------|
|       | MIN        | MAX   |
| A     | 6.30       | 6.90  |
| A1    | 0          | 0.13  |
| B     | 5.70       | 6.30  |
| C     | 2.10       | 2.50  |
| D     | 0.30       | 0.60  |
| E1    | 0.60       | 0.90  |
| E2    | 0.70       | 1.00  |
| F     | 0.30       | 0.60  |
| G     | 0.70       | 1.20  |
| L1    | 9.60       | 10.50 |
| L2    | 2.70       | 3.10  |
| H     | 0.60       | 1.00  |
| M     | 5.10       | 5.50  |
| N     | 2.09       | 2.49  |
| R     | 0.3        |       |
| T     | 1.40       | 1.60  |
| Y     | 5.10       | 6.30  |

TO-252 Package



迈诺斯科技

**MDT12N10L**

**NOTE:**

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. Please do not exceed the absolute maximum ratings of the device when circuit designing.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. MOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. Shenzhen Minos reserves the right to make changes in this specification sheet and is subject to change without prior notice.

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