

- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology
- ★ 100% EAS Guaranteed

Product Summary

RoHS

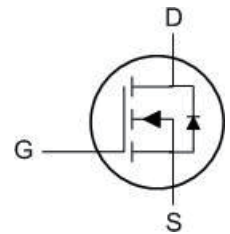
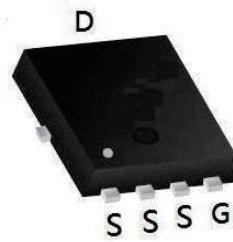
BVDSS	RDS(on)	ID
30V	8mΩ	30A

Description

The 30N03D is the high cell density trenched N-ch MOSFETs, which provide excellent $R_{DS(on)}$ and gate charge for most of the synchronous buck converter applications.

The 30N03D meet the RoHS and Green Product, requirement 100% EAS guaranteed with full function reliability approved.

PDFN3*3 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	30	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	20	A
I_{DM}	Pulsed Drain Current ²	90	A
E_{AS}	Single Pulse Avalanche Energy ³	39	mJ
I_{AS}	Avalanche Current	30	A
$P_D@T_C=25^\circ C$	Total Power Dissipation ⁴	15	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	85	$^\circ C/W$

Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=1mA$	-	0.034	-	V/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=7A$	-	8	12	$m\Omega$
		$V_{GS}=4.5V, I_D=4A$	-	11	18	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.2	1.5	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		-	-3.84	-	mV/ $^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=24V, V_{GS}=0V, T_J=25^\circ\text{C}$	-	-	1	μA
		$V_{DS}=24V, V_{GS}=0V, T_J=55^\circ\text{C}$	-	-	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS} = \pm 20V, V_{DS}=0V$	-	-	± 100	nA
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$	-	1.04	2.1	Ω
Q_g	Total Gate Charge (4.5V)	$V_{DS}=15V, V_{GS}=4.5V, I_D=7A$	-	8.4	-	nC
Q_{gs}	Gate-Source Charge		-	3.1	-	
Q_{gd}	Gate-Drain Charge		-	2.8	-	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=15V, V_{GS}=10V, R_G=3.3\Omega, I_D=7A$	-	2.4	-	ns
T_r	Rise Time		-	72	-	
$T_{d(off)}$	Turn-Off Delay Time		-	36	-	
T_f	Fall Time		-	14.4	-	
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1MHz$	-	816	-	pF
C_{oss}	Output Capacitance		-	107.8	-	
C_{rss}	Reverse Transfer Capacitance		-	82.6	-	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V$, Force Current	-	-	30	A
I_{SM}	Pulsed Source Current ^{2,5}		-	-	30	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	-	-	1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=20A$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Performance Characteristics

Figure1: Output Characteristics

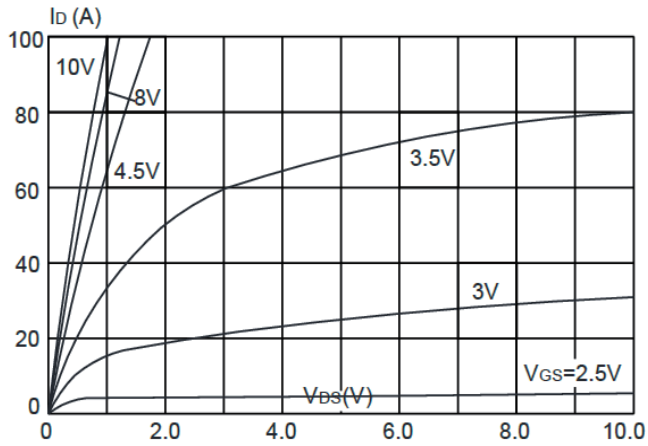


Figure 2: Typical Transfer Characteristics

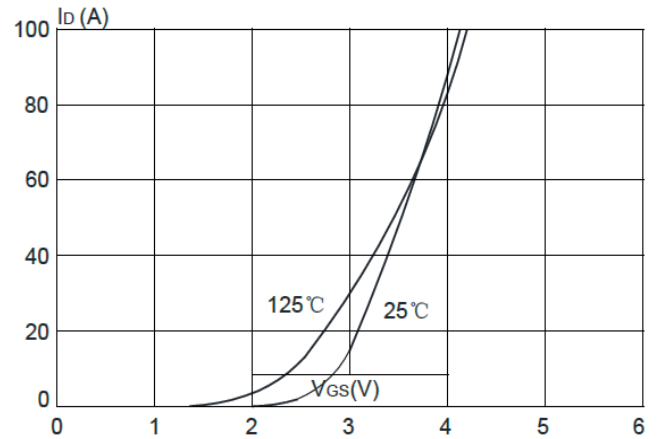


Figure 3: On-resistance vs. Drain Current

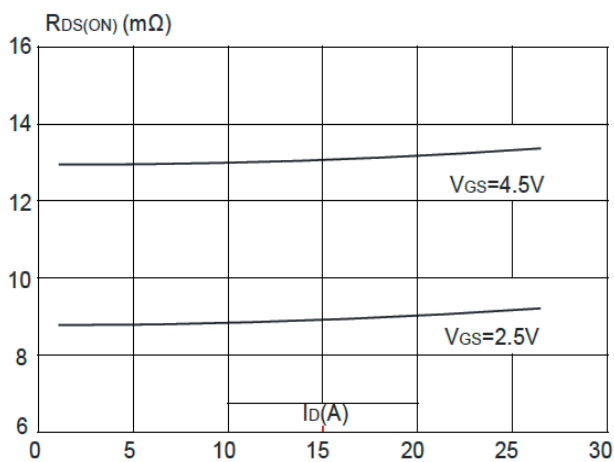


Figure 4: Body Diode Characteristics

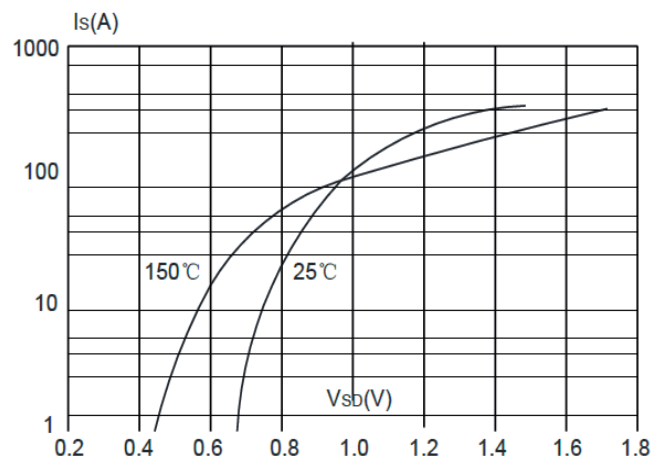


Figure 5: Gate Charge Characteristics

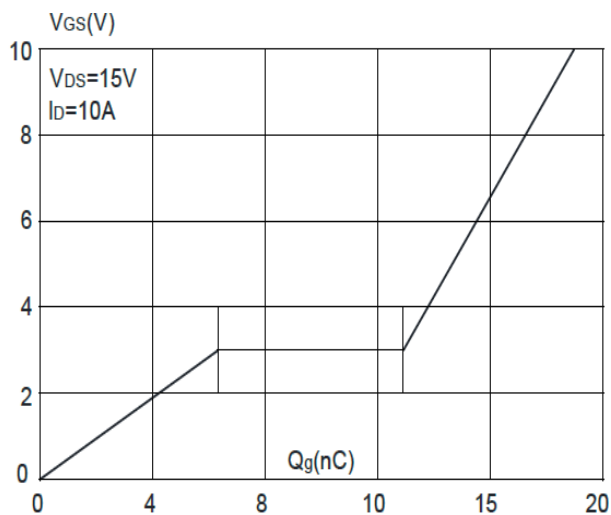
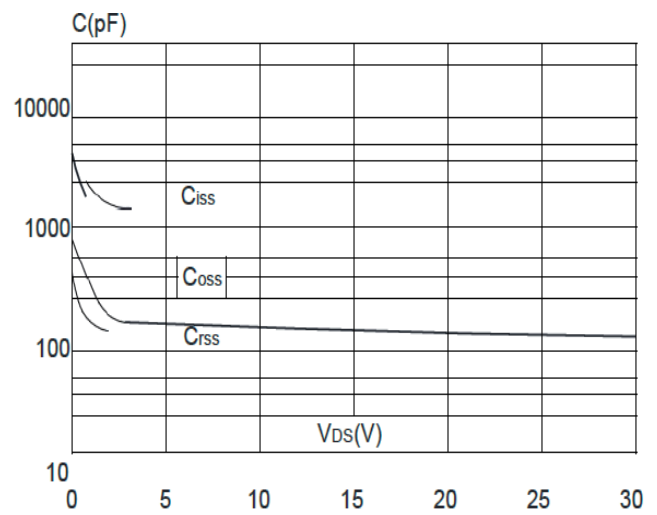


Figure 6: Capacitance Characteristics



Typical Performance Characteristics

Figure 7: Normalized Breakdown Voltage

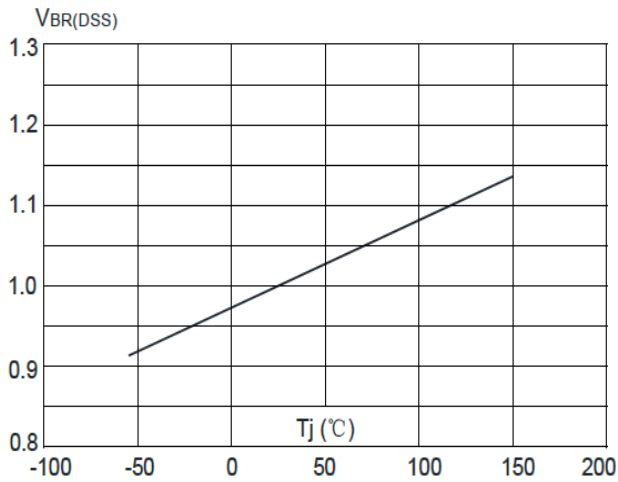


Figure 8: Normalized on Resistance vs. Junction Temperature

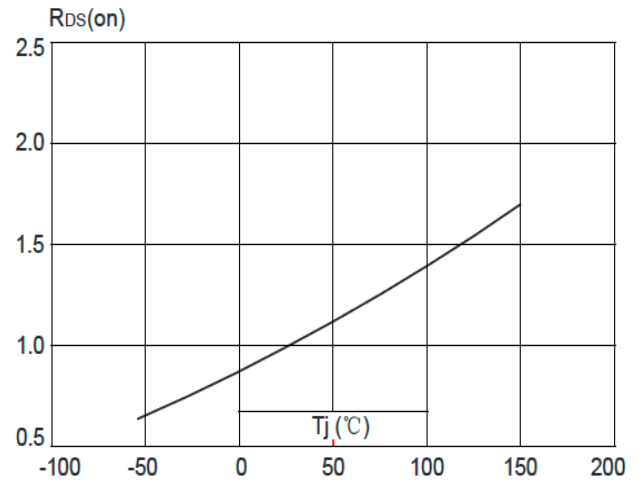


Figure 9: Maximum Safe Operating Area

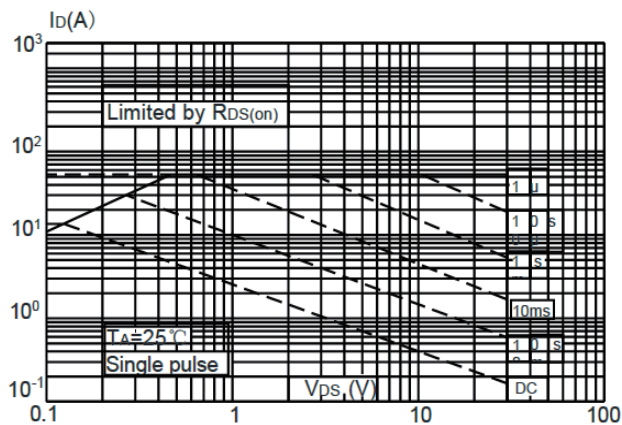


Figure 10: Maximum Continuous Drain Current vs. Temperature

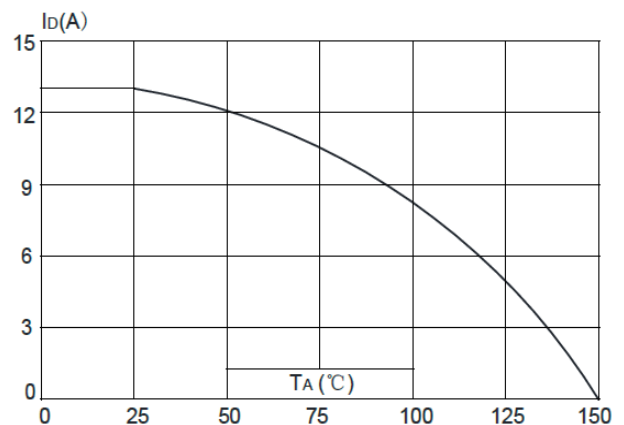
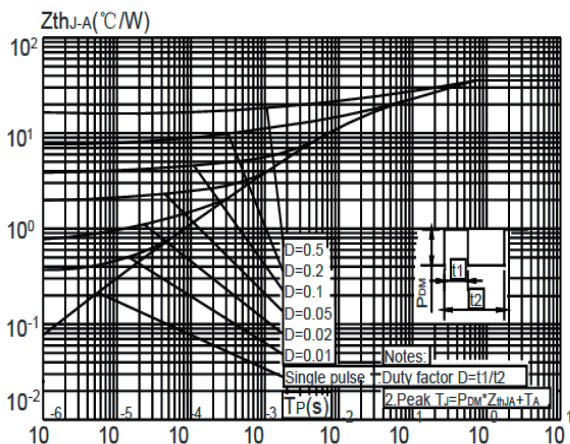


Figure 11: Maximum Effective Transient Thermal Impedance



Test Circuit

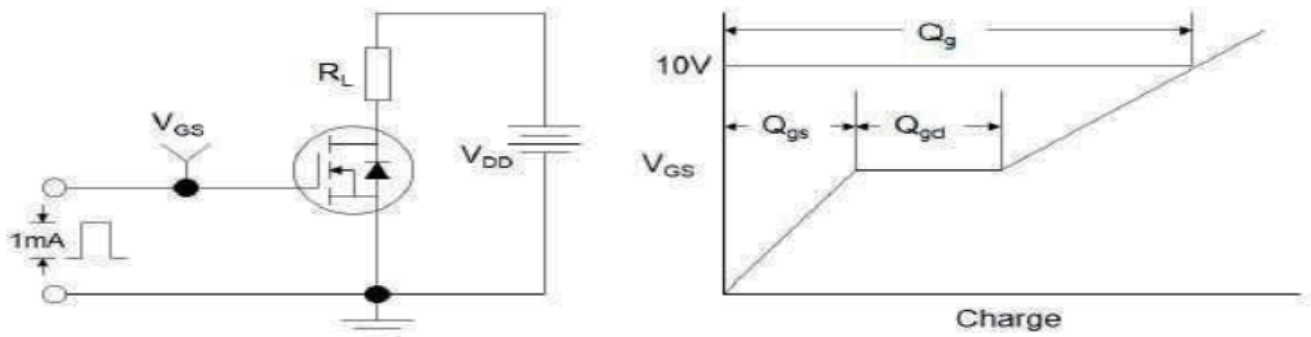


Figure1: Gate Charge Test Circuit & Waveform

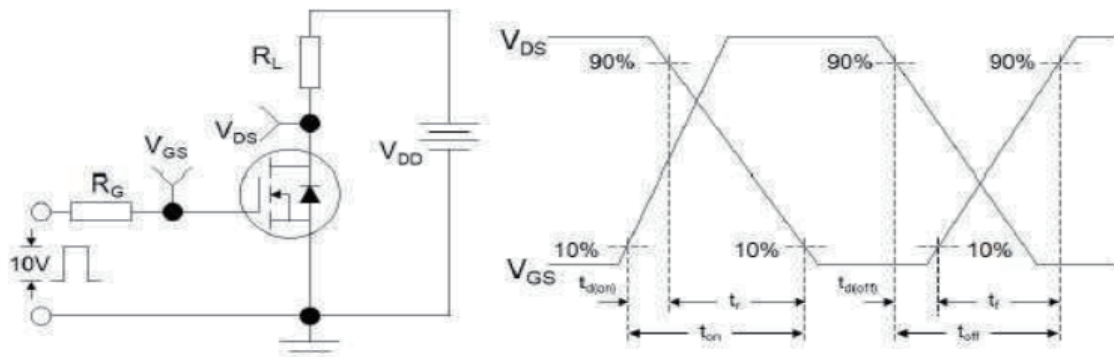


Figure 2: Resistive Switching Test Circuit & Waveforms

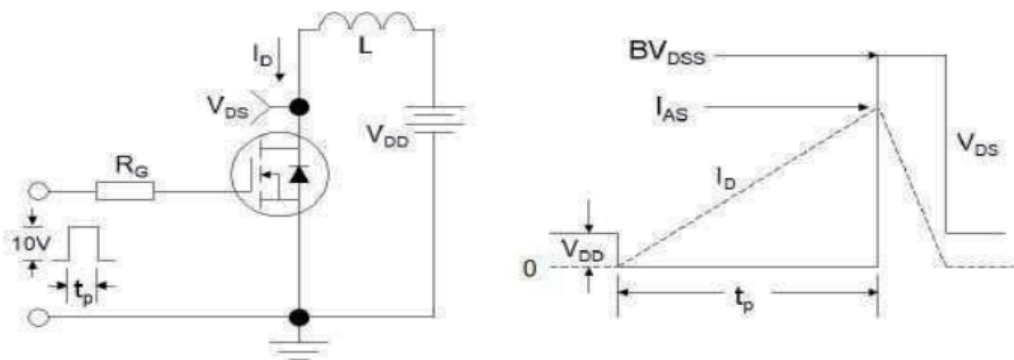


Figure 3: Unclamped Inductive Switching Test Circuit & Waveforms

