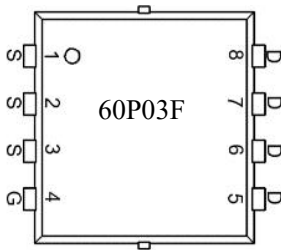
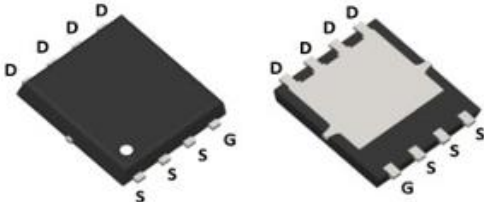
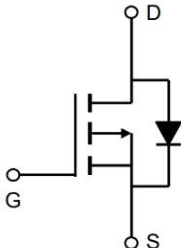


Features ➤ 100% EAS Guaranteed ➤ Green Device Available ➤ Super Low Gate Charge ➤ Excellent CdV/dt effect decline ➤ Advanced high cell density Trenchtechnology	Bvdss	Rdson	ID
	-30V	7.2mΩ	-60A
	Application ➤ Battery switching application ➤ Hard switched and high frequency circuits ➤ Power management		
Package			
			
Marking and pin assignment	PDFN5*6-8L top view		Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
60P03	60P03F	PDFN5*6-8L	5000

Absolute Maximum Ratings ($T_J=25^{\circ}\text{C}$ unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C=25^{\circ}\text{C}$	I_D	-60	A
	$T_C=100^{\circ}\text{C}$	I_D	-35	A
Pulsed Drain Current		I_{DM}^1	-168	A
Single Pulse Avalanche Energy		E_{AS}^2	45	mJ
Power Dissipation	$T_C = 25^{\circ}\text{C}$	P_D	45	W
Operating junction and storage temperature		T_J, T_{STG}	150, -55 ~ 150	$^{\circ}\text{C}$
Maximum Temperature for Soldering		T_L	-	$^{\circ}\text{C}$



Thermal Resistance Ratings

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-Case	$R_{\theta JC}$	3.36	$^{\circ}\text{C/W}$
Thermal resistance, junction – ambient ³	$R_{\theta JA}$	65	$^{\circ}\text{C/W}$

Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	D	S	
HL60P03F	PDFN5*6-8L	4	5,6,7,8	1,2,3	Tape Reel

Electrical Characteristics (T_j=25 $^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30	-	-	V
Gate-body Leakage current	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30V, V_{GS} = 0V$	-	-	-1	μA
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1.0	-	-2.5	V
Drain-Source On-Resistance ⁴	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -30A$	-	7.2	14	m Ω
		$V_{GS} = -4.5V, I_D = -15A$	-	10	22	
Forward Transconductance ⁴	g_{fs}	$V_{DS} = -5V, I_D = -30A$	-	57	-	S
Input Capacitance ⁵	C_{ISS}	$V_{DS} = -15V, V_{GS} = 0V,$ $f = 1MHz$	-	2396	-	pF
Output Capacitance ⁵	C_{OSS}		-	325	-	
Reverse Transfer Capacitance ⁵	C_{RSS}		-	283	-	
Gate Resistance ⁵	R_g	$f = 1MHz$	-	10.5	-	Ω
Total Gate Charge	Q_g	$V_{GS} = -10V, V_{DS} = -15V, I_D = -30A$	-	30	-	nC
Gate-Source Charge	Q_{gs}		-	5	-	
Gate-Drain Charge	Q_{gd}		-	7.5	-	
Turn-On Delay Time	$T_{d(on)}$	$V_{GS} = -10V, V_{DS} = -15V,$ $RG = 3\Omega, I_D = -30A$	-	14.1	-	ns
Rise Time	T_R		-	20	-	
Turn-Off Delay Time	$T_{d(off)}$		-	94	-	
Fall Time	T_F		-	65	-	
Diode Forward Current	I_S	$T_C = 25^{\circ}\text{C}$	-	-	-60	A
Diode Forward Voltage	V_{SD}	$I_S = -1A, V_{GS} = 0V$	-	-	-1.2	V
Reverse Recovery time	T_{rr}	$I_F = -30A,$	-	19	-	ns



Reverse Recovery Charge	Q_{rr}	$di/dt=100A/\mu s$	-	9	-	nC
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Note :

1. Repetitive rating, pulse width limited by junction temperature $T_J(\text{MAX})=150^{\circ}\text{C}$.
2. The EAS data shows Max. rating . The test condition is $V_{DD}=-25V$, $V_{GS}=-10V$, $L=0.1mH$, $I_{AS}=-30A$.
3. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
5. This value is guaranteed by design hence it is not included in the production test.

Typical Performance Characteristics

Fig1:output characteristics

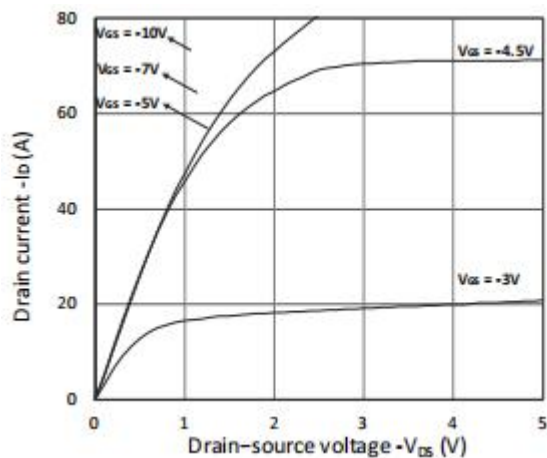


Fig2:Transfer Characteristics

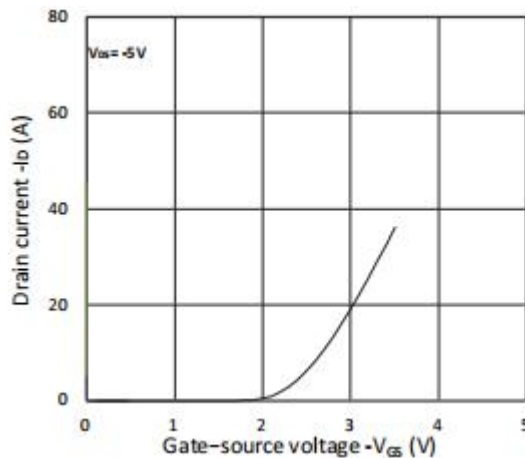


Fig3:Typ.Forward Characteristics of Reverse

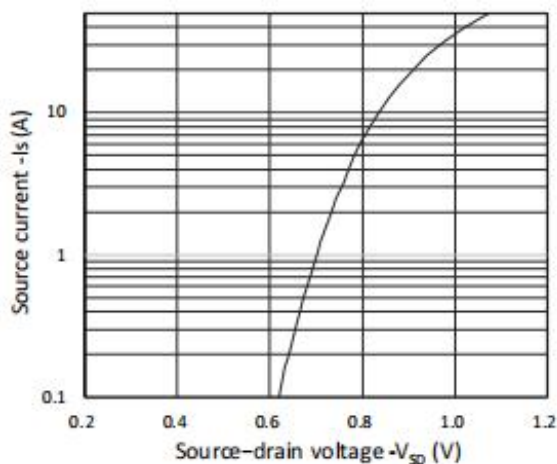


Fig4:4. $R_{DS(ON)}$ vs. V_{GS}

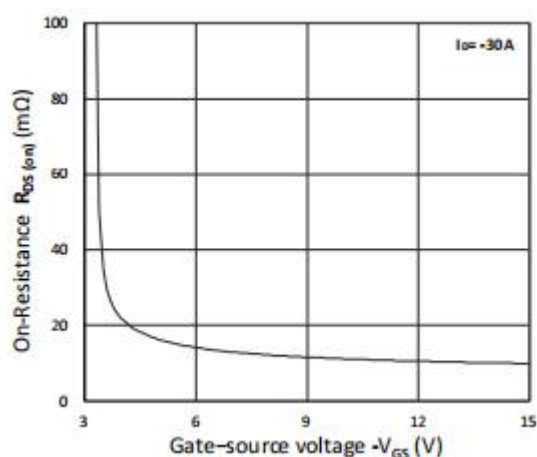


Fig5:Gate $R_{DS(ON)}$ vs. I_D

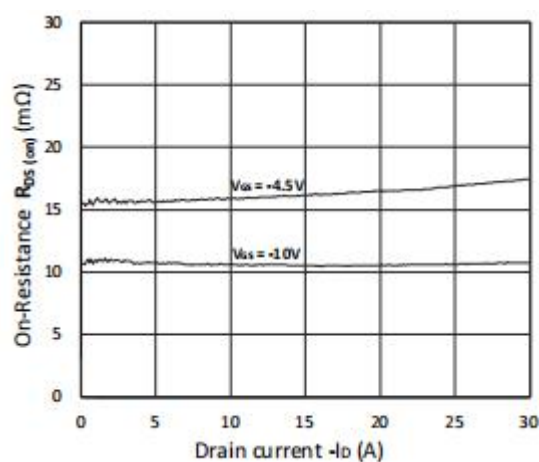


Fig6:Normalized $R_{DS(on)}$ vs. Temperature

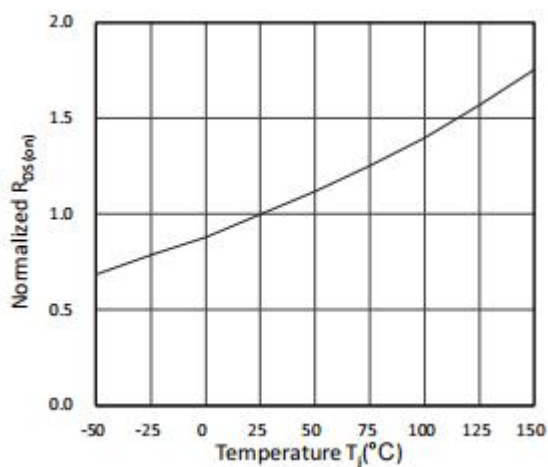


Fig7:Capacitance Characteristics

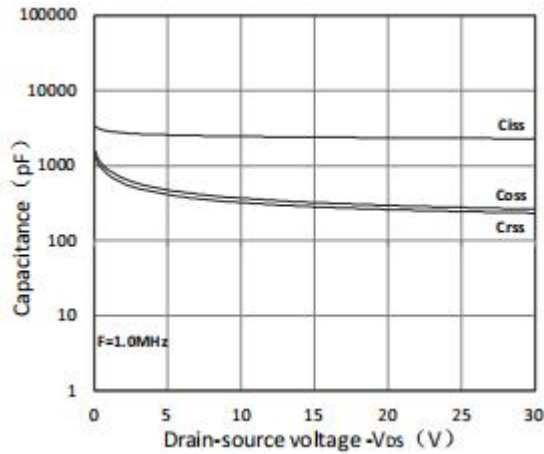


Fig8:Gate Charge Characteristics

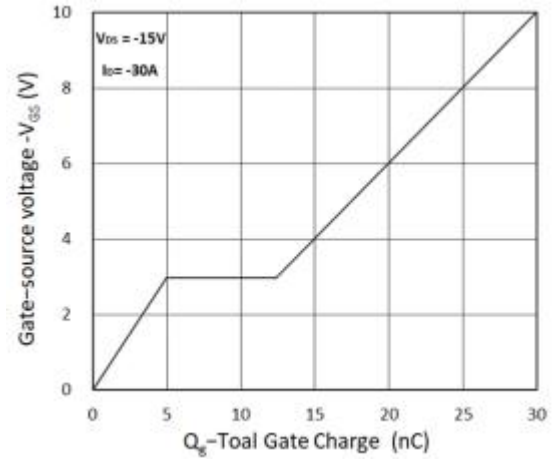


Fig9:Power Dissipation

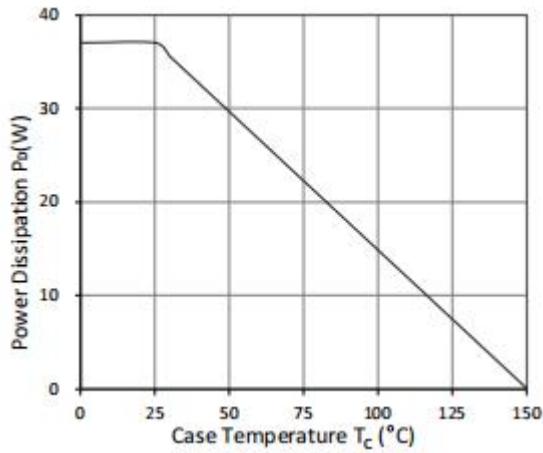


Fig10:Safe Operating Area

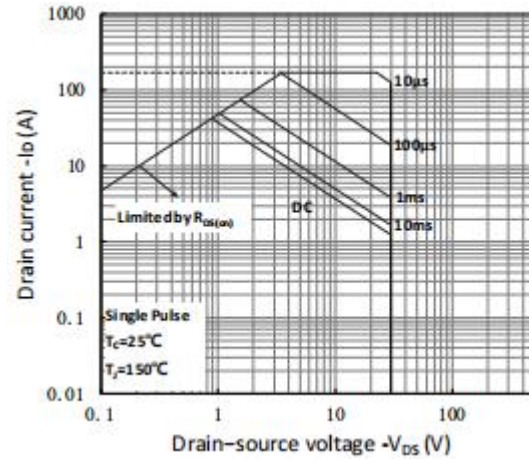
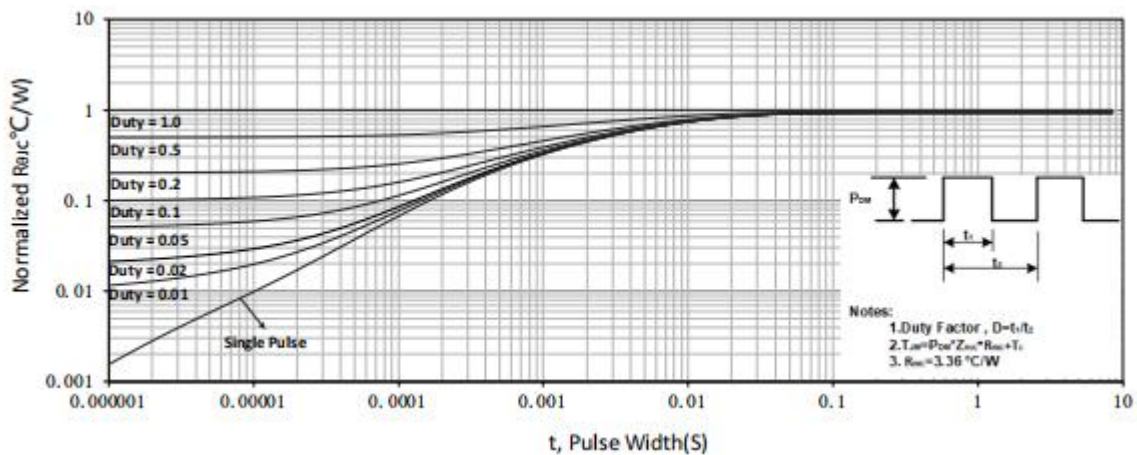
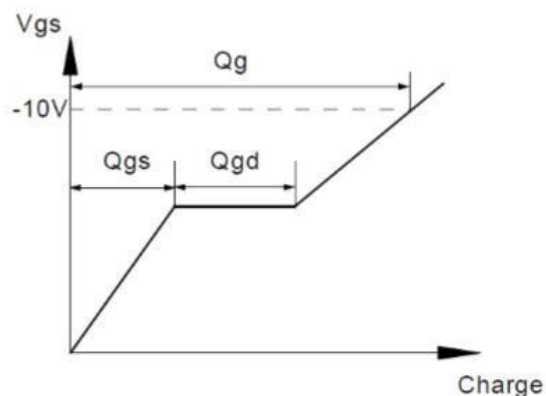
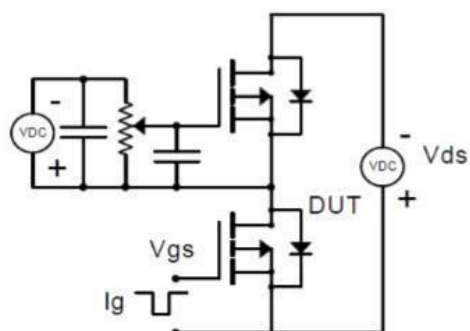


Fig11:Normalized Maximum Transient Thermal Impedance

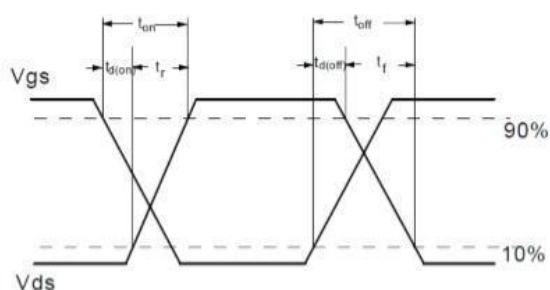
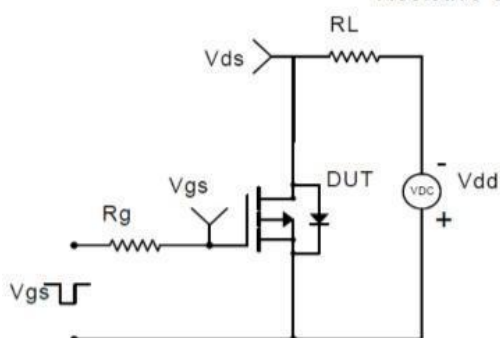


Test Circuit and Waveform

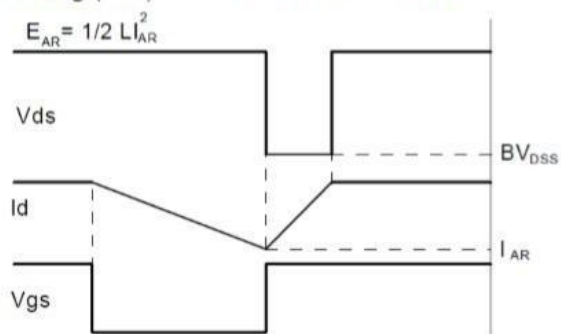
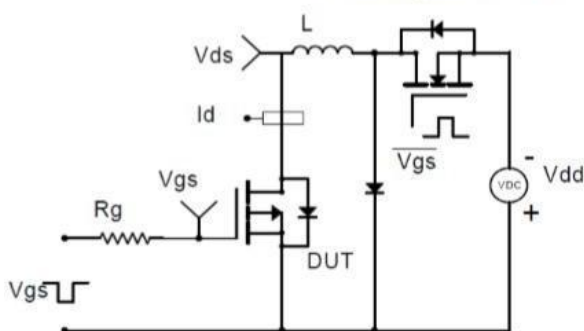
Gate Charge Test Circuit & Waveform



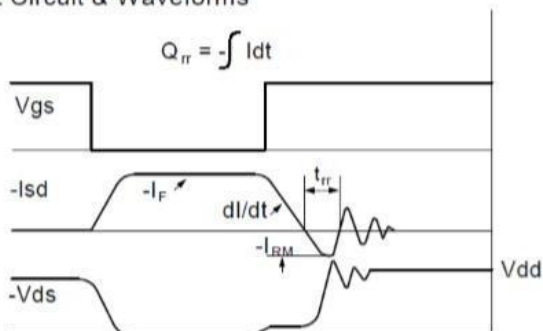
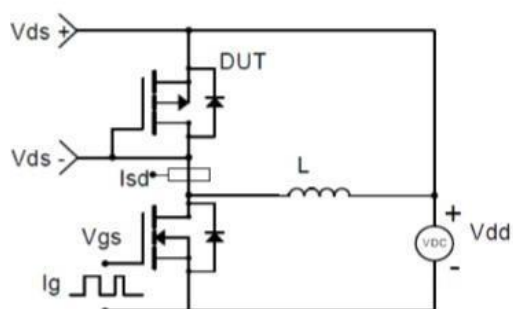
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

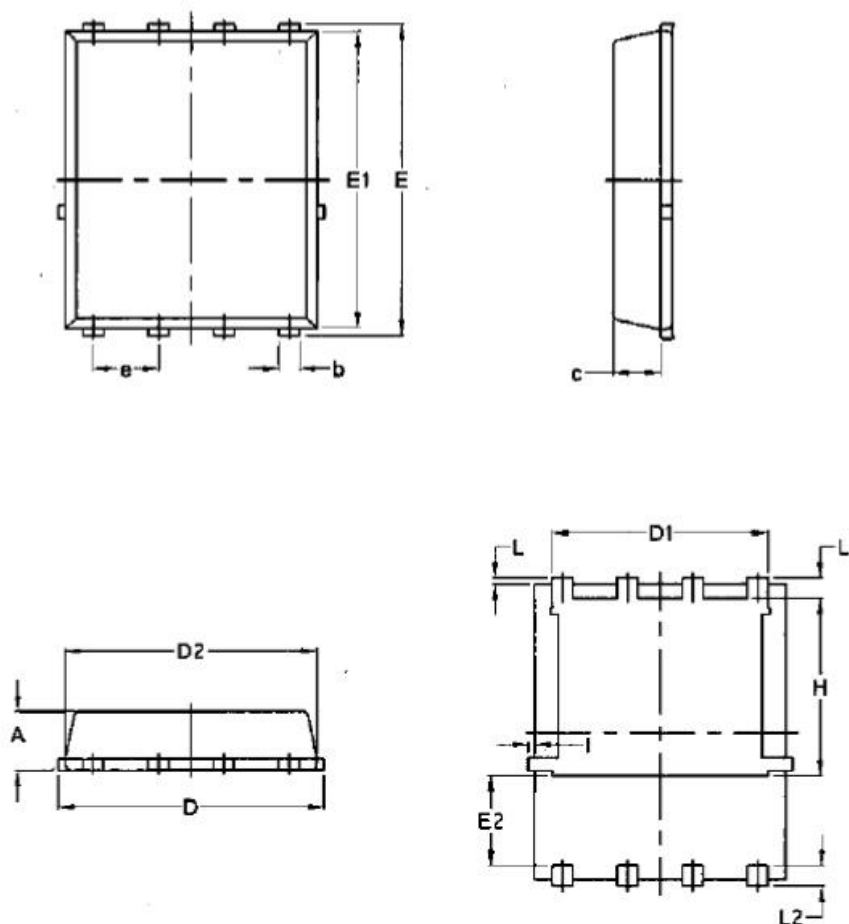


Diode Recovery Test Circuit & Waveforms





Package Dimensions PDFN5*6-8L



Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070



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