

Features

- Operation voltage range: 1.65~5.5V
- Inputs Accept Voltages To 5.5V
- High noise immunity
- Low Power Dissipation
- Max t_{PD} Of 3.2 ns At 5V
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 1000-V Charged-Device Model (C101)
- SOT23-6 Package Available
- SOT363 Package Available

General Description

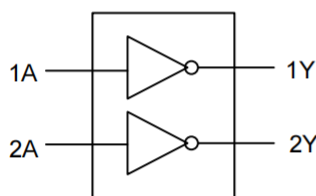
The **74LVC2G04** is a dual inverter gate and it provides the Boolean function $Y = \overline{A}$ in positive logic.

This device has power-down protective circuit to prevent the device from destruction when it is powered down.

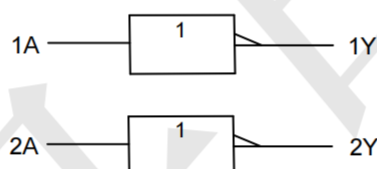
Ordering Information

ORDER NUMBER	PACKAGE DESCRIPTION	PACKAGE OPTION
74LVC2G04GV	SOT23-6	Tape and Reel,3000
74LVC2G04GW	SOT363	Tape and Reel,3000

Logic Diagram

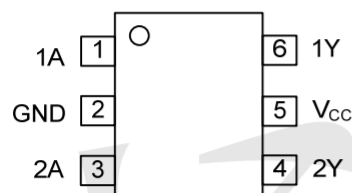


Logic symbol



IEC logic symbol

Pin Configuration



Marking

74LVC2G04GV Marking:V04

74LVC2G04GW Marking:V4

Function Table

INPUT(nA)	OUTPUT(nY)
H	L
L	H

Note: H: HIGH voltage level; L: LOW voltage level.

Absolute Maximum Ratings

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		V_{CC}	-0.5 ~ +6.5	V
Input Voltage		V_{IN}	-0.5 ~ +6.5	V
Output Voltage	Active Mode	V_{OUT}	-0.5 ~ $V_{CC} + 0.5$	V
	Power-Down Mode		-0.5 ~ +6.5	V
V_{CC} or GND Current		I_{CC}	±100	mA
Continuous Output Current ($V_{OUT}=0$ to V_{CC})		I_{OUT}	±50	mA
Input Clamp Current ($V_{IN}<0$)		I_{IK}	-50	mA
Output Clamp Current ($V_{OUT}>V_{CC}$ or $V_{OUT}<0$)		I_{OK}	-50	mA
Power Dissipation ($T_A=-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$)		P_D	300	mW
Operating Junction Temperature		T_J	-40 ~ +125	$^{\circ}\text{C}$
Storage Temperature		T_{STG}	-65 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Recommended Operating Conditions

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage		V_{CC}	1.65		5.5	V
Input Voltage		V_{IN}	0		5.5	V
Output Voltage	Active Mode	V_{OUT}	0		V_{CC}	V
	Power-Down Mode		0		5.5	V
Input Transition Rise or Fall Rate	$V_{CC}=1.65\text{V to }2.7\text{V}$	t_R / t_F	0		20	ns/V
	$V_{CC}=2.7\text{V to }5.5\text{V}$		0		10	ns/V

Electrical Characteristics (T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level Input Voltage	V _{IH}	V _{CC} =1.65V ~ 1.95V	0.65×V _{CC}			V
		V _{CC} =2.3V ~ 2.7V	1.7			V
		V _{CC} =2.7V ~ 3.6V	2			V
		V _{CC} =4.5V ~ 5.5V	0.7×V _{CC}			V
Low-level Input Voltage	V _{IL}	V _{CC} =1.65V ~ 1.95V			0.35×V _{CC}	V
		V _{CC} =2.3V ~ 2.7V			0.7	V
		V _{CC} =2.7V ~ 3.6V			0.8	V
		V _{CC} =4.5V ~ 5.5V			0.3×V _{CC}	V
High-Level Output Voltage	V _{OH}	V _{CC} =1.65 ~ 5.5V, I _{OH} =-100μA	V _{CC} -0.1			V
		V _{CC} =1.65V, I _{OH} =-4mA	1.2			V
		V _{CC} =2.3V, I _{OH} =-8mA	1.9			V
		V _{CC} =2.7V, I _{OH} =-12mA	2.2			V
		V _{CC} =3.0V, I _{OH} =-24mA	2.3			V
		V _{CC} =4.5V, I _{OH} =-32mA	3.8			V
Low-Level Output Voltage	V _{OL}	V _{CC} =1.65 ~ 5.5V, I _{OL} =100μA			0.1	V
		V _{CC} =1.65V, I _{OL} =4mA			0.45	V
		V _{CC} =2.3V, I _{OL} =8mA			0.3	V
		V _{CC} =2.7V, I _{OL} =12mA			0.4	V
		V _{CC} =3.0V, I _{OL} =24mA			0.55	V
		V _{CC} =4.5V, I _{OL} =32mA			0.55	V
Input Leakage Current	I _{I(LEAK)}	V _{CC} =5.5V, V _{IN} =5.5V or GND		±0.1	±5	μA
Power OFF Leakage Current	I _{OFF}	V _{CC} =0V, V _{IN} or V _{OUT} =5.5V		±0.1	±10	μA
Quiescent Supply Current	I _Q	V _{CC} =5.5V, V _{IN} =V _{CC} or GND, I _{OUT} =0		0.1	10	μA
Additional Quiescent Supply Current Per Input Pin	ΔI _{CC}	V _{CC} =2.3 ~ 5.5V, One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND		5	500	μA

Switching Characteristics (T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Propagation delay from input (A) to output(Y)	t _{PLH} t _{PHL}	C _L =30pF	V _{CC} =1.8±0.15V, R _L =1KΩ	1.0	3.5	8.0	ns
			V _{CC} =2.5±0.2V, R _L =500Ω	1.0	2.2	4.4	ns
		C _L =50pF	V _{CC} =2.7V, R _L =500Ω	1.0	2.7	5.2	ns
			V _{CC} =3.3±0.3V, R _L =500Ω	0.5	2.7	4.1	ns
			V _{CC} =5±0.5V, R _L =500Ω	1.0	1.9	3.2	ns



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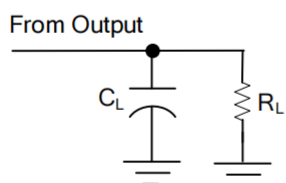
—台丹电子—

74LVC2G04

Dual Inverter

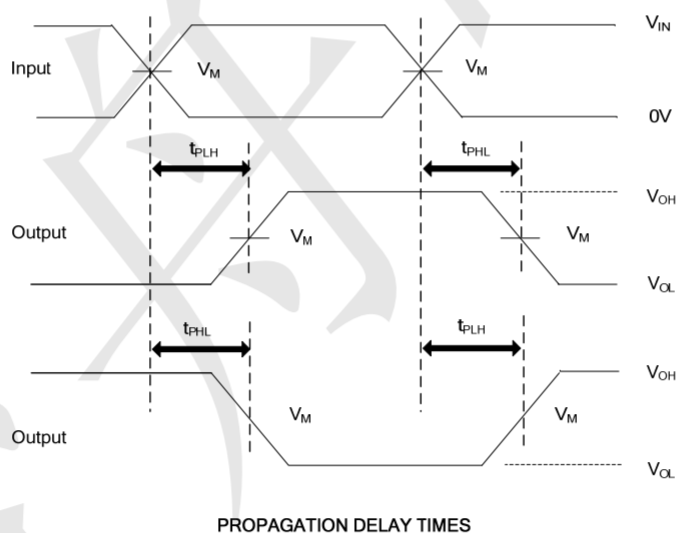
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TEST CIRCUIT AND WAVEFORMS



TEST CIRCUIT

V_{CC}	Inputs		V_M	C_L	R_L
	V_{IN}	t_R, t_F			
$1.8V \pm 0.15V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	30pF	1K Ω
$2.5V \pm 0.2V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	30pF	500 Ω
2.7V	2.7V	$\leq 2.5ns$	1.5V	50pF	500 Ω
$3.3V \pm 0.3V$	2.7V	$\leq 2.5ns$	1.5V	50pF	500 Ω
$5V \pm 0.5V$	V_{CC}	$\leq 2.5ns$	$V_{CC}/2$	50pF	500 Ω



Notes: 1. C_L includes probe and jig capacitance.

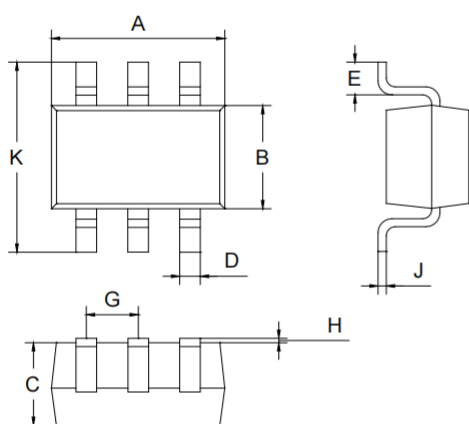
2. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10MHz$, $Z_0=50\Omega$.

V

V

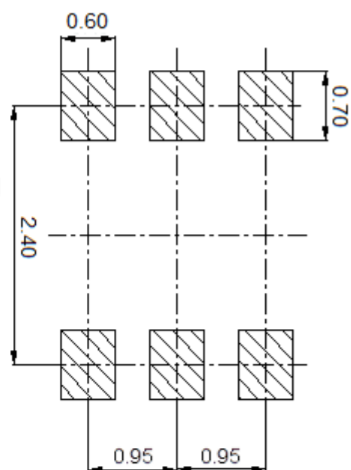
Package Outline Dimensions (Unit: mm)

SOT23-6



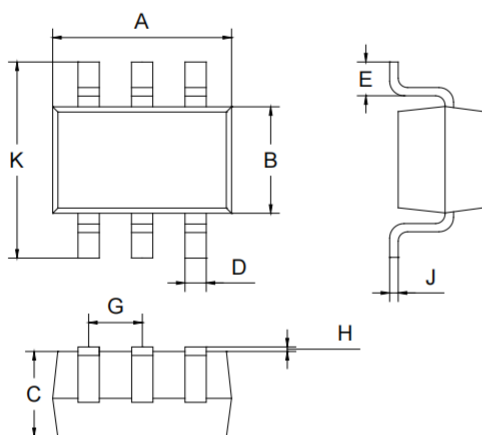
Dimension	Min.	Max.
A	2.80	3.00
B	1.50	1.70
C	1.00	1.20
D	0.35	0.45
E	0.35	0.55
G	0.90	1.00
H	0.02	0.10
J	0.10	0.20
K	2.60	3.00

Mounting Pad Layout (Unit: mm)



Package Outline Dimensions (Unit: mm)

SOT363



Dimension	Min.	Max.
A	2.00	2.20
B	1.15	1.35
C	0.85	1.05
D	0.15	0.35
E	0.25	0.40
G	0.60	0.70
H	0.02	0.10
J	0.05	0.15
K	2.20	2.40

Mounting Pad Layout (Unit: mm)

