MSH100N020D

N-Channel 100-V (D-S) MOSFET

Description

The device is the highest performance trench N-ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

The device meets the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

Features

- $R_{DS(ON)}$ =19.5mΩ@ V_{GS} =10V
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

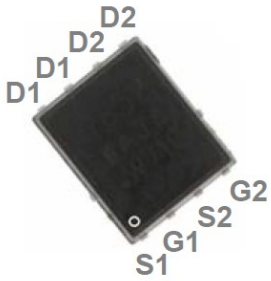
Typical Applications

- Networking
- Load Switch
- LED Applications

Package type：PDFN 5X6 Dual

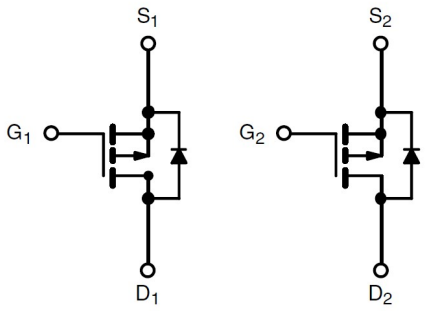
Packing & Order Information

3,000/Reel

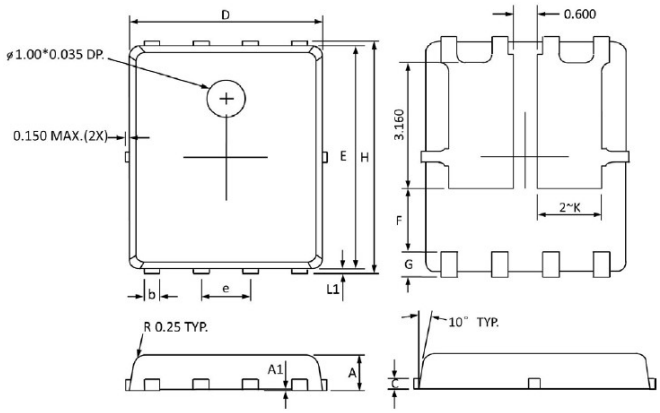


RoHS Compliant

Graphic Symbol

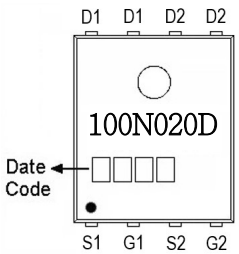


Package Dimension



REF.	Millimeter			REF.	Millimeter		
	Min.	Nom.	Max.		Min.	Nom.	Max.
A	0.90	1.00	1.10	E	5.70	-	5.90
A1	0.00	-	0.05	e	-	1.27	-
b	0.33	-	0.51	H	5.90	-	6.20
c	0.20	-	0.30	G	0.50	-	0.70
D	4.80	-	5.00	L1	0.06	-	0.20
F	1.6 Ref.			K	-	1.60	-

Marking



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MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	±20	V
I_D	Continuous Drain Current[1] (T_C =25°C)	28.5	A
	Continuous Drain Current[1] (T_C =100°C)	20	A
I_{DM}	Pulsed Drain Current[1,2]	90	A
I_{AS}	Single Pulse Avalanche Current, L =0.1mH[3]	30	A
E_{AS}	Single Pulse Avalanche Energy, L =0.1mH[3]	45	mJ
P_D	Power Dissipation[4] (T_C =25°C)	30	W
	Power Dissipation[4] (T_A =25°C)	2	W
T_J/T_{STG}	Operating Junction and Storage Temperature	-55 to +150	°C

Thermal Resistance Ratings

Symbol	Parameter	Maximum	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient[1]	62.5	°C/W
$R_{\theta JC}$	Maximum Junction-to-Case[1]	4.2	°C/W

Electrical Characteristics (T_J=25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{GS\ (th)}$	Gate Threshold Voltage	V_{DS} =V_{GS}, I_D =250μA	1.0	1.7	2.5	V
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} =0V, I_D =250μA	100	-	-	V
I_{GSS}	Gate-Source Leakage Current	V_{DS} =0V, V_{GS} =±20V	-	-	±100	nA
I_{DSS}	Drain-Source Leakage Current	V_{DS} =80V, V_{GS} =0V, T_J =25°C V_{DS} =80V, V_{GS} =0V, T_J =55°C	-	-	1 5	μA
$R_{DS\ (on)}$	Static Drain-Source On-Resistance[2]	V_{GS} =10V, I_D =10A V_{GS} =4.5V, I_D =10A	- -	16.5 22	19.5 29	mΩ
EAS	Single Pulse Avalanche Energy[5]	V_{DD} =25V, L =0.1mH, I_{AS} =22A	24	-	-	mJ
V_{SD}	Diode Forward Voltage[2]	I_S =10A, V_{GS} =0V, T_J =25°C	-	-	1.2	V
I_S	Continuous Source Current[1,6]	V_G =V_D =0V, Force Current	-	-	28.5	A
I_{SM}	Pulsed Source Current[2,6]		-	-	60	

Notes

1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%.
3. The EAS data shows maximum rating. The test condition is V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=30A.
4. The power dissipation is limited by 150℃ junction temperature.
5. The Min. value is 100% EAS tested guarantee.
6. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

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Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Q_g	Total Gate Charge[2]	V_{DS} =50V	--	17.9	--	nC
Q_{gs}	Gate-Source Charge	I_D =10A	--	2.8	--	
Q_{gd}	Gate-Drain (“Miller”) Charge	V_{GS} =10V	--	5.1	--	
$t_{d(on)}$	Turn-On Delay Time[2]	V_{DS} =30V	--	13	--	ns
t_r	Rise Time	I_D =1A	--	6	--	
$t_{d(off)}$	Turn-Off Delay Time	V_{GS} =10V	--	30	--	
t_f	Fall Time	R_G =6Ω	--	29	--	
C_{ISS}	Input Capacitance	V_{DS} =50V	--	849	--	pF
C_{OSS}	Output Capacitance	V_{GS} =0V	--	185	--	
C_{RSS}	Reverse Transfer Capacitance	f =1.0MHz	--	8	--	
Rg	Gate Resistance	V_{GS} =V_{DS} =0V, f =1.0MHz	--	0.8	--	Ω

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- **Typical Electrical Characteristics**

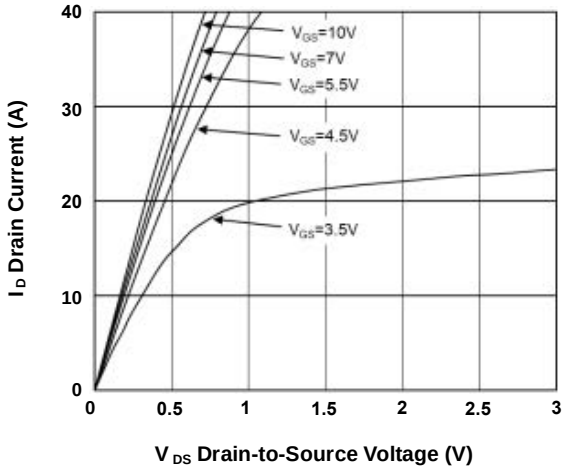

FIG.1-Typical Output Characteristics

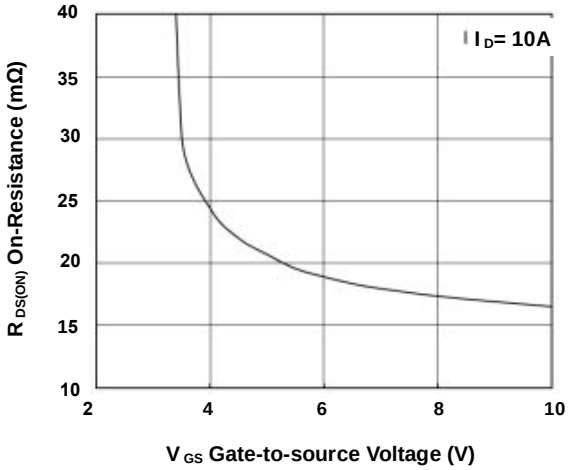

FIG.2-On-Resistance vs. G-S Voltage

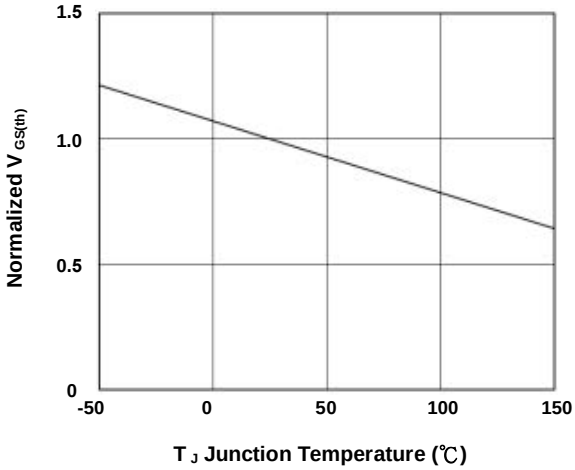

FIG.3-Normalized $V_{GS(th)}$ vs. T_J

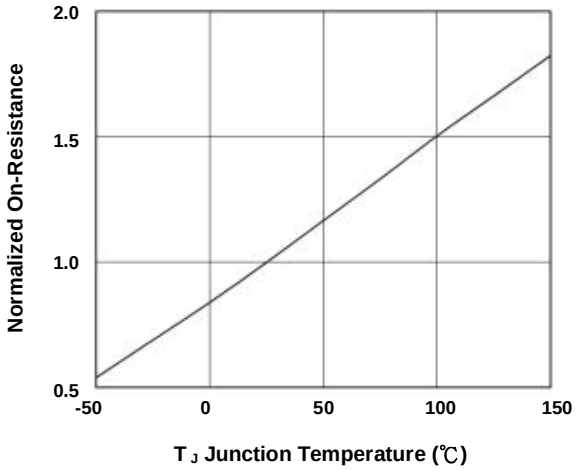

FIG.4-Normalized R_{DSON} vs. T_J

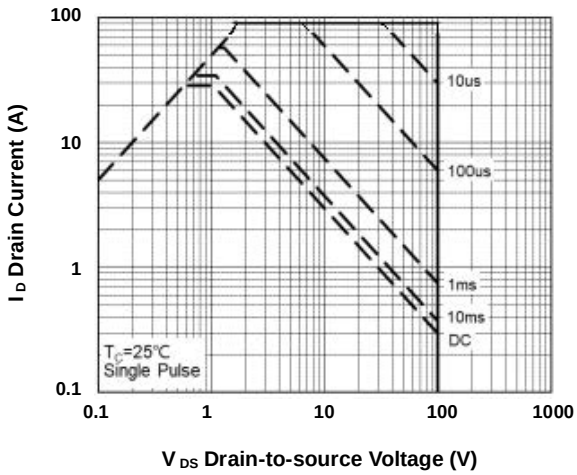

FIG.5-Safe Operating Area

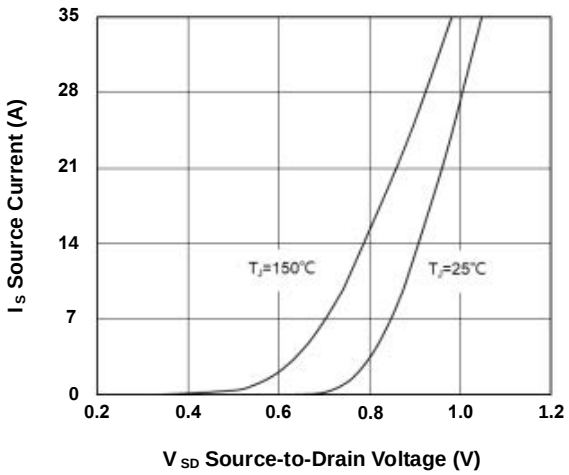

FIG.6-Forward Characteristics of Reverse

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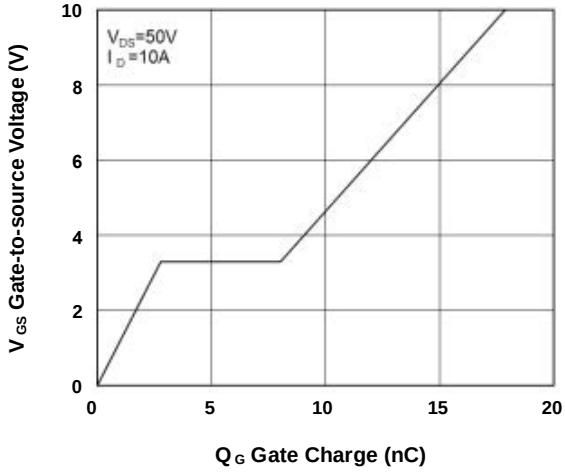

FIG.7-Gate Charge Characteristics

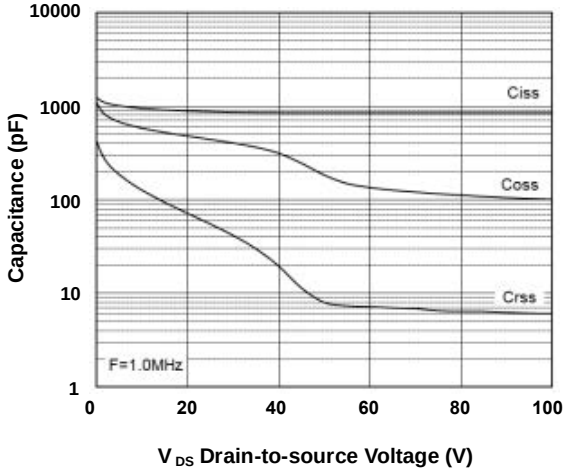

FIG.8-Capacitance Characteristics

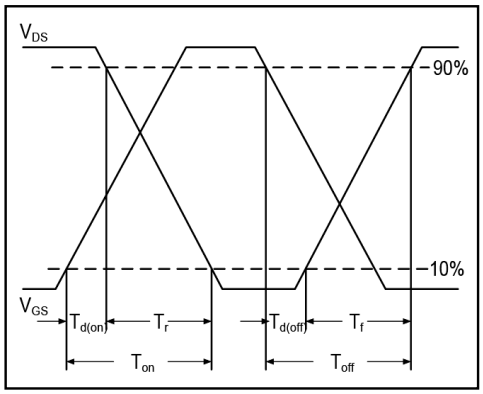

FIG.9-Switching Time Waveform

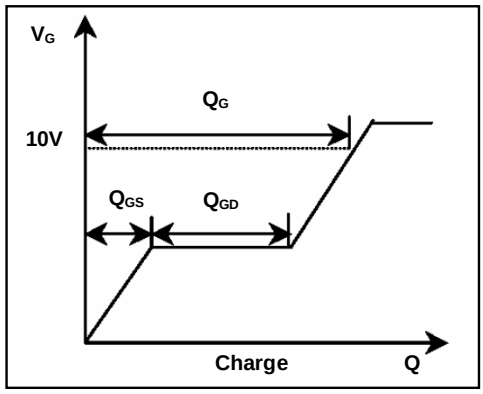

FIG.10-Gate Charge Waveform

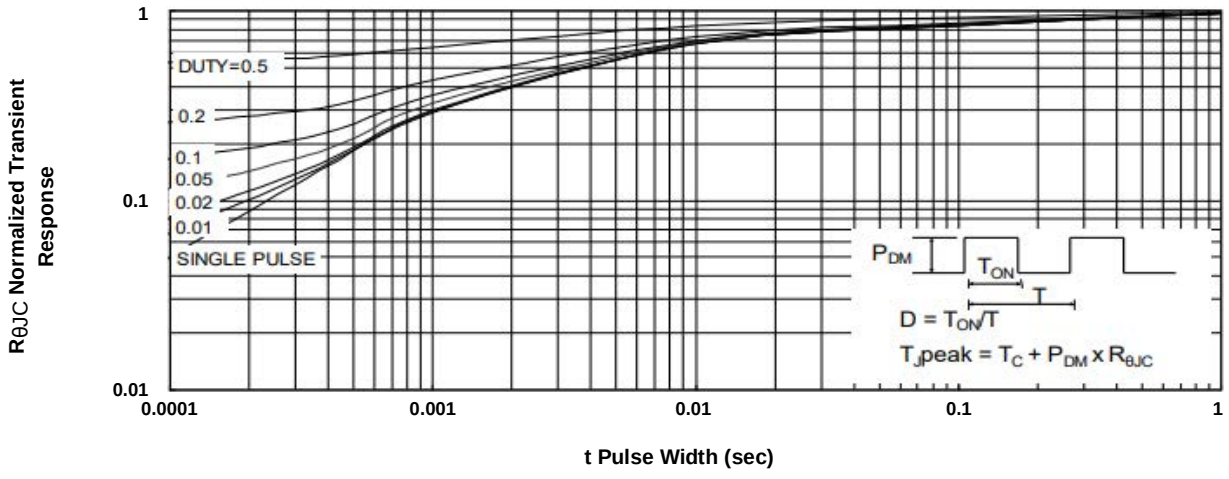

FIG.11-Normalized Maximum Transient Thermal Impedance

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