MSD100P12

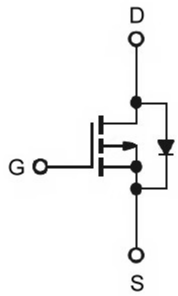
P-Channel 100-V (D-S) MOSFET

Description

The device is the highest performance trench P-ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

The device meets the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

Graphic Symbol



Features

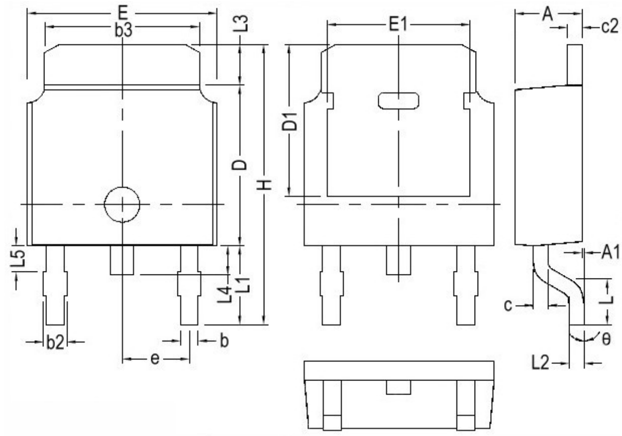
- $R_{DS(ON)}$ =210mΩ@ V_{GS} =-10V
- Low Reverse Transfer Capacitance
- High Switching Speed
- 100% EAS Guaranteed
- Green Device Available

Typical Applications

- Networking
- Load Switch
- LED Applications

Package type：TO-252

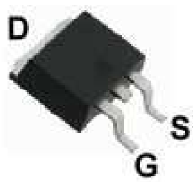
Package Dimension



REF.	Millimeter			REF.	Millimeter		
	Min.	Nom.	Max.		Min.	Nom.	Max.
A	2.20	2.30	2.38	E1	4.40	-	-
A1	0	-	0.127	e	2.286 BSC		
b	0.64	0.76	0.88	H	9.40	10.00	10.40
b2	0.77	0.84	1.14	L	1.40	1.52	1.77
b3	5.21	5.34	5.46	L1	2.743 Ref.		
c	0.45	0.50	0.60	L2	0.508 BSC		
c2	0.45	0.50	0.58	L3	0.89	-	1.27
D	6.00	6.10	6.223	L4	0.64	-	1.01
D1	5.21	-	-	L5	-	-	-
E	6.40	6.60	6.731	θ	0°	-	10°

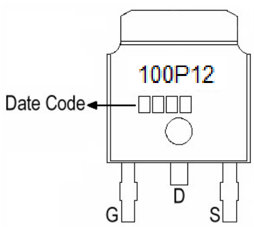
Packing & Order Information

2,500/Reel



RoHS Compliant

Marking



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MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{DS}	Drain-Source Voltage	-100	V
V_{GS}	Gate-Source Voltage	±20	V
I_D	Continuous Drain Current[1] (T_C =25°C)	-12	A
	Continuous Drain Current[1] (T_C =100°C)	-7.8	A
I_{DM}	Pulsed Drain Current[1,2]	-24	A
I_{AS}	Single Pulse Avalanche Current, L =0.5mH[3]	-14	A
E_{AS}	Single Pulse Avalanche Energy, L =0.5mH[3]	49	mJ
P_D	Power Dissipation[4] (T_C =25°C)	38	W
	Power Dissipation[4] (T_A =25°C)	2	W
T_J/T_{STG}	Operating Junction and Storage Temperature	-55 to +150	°C

Thermal Resistance Ratings

Symbol	Parameter	Maximum	Units
$R_{θJA}$	Maximum Junction-to-Ambient[1]	62.5	°C/W
$R_{θJC}$	Maximum Junction-to-Case[1]	2.8	°C/W

Electrical Characteristics (T_J=25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{GS\ (th)}$	Gate Threshold Voltage	V_{DS} =V_{GS}, I_D =-250μA	-1.0	-1.9	-2.5	V
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} =0V, I_D =-250μA	-100	-	-	V
I_{GSS}	Gate-Source Leakage Current	V_{DS} =0V, V_{GS} =±20V	-	-	±100	nA
I_{DSS}	Drain-Source Leakage Current	V_{DS} =-100V, V_{GS} =0V, T_J =25°C V_{DS} =-80V, V_{GS} =0V, T_J =125°C	-	-	-1 -10	μA
$R_{DS\ (on)}$	Static Drain-Source On-Resistance[2]	V_{GS} =-10V, I_D =-5A V_{GS} =-4.5V, I_D =-3A	- -	170 190	210 240	mΩ
EAS	Single Pulse Avalanche Energy[5]	V_{DD} =-25V, L =0.5mH, I_{AS} =-10A	25	-	-	mJ
V_{SD}	Diode Forward Voltage[2]	I_S =-5A, V_{GS} =0V, T_J =25°C	-	-	-1.2	V
I_S	Continuous Source Current[1,6]	V_G =V_D =0V, Force Current	-	-	-12	A
I_{SM}	Pulsed Source Current[2,6]		-	-	-24	

Notes

1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%.
3. The EAS data shows maximum rating. The test condition is V_{DD}=-25V, V_{GS}=-10V, L=0.5mH, I_{AS}=-14A.
4. The power dissipation is limited by 150℃ junction temperature.
5. The Min. value is 100% EAS tested guarantee.
6. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

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Dynamic						
Symbol	**Parameter**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Units**
Q_g	Total Gate Charge[2]	V_{DS} =-50V I_D =-5A V_{GS} =-10V	--	19	--	nC
Q_{gs}	Gate-Source Charge		--	3.4	--	
Q_{gd}	Gate-Drain Charge		--	2.9	--	
$t_{d(on)}$	Turn-On Delay Time[2]	V_{DS} =-30V I_D =-1A V_{GS} =-10V R_G =3.3Ω	--	9	--	ns
t_r	Rise Time		--	6	--	
$t_{d(off)}$	Turn-Off Delay Time		--	39	--	
t_f	Fall Time		--	33	--	
C_{ISS}	Input Capacitance	V_{DS} =-30V V_{GS} =0V f =1.0MHz	--	1228	--	pF
C_{OSS}	Output Capacitance		--	41	--	
C_{RSS}	Reverse Transfer Capacitance		--	29	--	
Rg	Gate Resistance	V_{GS} =V_{DS} =0V, f =1.0MHz	--	13	--	Ω

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- **Typical Electrical Characteristics**

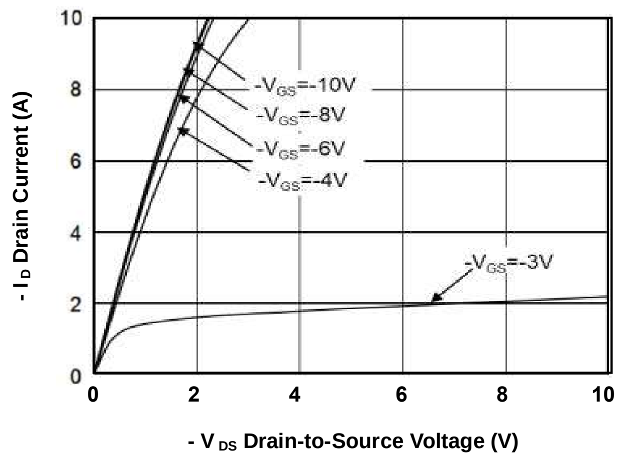

FIG.1-Typical Output Characteristics

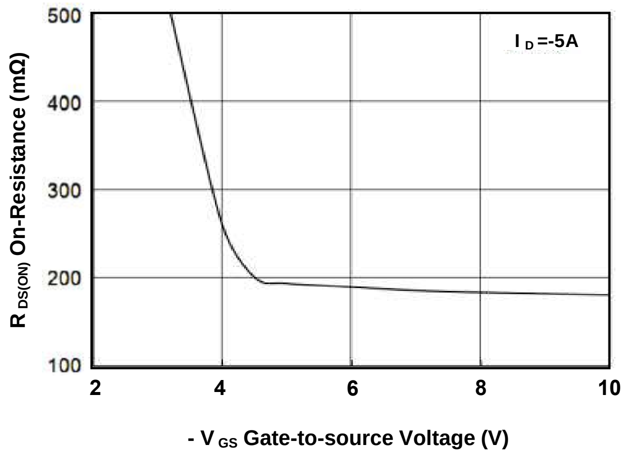

FIG.2-On-Resistance vs. G-S Voltage

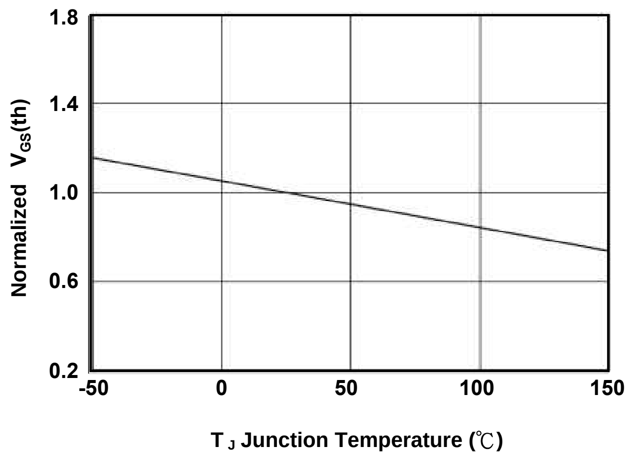

FIG.3-Normalized V_{GS} vs. T_J

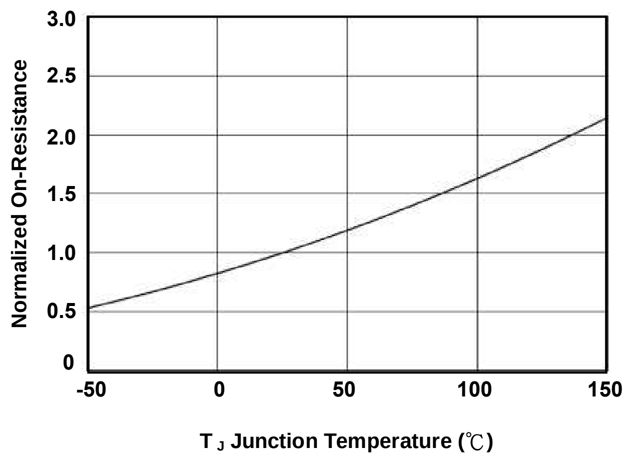

FIG.4-Normalized R_{DSON} vs. T_J

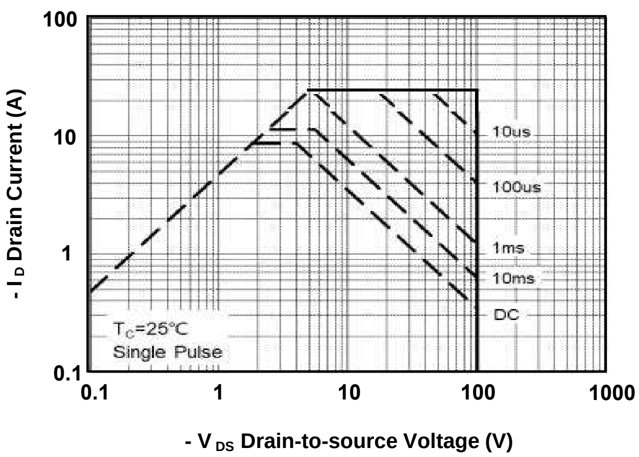

FIG.5-Safe Operating Area

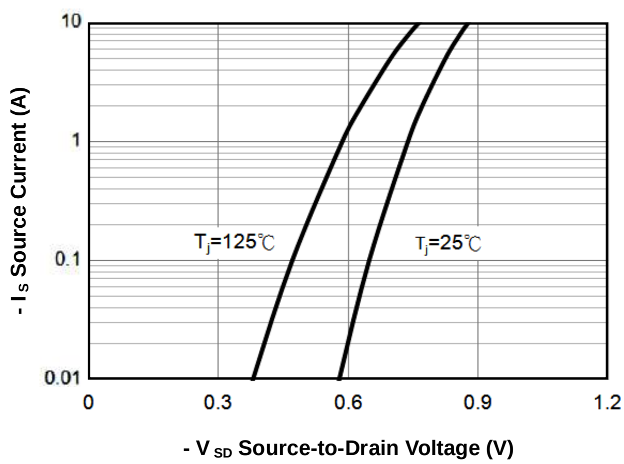

FIG.6-Forward Characteristics of Reverse

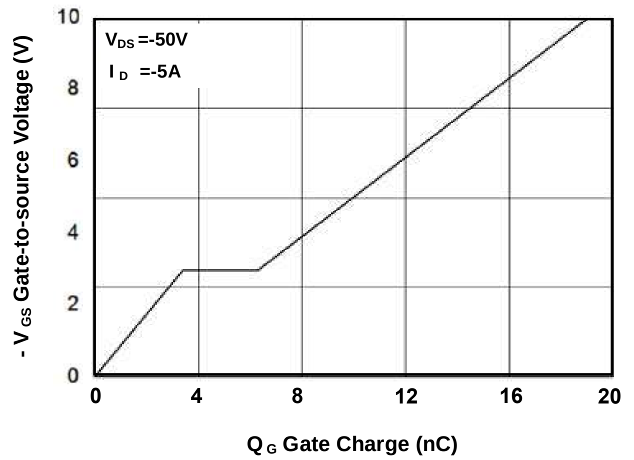

FIG.7-Gate Charge Characteristics

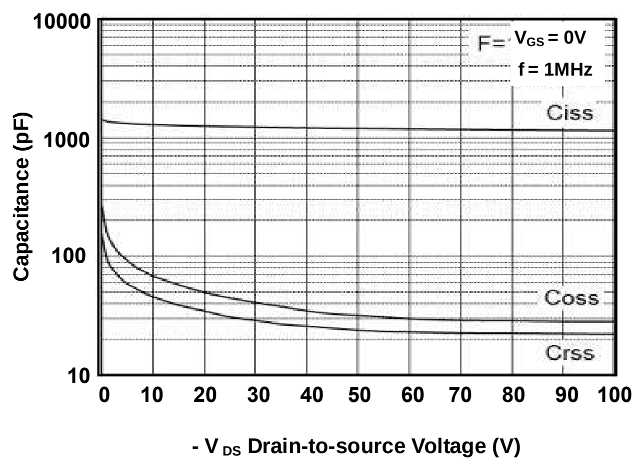

FIG.8-Capacitance Characteristics

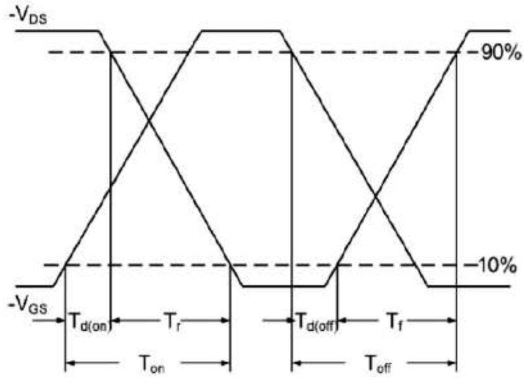

FIG.9-Switching Time Waveform

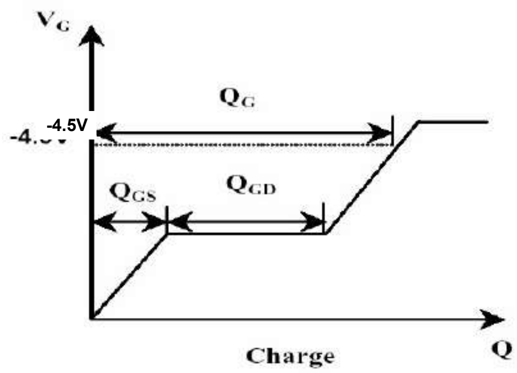

FIG.10-Gate Charge Waveform

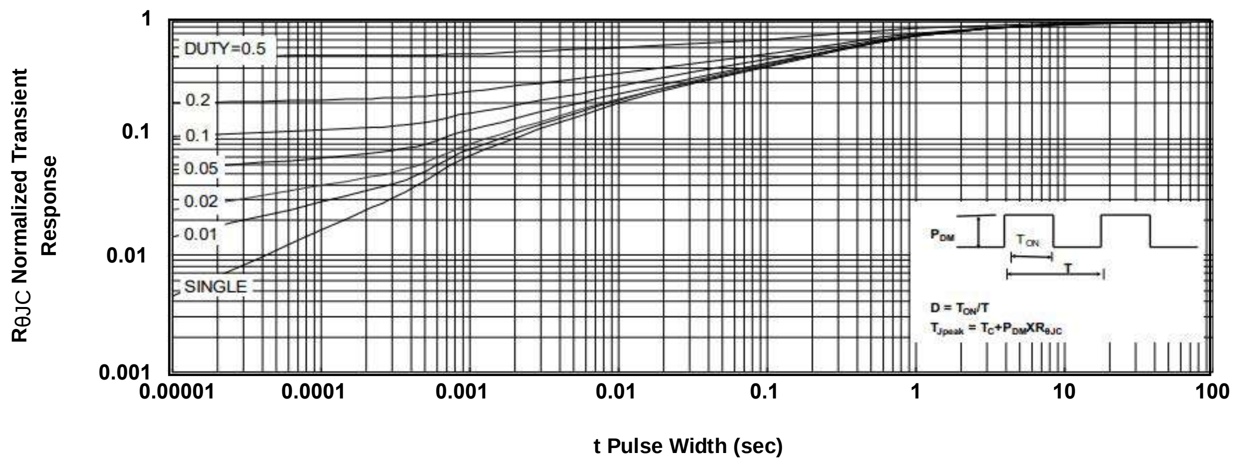

FIG.11-Normalized Maximum Transient Thermal Impedance

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