

# SGM72112A SP12T Switch with MIPI RFFE Interface

### **GENERAL DESCRIPTION**

The SGM72112A is a single-pole/twelve-throw (SP12T) antenna switch, which supports from 0.1GHz to 3GHz. The device features low insertion loss and high isolation, which make it suitable for high linearity receiving applications. It also has the advantage of high linearity performance. The SGM72112A is not subject to cellular interference and is applied to multi-mode and multi-band LTE mobile phones.

The SGM72112A has the ability to SP12T RF switch and MIPI controller on silicon-on-insulator (SOI) process, Internal driver and decoder for switch control signals, which makes it flexible in RF path band and routing selection.

No external DC blocking capacitors required on the RF paths as long as no external DC voltage is applied, which can save PCB area and cost.

The SGM72112A is available in a Green UTQFN-2.5× 2.5-20L package,

#### **APPLICATIONS**

3G/4G Applications

#### **FEATURES**

- Supply Voltage Range: 2.4V to 4.8V
- Advanced Silicon-On-Insulator (SOI) Process
- Frequency Range: 0.1GHz to 3GHz
- Low Insertion Loss: 0.7dB (TYP) at 2.7GHz
- MIPI RFFE Interface Compatible
- No External DC Blocking Capacitors Required
- Available in a Green UTQFN-2.5×2.5-20L Package

### **BLICK DIAGRAM**

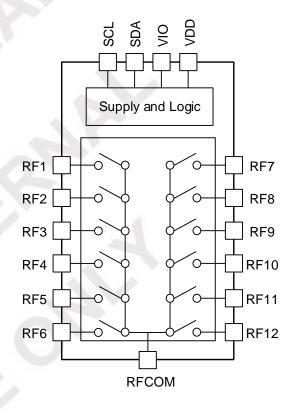


Figure 1 SGM72112A Block Diagram

#### PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM72112A	UTQFN-2.5×2.5-20L	-40°C to +85°C	SGM72112AYURE20G/TR	RD8 XXXX	Tape and Reel, 2000

#### MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code.

YYY — Serial Number

XXXX

Trace Code

Date Code - Year

Green (RoHS & HSF): PS Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your PSMICRO representative directly.

#### **ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, V <sub>DD</sub>	5V
Supply Voltage (MIPI), Vio	2V
SDA, SCL Control Voltage	2V
RF Input Power, PIN	26dBm
Junction Temperature	+150°C
Storage Temperature Range	55°C to +150°C
Lead Temperature (Soldering, 10s)	+260°C
ESD Susceptibility HBM	1000V

#### RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range	40°C to +85°C
Operating Frequency Range	0.1GHz to 3GHz
Supply Voltage, V <sub>DD</sub>	2.4V to 4.8V
Supply Voltage (MIPI), Vio	1.65V to 1.95V

#### **OVERSTRESS CAUTION**

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

#### **ESD SENSITIVITY CAUTION**

This integrated circuit can be damaged if ESD protections are not considered carefully. PSMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

#### **DISCLAIMER**

PS Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

# **PIN CONFIGURATION**

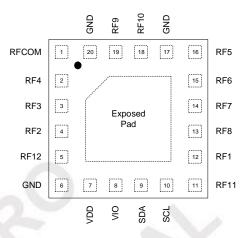


Figure 2. SGM72112A-20L

# **PIN DESCRIPTION**

PIN	NAME	FUNCTION	PIN	NAME	FUNCTION
1	RFCOM	RF Common Port.	10	SCL	RFFE Clock Signal.
2	RF4	RF Port 4.	11	RF11	RF Port 11.
3	RF3	RF Port 3.	12	RF1	RF Port 1.
4	RF2	RF Port 2	13	RF8	RF Port 8.
5	RF12	RF Port 12.	14	RF7	RF Port 7.
6, 17, 20	GND	Ground.	15	RF6	RF Port 6.
7	VDD	DC Power Supply.	16	RF5	RF Port 5.
8	VIO	Supply voltage for MIPI.	18	RF10	RF Port 10.
9	SDA	RFFE Data Signal.	19	RF9	RF Port 9.
Exposed Pad	GND	Ground.		-	

# Register\_0 TRUTH TABLE

Table 1 Register\_0 Truth Table

State	Mode				Regis	ster_0 Bits			
State	Wode	D7	D6	D5	D4	D3	D2	D1	D0
1	Isolation	0	0	0	0	0	0	0	0
2	RF1	0	0	0	0	0	1	0	0
3	RF2	0	0	0	0	0	1	1	1
4	RF3	0	0	0	0	1	0	0	1
5	RF4	0	0	0	0	1	0	1	1
6	RF5	0	0	0	0	1	1	0	0
7	RF6	0	0	0	0	0	0	0	1
8	RF7	0	0	0	0	0	0	1	0
9	RF8	0	0	0	0	0	0	1	1
10	RF9	0	0	0	0	1	0	1	0
11	RF10	0	0	0	0	1	0	0	0
12	RF11	0	0	0	0	0	1	0	1
13	RF12	0	0	0	0	0	1	1	0

# **ELECTRICAL CHARACTERISTICS**

(Typical values,  $V_{DD}$  = 2.8V,  $T_A$  = +25°C,  $P_{IN}$  = 0dBm, 50 $\Omega$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
DC Specifications							
Supply Voltage	$V_{DD}$		2.4	2.8	4.8	V	
Supply Current	I <sub>DD</sub>			32	60	μA	
V <sub>IO</sub> Supply Voltage	V <sub>IO</sub>		1.65	1.8	1.95	V	
V <sub>IO</sub> Supply Current	I <sub>IO</sub>			4.8	10	μA	
Control Voltage	V <sub>CTL_H</sub>	High	0.8 × V <sub>IO</sub>	V <sub>IO</sub>	1.95	V	
Control Voltage	V <sub>CTL_L</sub>	Low	0		0.45	_ v	
Switching Time	t <sub>SW</sub>	50% of control voltage to 90% of RF power		1	2	μs	
Turn-On Time	t <sub>ON</sub>	Time from $V_{DD} = 0V$ to part ON and RF at 90%		5	10	μs	
RF Specifications					1	-1	
		$f_0 = 0.1 GHz$ to 1.0 GHz		0.5	0.65		
Insertion Loss (RFCOM to All RF Ports)	IL	$f_0 = 1.0 GHz$ to 2.0 GHz		0.6	0.75	dB	
(IN COM to All IN TOTO)	111	$f_0 = 2.0 GHz$ to 2.7 GHz		0.7	0.85		
	11/10	f <sub>0</sub> = 0.1GHz to 1.0GHz	21	26			
Isolation (RFCOM to All RF Ports)	ISO	$f_0 = 1.0$ GHz to 2.0GHz	15	20		dB	
(IN COM to All IN 1 orts)		$f_0 = 2.0$ GHz to 2.7GHz	12	17			
7		$f_0 = 0.1 GHz$ to 1.0 GHz	19	22			
Input Return Loss (RFCOM to All RF Ports)	RL	$f_0 = 1.0$ GHz to 2.0GHz	18	21		dB	
	1	$f_0 = 2.0$ GHz to 2.7GHz	10	13			
0.1dB Compression Point (RFCOM to All RF Ports)	P <sub>0.1dB</sub>	$f_0 = 0.1$ GHz to 3GHz		26		dBm	

## MIPI READ AND WRITE TIMING

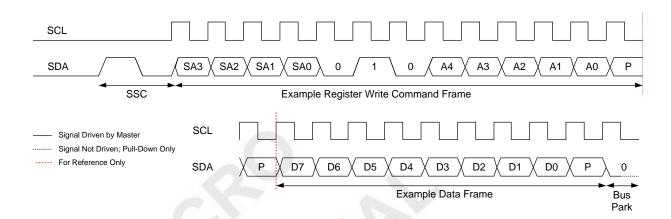


Figure 3. Register Write Command Timing Diagram

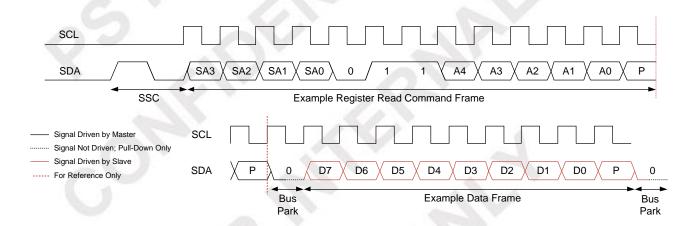


Figure 4. Register Read Command Timing Diagram

## **COMMAND SEQUENCE BIT DEFINITIONS**

_		244.00	C8 C7	07					Parity	DDC	Extended Operation					
Туре	ype SSC	C11-C8		C6-C5	C4	C3-C0	Bits	BPC	DA7(1)- DA0(1)	Parity Bits	ВРС	DA7(n)- DA0(n)	Parity Bits	ВРС		
Reg0 Write	Υ	SA[3:0]	1	Data[6:5]	Data[4]	Data[3:0]	Y	Υ	-	-	-	-	-	-		
Reg Write	Υ	SA[3:0]	0	10	Addr[4]	Addr[3:0]	Υ	-	Data[7:0]	Υ	Υ	-	-	-		
Reg Read	Υ	SA[3:0]	0	11	Addr[4]	Addr[3:0]	Y	Υ	Data[7:0]	Υ	Y	-	-	-		

#### Legends:

SSC = Sequence start command

SA = Slave address

D = Register Address

A = Data bits

C = Command frame bits

BPC = Bus park cycle

# **REGISTER MAPS**

Register\_0 Register Address: 0x0000; R/W

Table 2. Register\_0 Register Details

Bit(s)	Bit Name	Description	Default	R/W
D[7:0]	MODE_CTRL	See Table 1 section.	0000 0000	R/W

# PM\_TRIG

Register Address: 0x001C; R/W and W Table 3. PM\_TRIG Register Details

Bit(s)	Bit Name	Description	Default	Туре
D[7]	PWR_MODE_1	0: Normal 1: Low power	0	R/W
D[6]	PWR_MODE_0	O: Active - Normal     1: Startup - All registers are reset to the default	0	R/W
D[5]	TRIGGER_MASK_2	0: TRIGGER_2 enabled 1: TRIGGER_2 disabled If any one of the three TRIGGER_MASK_x is set to logic '1', the corresponding trigger is disabled, in that case data written to a register associated with the trigger goes	0	R/W
D[4]	TRIGGER_MASK_1	0: TRIGGER_1 enabled 1: TRIGGER_1 disabled Control of the destination register. Otherwise, if the TRIGGER_MASK_x is set to logic '0', incoming data is written to the shadow register, and the	0	R/W
D[3]	TRIGGER_MASK_0	0: TRIGGER_0 enabled destination register is unchanged until its corresponding trigger is asserted.		R/W
D[2]	TRIGGER_2	O: Keep its associated destination registers unchanged.  1: Load its associated destination registers with the data in the parallel shadow register, provided TRIGGER_MASK_2 is set to logic '0'.	0	W
D[1]	TRIGGER_1	O: Keep its associated destination registers unchanged.  1: Load its associated destination registers with the data in the parallel shadow register, provided TRIGGER_MASK_1 is set to logic '0'.	0	W
D[0]	TRIGGER_0	O: Keep its associated destination registers unchanged.  1: Load its associated destination registers with the data in the parallel shadow register, provided TRIGGER_MASK_0 is set to logic '0'.	0	W

# PRODUCT\_ID

Register Address: 0x001D; R

Table 4. PRODUCT\_ID Register Details

Bit(s)	Bit Name	Description	Default	Туре
D[7:0]	PRODUCT_ID	Product ID.	0000 0011	R

# **REGISTER MAPS (continued)**

# MANUFACTURER\_ID Register Address: 0x001E; R

Table 5. MANUFCTURER\_ID Register Details

Bit(s)	Bit Name	Description	Default	Туре
D[7:0]	MANUFACTURER_ID [7:0]	Lower eight bits of MIPI registered Manufacturer ID. Read-only. Note that during USID programming, the write command sequence is executed on the register, but the value does not change.	0100 1010	R

## MAN\_USID

Register Address: 0x001F; R and R/W Table 6. MAN\_USID Register Details

Bit(s)	Bit Name	Description	Default	Туре
D[7:6]	Reserved	Reserved	00	R
D[5:4]	MANUFACTURER_ID [9:8]	Upper two bits of Manufacturer ID. Read-only. Note that during USID programming, the write command sequence is executed on the register, but the value does not change.	00	R
D[3:0]	USID	USID of the device	1011	RW

# **TYPICAL APPLICATION CIRCUIT**

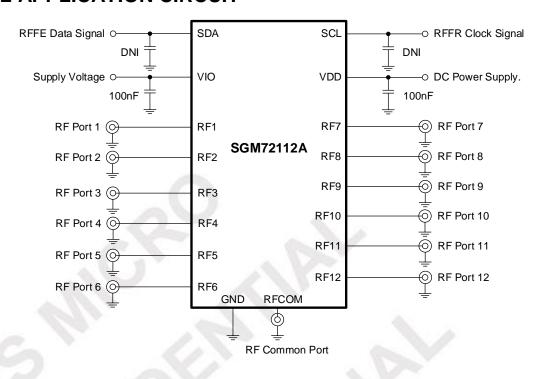


Figure 5. SGM72112A Typical Application Circuit

# **EVALUATION BOARD LAYOUT**

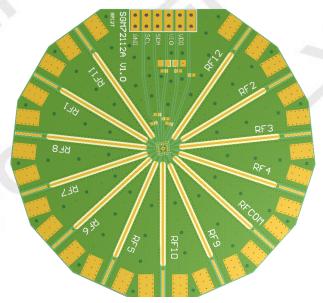
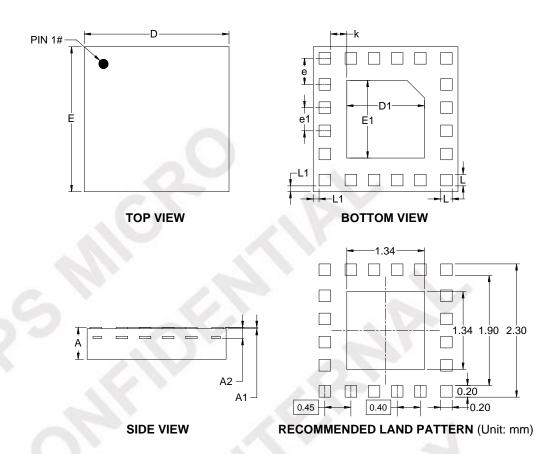


Figure 6. SGM72112A Evaluation Board Layout

# PACKAGE OUTLINE DIMENSIONS UTQFN-2.5×2.5-20L

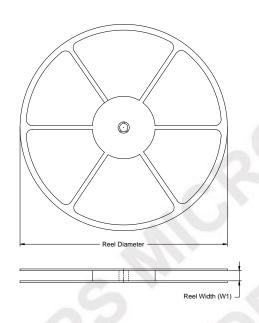


Cumbal	Dimensions In Millimeters					
Symbol	MIN	MOD	MAX			
Α	0.500	0.550	0.600			
A1	0.000	0.020	0.050			
A2	0.152 REF					
D	2.400	2.500	2.600			
E	2.400	2.500	2.600			
D1	1.240	1.340	1.440			
E1	1.240	1.340	1.440			
е	0.450 BSC					
e1	0.400 BSC					
k	0.280 REF					
L	0.150	0.200	0.250			
L1	0.100 REF					

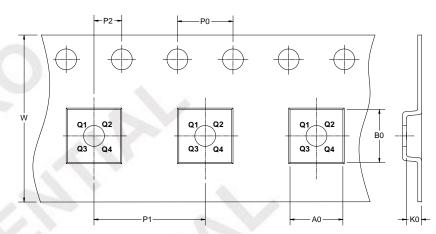
NOTE: This drawing is subject to change without notice.

## TAPE AND REEL INFORMATION

## **REEL DIMENSIONS**



#### **TAPE DIMENSIONS**



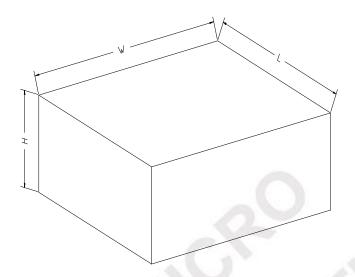
→ DIRECTION OF FEED

NOTE: The picture is only for reference. Please make the object as the standard.

#### **KEY PARAMETER LIST OF TAPE AND REEL**

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant	
UTQFN-2.5×2.5-20L	7"	12.4	2.66	2.69	0.77	4.0	8.0	2.0	12.0	Q2	DD0001

#### **CARTON BOX DIMENSIONS**



NOTE: The picture is only for reference. Please make the object as the standard.

# **KEY PARAMETER LIST OF CARTON BOX**

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton		
7" (Option)	368	227	224	8		
7"	442	410	224	18	DD0002	

#### **SGM72112A**



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