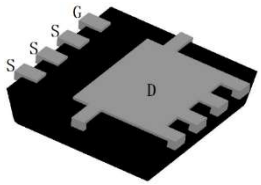
WCL072N06DR

Single N-Channel, 60V, 43A, Power MOSFET

https://www.omnivision-group.com

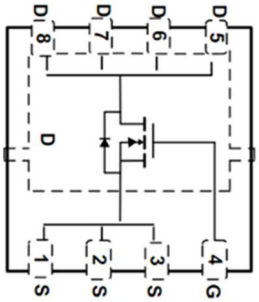
V_{DS} (V)	Max. $R_{DS(on)}$ (mΩ)
60	6.2@ V_{GS}=10V
	9.7@ V_{GS}=4.5V



PDFN3333-8L

Description

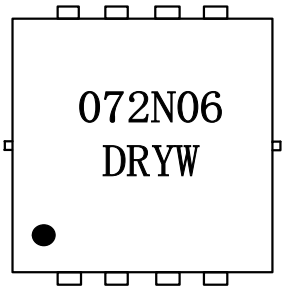
The WCL072N06DR is N-Channel enhancement MOS Field Effect Transistor. Uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in DC-DC conversion, power switch and charging circuit. Standard Product WCL072N06DR is Pb-free..



Pin configuration (Top view)

Features

- Trench Technology
- Supper high density cell design
- Excellent ON resistance
- Low Threshold Voltage
- Package PDFN3333-8L



072N06 = Device Code
DR = Special Code
Y = Year
W = Week(A~z)

Marking

Applications

- DC/DC converters
- Power supply converters circuit
- Load/Power Switching for portable device

Order information

Device	Package	Shipping
WCL072N06DR-8/TR	PDFN3333-8L	5000/Tape&Reel

Absolute Maximum ratin

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current [d]	T_C=25°C	I_D	43	A
	T_C=100°C		36	A
Pulsed Drain Current [c]		I_{DM}	180	A
Continuous Drain Current	T_A=25°C	I_{DSM}	19	A
	T_A=70°C		15	
Avalanche Energy L=0.3mH		E_{AS}	99	mJ
Power Dissipation [b]	T_C=25°C	P_D	40	W
	T_C=100°C		16	
Power Dissipation [a]	T_A=25°C	P_{DSM}	4.4	W
	T_A=70°C		2.8	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature Range		T_{STG}	-55 to 150	°C

Thermal resistance ratings

Single Operation					
Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient Thermal Resistance [a]	t ≤ 10 s	$R_{\theta JA}$	22	29	°C/W
	Steady State		49	61	
Junction-to-Case Thermal Resistance	Steady State	$R_{\theta JC}$	2.5	3.1	

Note:

a FR-4 board (38mm X 38mm X t1.6mm, 70um Copper) partially covered with copper (645mm^2 area). The power dissipation P_{DSM} is based on Junction-to-Ambient thermal resistance $R_{\theta JA}$ t≤10s value and the $T_{J(MAX)}$=150°C. The value is only for reference, any application depends on the user's specific board design.

b The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

c Repetitive rating, ~10us pulse width, duty cycle ~1%, keep initial T_J =25°C, the maximum allowed junction temperature of 150°C.

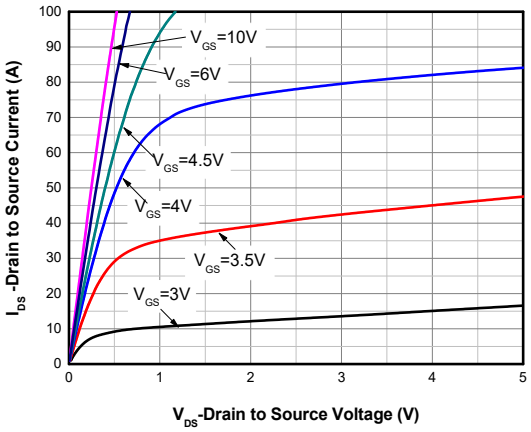
d The maximum current rating by source bonding technology.

e The static characteristics are obtained using ~380us pulses, duty cycle ~1%.

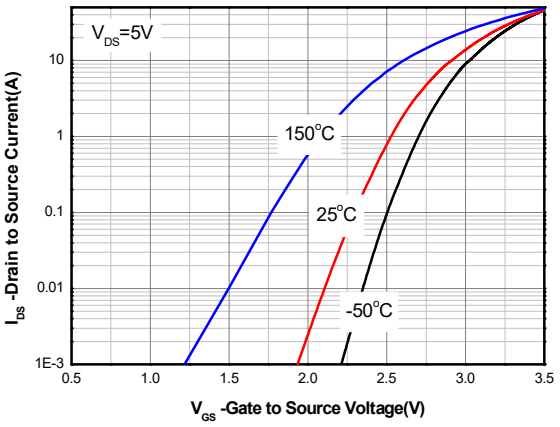
Electronics Characteristics (Ta=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 250uA	60			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60V, V_{GS} = 0V			1	uA
Gate-to-source Leakage Current	I_{GSS}	V_{DS}= 0 V, V_{GS} = ±20V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS}= V_{DS}, I_D = 250uA	1.3	1.8	2.3	V
Drain-to-source On-resistance	$R_{DS(on)}$	V_{GS}= 10V, I_D = 20A		4.8	6.2	mΩ
		V_{GS}= 4.5V, I_D = 20A		7.4	9.7	
CHARGES, CAPACITANCES AND GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{GS}=0V,V_{DS}=30V, f=1MHz		1850		pF
Output Capacitance	C_{OSS}			790		
Reverse Transfer Capacitance	C_{RSS}			34		
Total Gate Charge(10V)	$Q_{G(TOT)}$	V_{GS}=10V,V_{DD}=30V, I_D=20A		34.6		nC
Total Gate Charge(4.5V)	$Q_{G(TOT)}$	V_{GS}=4.5V,V_{DD}=30V, I_D=20A		17.6		
Gate-to-Source Charge	Q_{GS}	V_{GS}=10V,V_{DD}=30V, I_D=20A		6.7		
Gate-to-Drain Charge	Q_{GD}			6.8		
Gate Resistance	R_g	f=1MHz		1.2		Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	td(ON)	V_{GS}= 10V, V_{DD} = 30V, R_G=3Ω,I_D=20A		9.8		ns
Rise Time	tr			32		
Turn-Off Delay Time	td(OFF)			50.5		
Fall Time	tf			30.0		
Body Diode Reverse Recovery Time	trr	I_F=20A, dI/dt=100A/μs		34		ns
Body Diode Reverse Recovery Charge	Qrr			28		nC
BODY DIODE CHARACTERISTICS						
Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 20A		0.8	1.2	V
Maximum Continuous Current	I_S				35	A

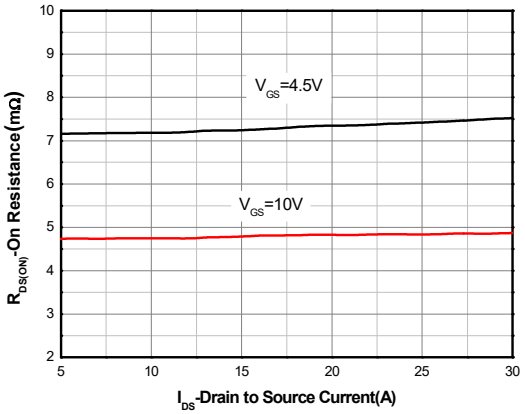
Typical Characteristics (Ta=25°C, unless otherwise noted)



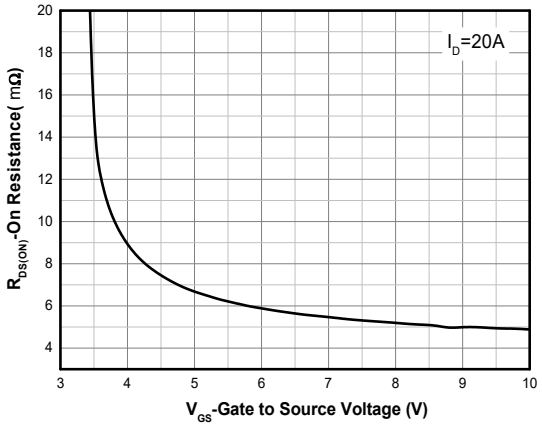
Output Characteristics [e]



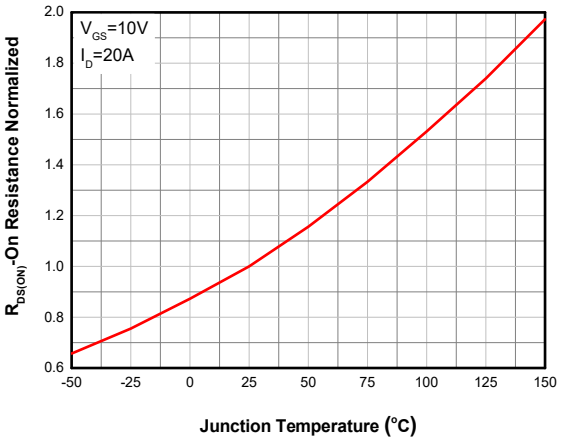
Transfer Characteristics [e]



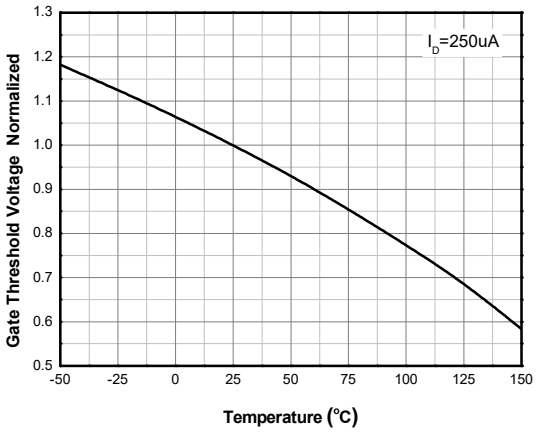
On-Resistance vs. Drain Current [e]



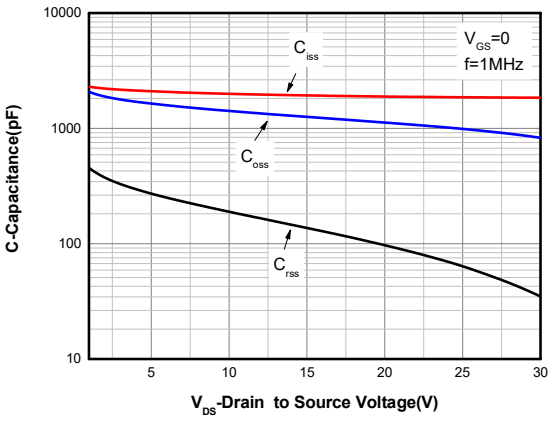
On-Resistance vs. Gate-to-Source Voltage [e]



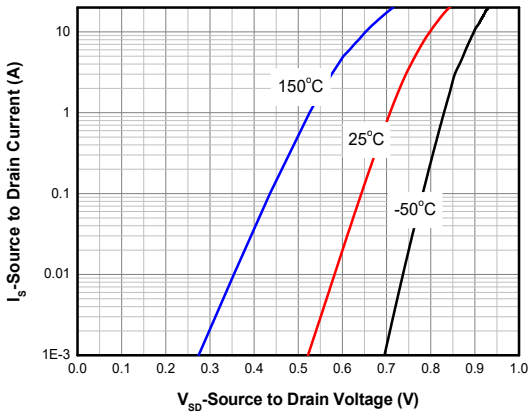
On-Resistance vs. Gate-to-Source Voltage [e]



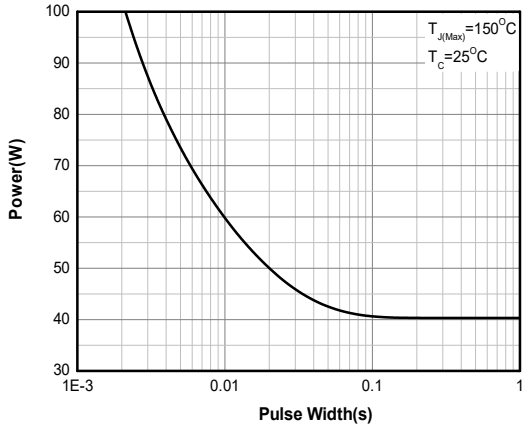
Threshold Voltage vs. Temperature



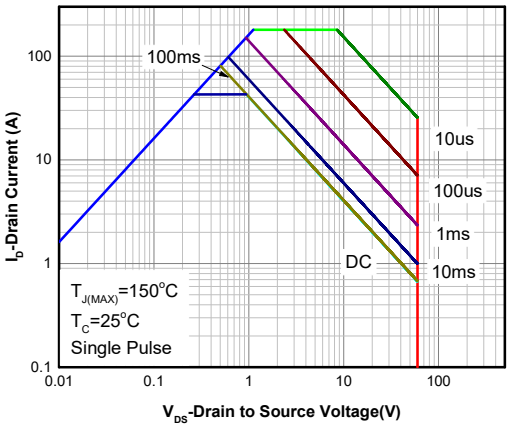
Capacitance



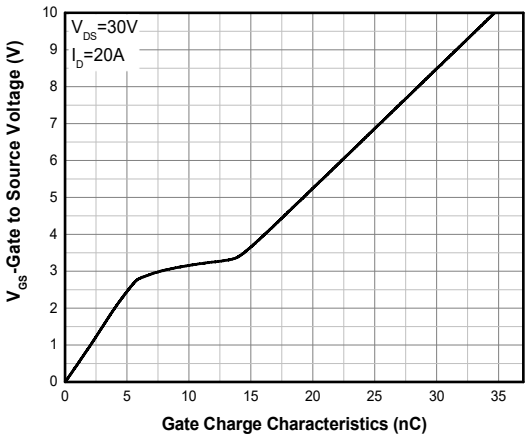
Body Diode Forward Voltage [e]



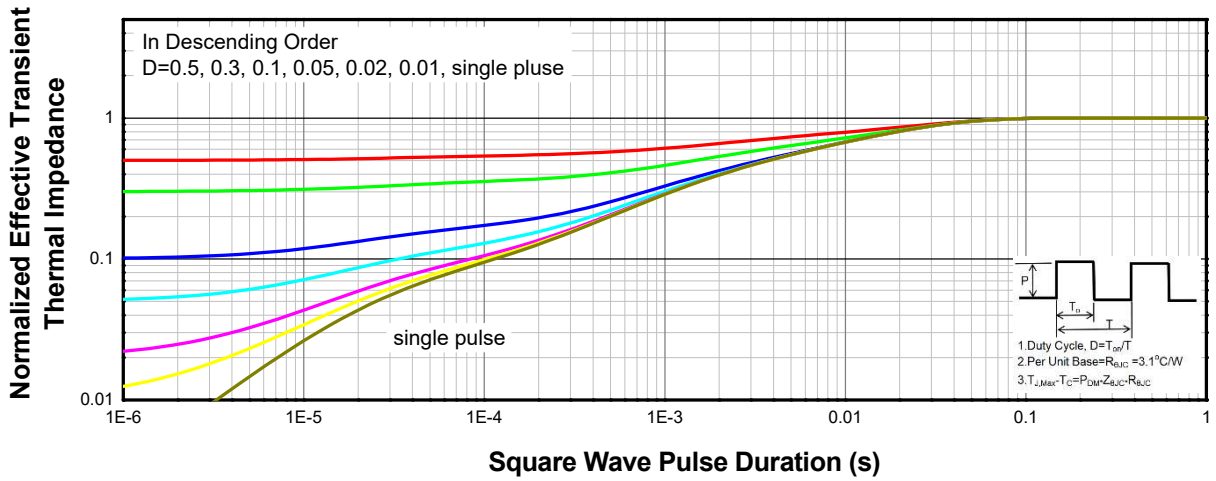
Single Pulse power



Safe Operating Area

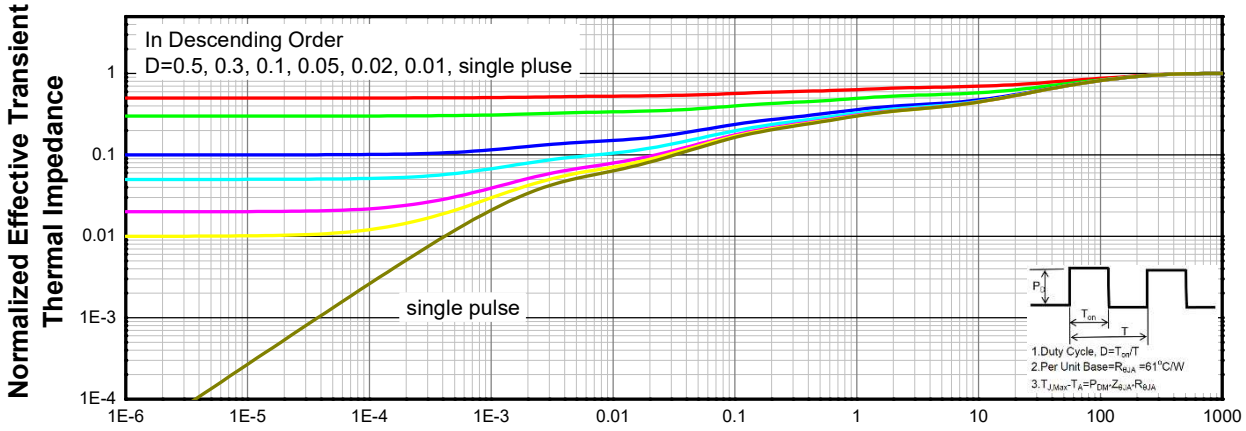


Gate Charge Characteristics



Square Wave Pulse Duration (s)

Transient Thermal Response (Junction-to-Case)

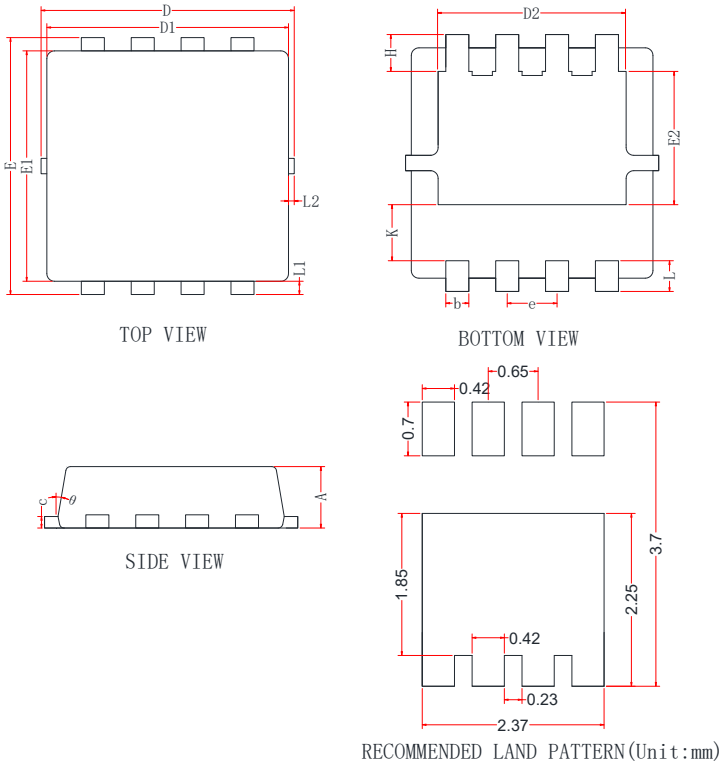


Square Wave Pulse Duration (s)

Transient Thermal Response (Junction-to-Ambient)

PACKAGE OUTLINE DIMENSIONS

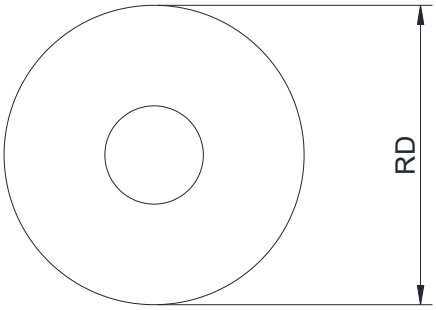
PDFN3333-8L



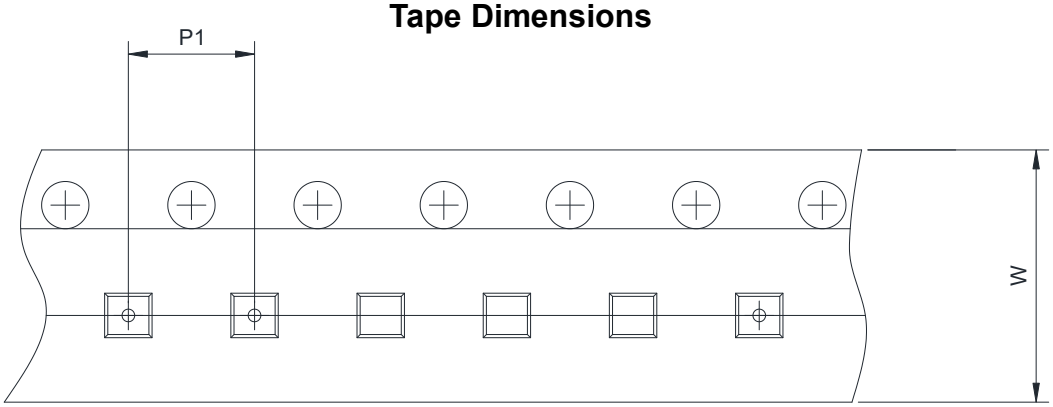
Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.70	0.80	0.90
b	0.25	0.30	0.35
c	0.14	0.15	0.20
D	3.20	3.30	3.40
D1	3.05	3.15	3.25
D2	2.49	2.59	2.69
e	0.55	0.65	0.75
E	3.25	3.35	3.45
E1	2.85	3.00	3.15
E2	1.76	1.86	1.96
H	0.20	0.35	0.50
K	0.54	0.64	0.74
L	0.30	0.40	0.50
L1	0.05	0.15	0.25
L2	-	-	0.15
θ	8 °	10 °	12 °

TAPE AND REEL INFORMATION

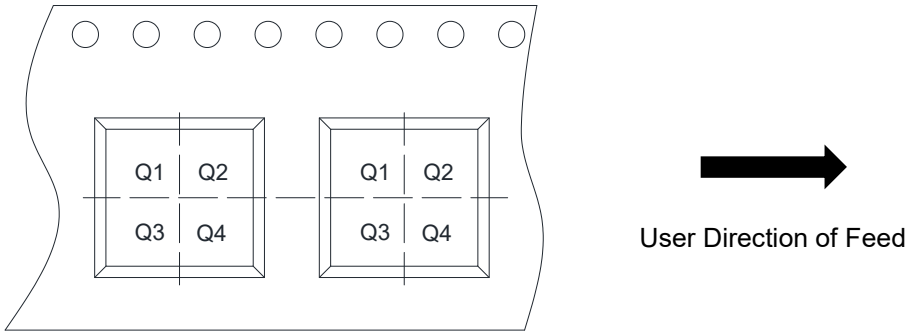
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☐ 7inch	☑ 13inch		
W	Overall width of the carrier tape	☐ 8mm	☑ 12mm	☐ 16mm	
P1	Pitch between successive cavity centers	☐ 2mm	☐ 4mm	☑ 8mm	
Pin1	Pin1 Quadrant	☑ Q1	☐ Q2	☐ Q3	☐ Q4