

INN650DA04

650V GaN Enhancement-mode Power Transistor

Features

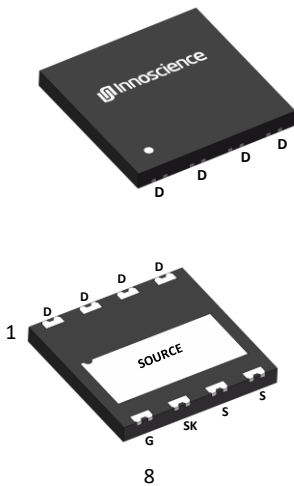
- Enhancement mode transistor-Normally off power switch
- Ultra high switching frequency
- No reverse-recovery charge
- Low gate charge, low output charge
- Qualified for industrial applications according to JEDEC Standards
- ESD safeguard
- RoHS, Pb-free, REACH-compliant

Benefits

- High efficiency power switching
- High power density
- Enables higher switching frequency
- System cost savings

Applications

- AC-DC converters
- DC-DC converters
- Totem pole PFC
- Fast battery charging
- High density power conversion
- High efficiency power conversion



Gate	8
Drain	1,2,3,4
Kelvin Source	7
Source	5,6



Table 1 Key Performance Parameters at T_j = 25 °C

Parameter	Value	Unit
V _{DS,max}	650	V
R _{DS(on),max}	480	mΩ
Q _{G,typ}	0.9	nC
I _{DS,Pulse}	11	A
Q _{oss @ 400V}	8	nC
Q _{rr}	0	nC

Table 2 Ordering Information

Type/Ordering Code	Package	Marking
INN650DA04	DFN 5X6	INN650DA04

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1 Maximum ratings

at $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact Innoscence sales office.

Table 3 Maximum ratings

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Drain source voltage	$V_{DS,max}$	-	-	650	V	$V_{GS} = 0\text{ V}$, $I_D = 10\text{ }\mu\text{A}$
Drain source voltage transient ¹	$V_{DS(transient)}$	-	-	750	V	$V_{GS} = 0\text{ V}$, $V_{DS} = 750\text{ V}$
Continuous current, drain source	I_D	-	-	7	A	$T_c = 25\text{ }^{\circ}\text{C}$
Pulsed current, drain source ²	$I_{D,pulse}$	-	-	11	A	$T_c = 25\text{ }^{\circ}\text{C}$; $V_G = 6\text{ V}$; See Figure 16;
Pulsed current, drain source ²	$I_{D,Pulse}$	-	-	6	A	$T_c = 125\text{ }^{\circ}\text{C}$; $V_G = 6\text{ V}$; See Figure 17;
Gate source voltage, continuous ³	V_{GS}	-1.4	-	+7	V	$T_j = -55\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$
Gate source voltage, pulsed	$V_{GS,pulse}$	-20	-	+10	V	$T_j = -55\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$; $t_{Pulse} = 50\text{ ns}$, $f = 100\text{ kHz}$ open drain
Power dissipation	P_{tot}	-	-	39	W	$T_c = 25\text{ }^{\circ}\text{C}$
Operating temperature	T_j	-55	-	+150	$^{\circ}\text{C}$	
Storage temperature	T_{stg}	-55	-	+150	$^{\circ}\text{C}$	

1 $V_{DS(transient)}$ is intended for surge rating during non-repetitive events, $t_{Pulse} < 1\text{ }\mu\text{s}$

2 Pulse = 300 μs

3 The minimum V_{GS} is clamped by ESD protection circuit, as shown in Figure 10

2 Thermal characteristics

Table 4 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction-case	R_{thJC}	-	-	3.2	°C/W	
Reflow soldering temperature	T_{sold}	-	-	260	°C	MSL3

3 Electrical characteristics

at $T_j = 25\text{ }^{\circ}\text{C}$, unless specified otherwise

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(TH)}$	1.2	1.6	2.2	V	$I_D = 5.2\text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 25\text{ }^{\circ}\text{C}$
		-	1.7	-		$I_D = 5.2\text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 125\text{ }^{\circ}\text{C}$
Drain-source leakage current	I_{DSS}	-	0.4	10	μA	$V_{DS} = 650\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$
		-	5	80		$V_{DS} = 650\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 150\text{ }^{\circ}\text{C}$
Gate-source leakage current	I_{GSS}	-	4	-	μA	$V_{GS} = 6\text{ V}$; $V_{DS} = 0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	365	480	$\text{m}\Omega$	$V_{GS} = 6\text{ V}$; $I_D = 2\text{ A}$; $T_j = 25\text{ }^{\circ}\text{C}$
		-	750	-	$\text{m}\Omega$	$V_{GS} = 6\text{ V}$; $I_D = 2\text{ A}$; $T_j = 150\text{ }^{\circ}\text{C}$
Gate resistance	R_G	-	3	-	Ω	$F = 5\text{ MHz}$; open drain

Table 6 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	34	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$; $f = 100\text{ kHz}$
Output capacitance	C_{oss}	-	9	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$; $f = 100\text{ kHz}$
Reverse transfer capacitance	C_{rss}	-	0.4	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$; $f = 100\text{ kHz}$
Effective output capacitance, energy related ¹	$C_{o(er)}$	-	13	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 0\text{ to }400\text{ V}$
Effective output capacitance, time related ²	$C_{o(tr)}$	-	20	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 0\text{ to }400\text{ V}$
Output Charge	Q_{oss}	-	8	-	nC	$V_{GS} = 0\text{ V}$; $V_{DS} = 0\text{ to }400\text{ V}$
Turn-on delay time	$t_{d(on)}$	-	2	-	nS	See Figure 22
Turn-off delay time	$t_{d(off)}$	-	3	-	nS	See Figure 22
Rise time	t_r	-	7	-	nS	See Figure 22
Fall time	t_f	-	3	-	nS	See Figure 22

¹ $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V

² $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400 V

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate charge	Q_G	-	0.9	-	nC	$V_{GS} = 0 \text{ to } 6 \text{ V}; V_{DS} = 400 \text{ V};$ $I_D = 2 \text{ A}$
Gate-source charge	Q_{GS}	-	0.1	-	nC	
Gate-drain charge	Q_{GD}	-	0.3	-	nC	
Gate Plateau Voltage	V_{Plat}	-	2.7	-	V	$V_{DS} = 400 \text{ V}; I_D = 2 \text{ A}$

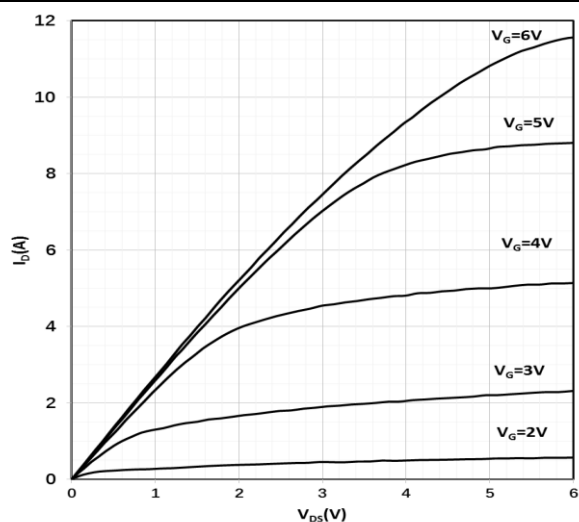
Table 8 Reverse conduction characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	V_{SD}	-	3	-	V	$V_{GS} = 0 \text{ V}; I_{SD} = 2 \text{ A}$
Pulsed current, reverse	$I_{S,pulse}$	-	-	11	A	$V_G = 6 \text{ V}$
Reverse recovery charge	Q_{rr}	-	0	-	nC	$I_{SD} = 2 \text{ A}; V_{DS} = 400 \text{ V}$
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

4 Electrical characteristics diagrams

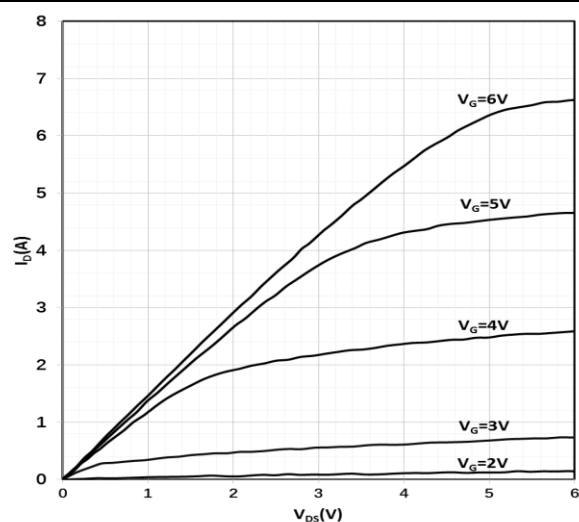
at $T_j = 25\text{ }^{\circ}\text{C}$, unless specified otherwise

Figure 1 Typ. output characteristics



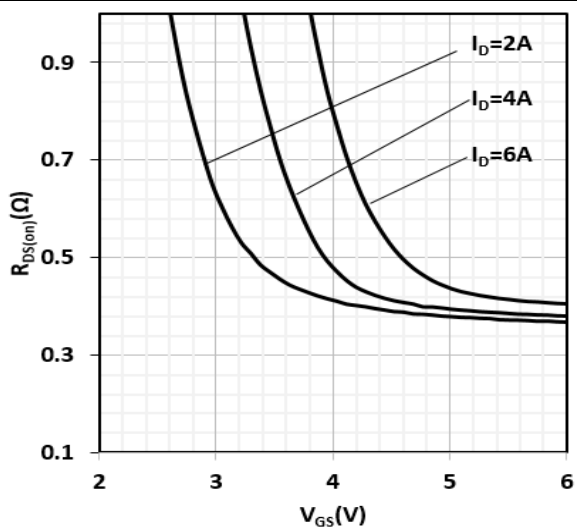
$$I_D = f(V_{DS}, V_{GS}); T_j = 25\text{ }^{\circ}\text{C}$$

Figure 2 Typ. output characteristics



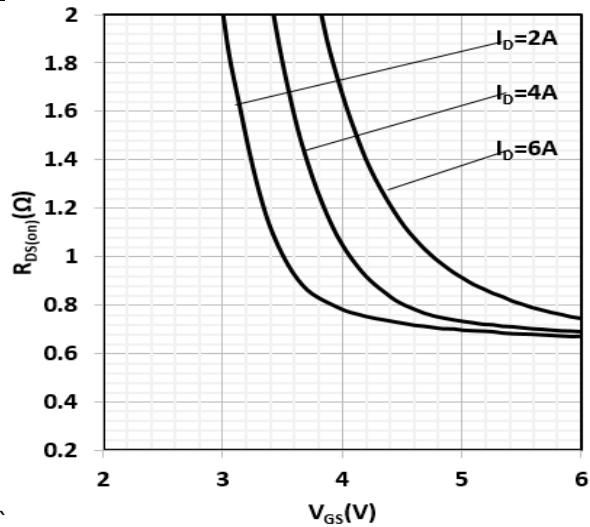
$$I_D = f(V_{DS}, V_{GS}); T_j = 125\text{ }^{\circ}\text{C}$$

Figure 3 Typ. Drain-source on-state resistance



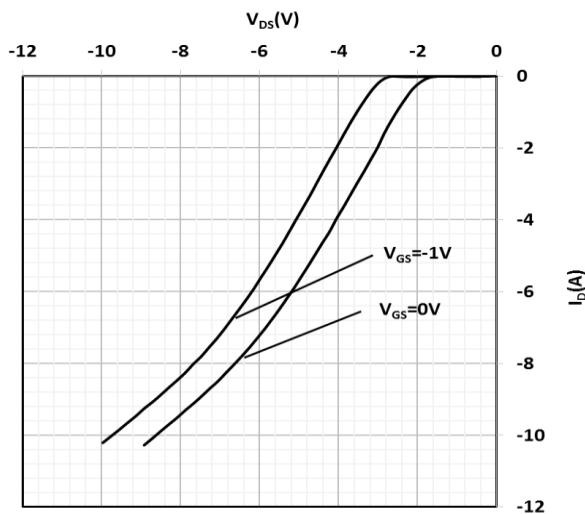
$$R_{DS(on)} = f(I_D, V_{GS}); T_j = 25\text{ }^{\circ}\text{C}$$

Figure 4 Typ. Drain-source on-state resistance



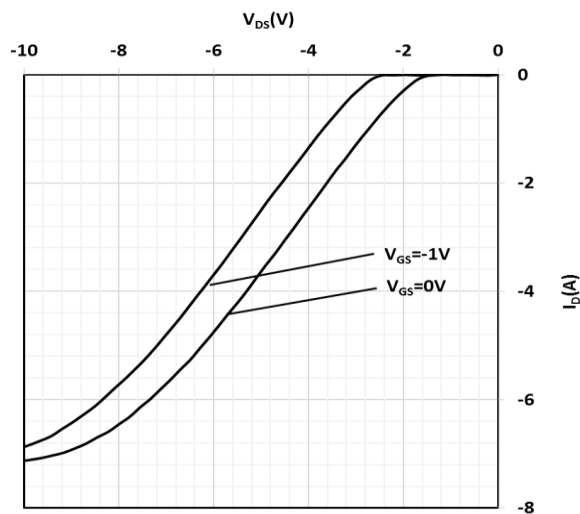
$$R_{DS(on)} = f(I_D, V_{GS}); T_j = 125\text{ }^{\circ}\text{C}$$

Figure 5 Typ. channel reverse characteristics



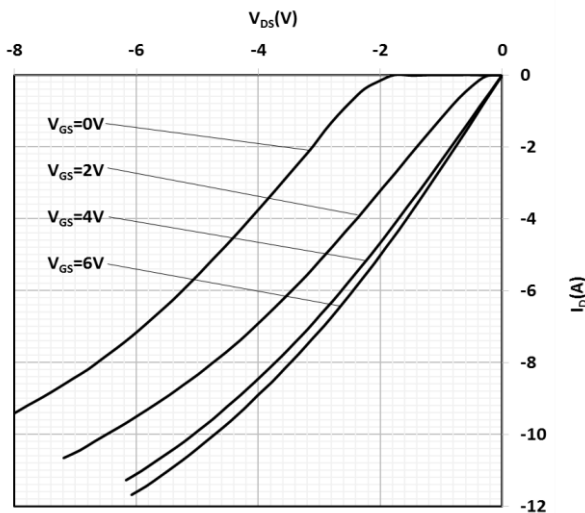
$I_D = f(V_{DS}, V_{GS}); T_j = 25\text{ }^{\circ}\text{C}$

Figure 6 Typ. channel reverse characteristics



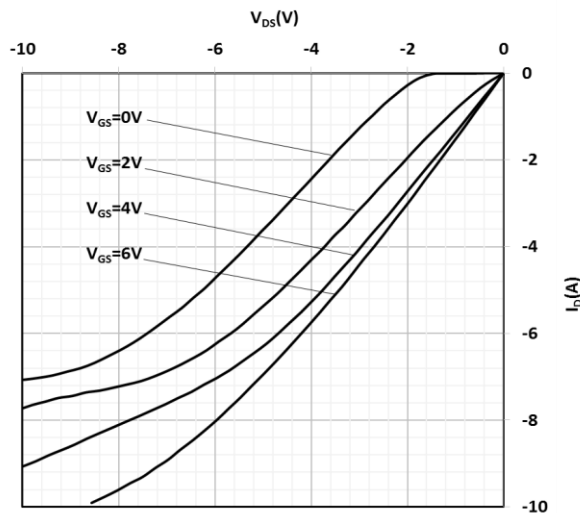
$I_D = f(V_{DS}, V_{GS}); T_j = 125\text{ }^{\circ}\text{C}$

Figure 7 Typ. channel reverse characteristics



$I_D = f(V_{DS}, V_{GS}); T_j = 25\text{ }^{\circ}\text{C}$

Figure 8 Typ. channel reverse characteristics



$I_D = f(V_{DS}, V_{GS}); T_j = 125\text{ }^{\circ}\text{C}$

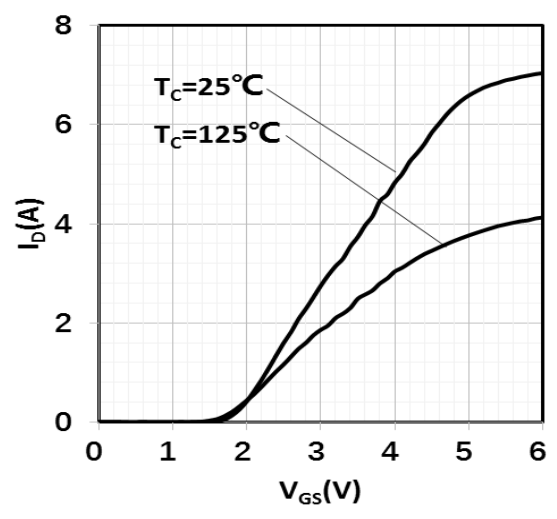
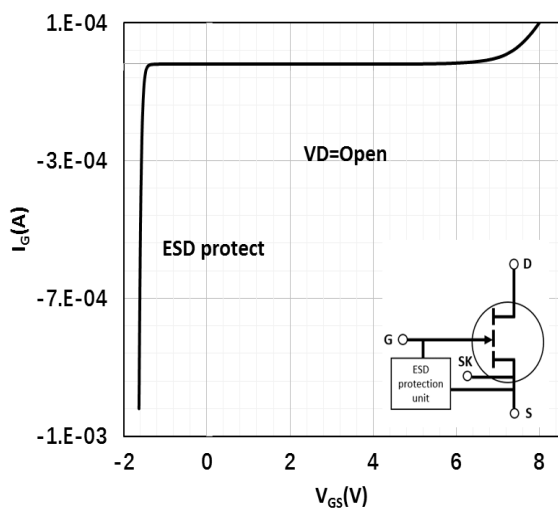
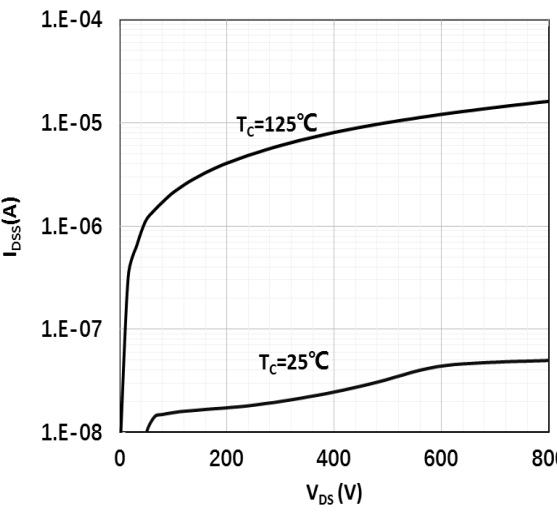
Figure 9 Typ. transfer characteristics  $I_D = f(V_{GS}); V_{DS} = 3\text{ V}$	Figure 10 Typ. Gate-to-Source leakage  $I_G = f(V_{GS}); I_g \text{ reverse turn on by ESD unit}$
Figure 11 Drain-source leakage characteristics  $I_{DSS} = f(V_{DS}); V_{GS} = 0\text{ V}$	

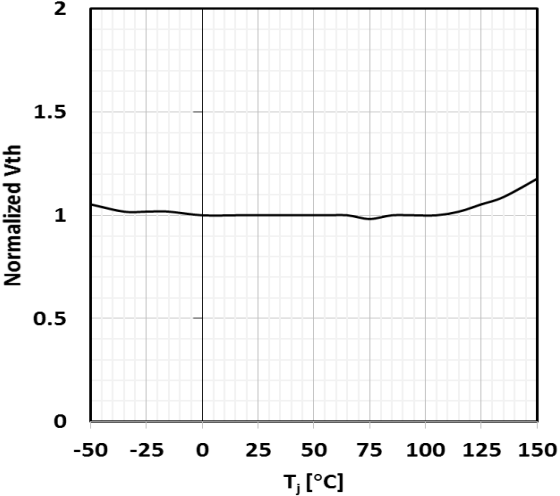
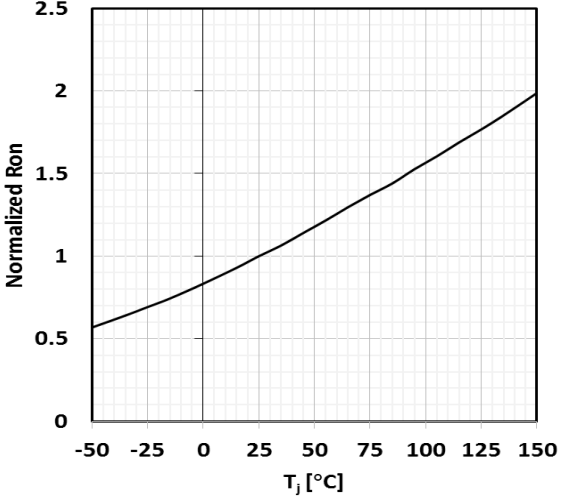
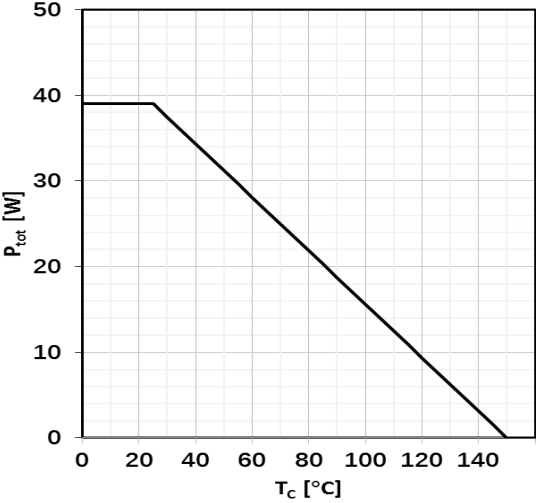
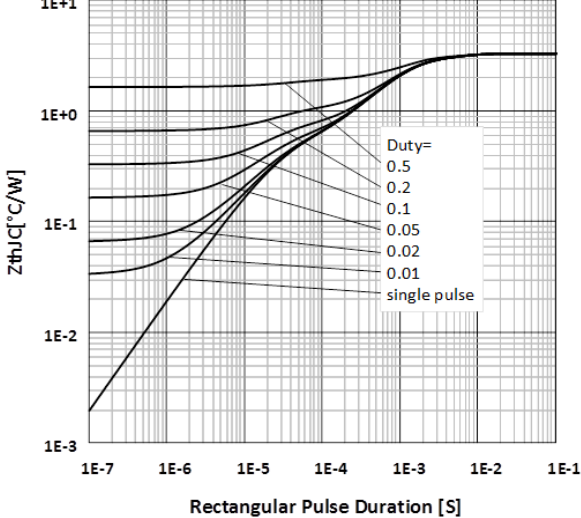
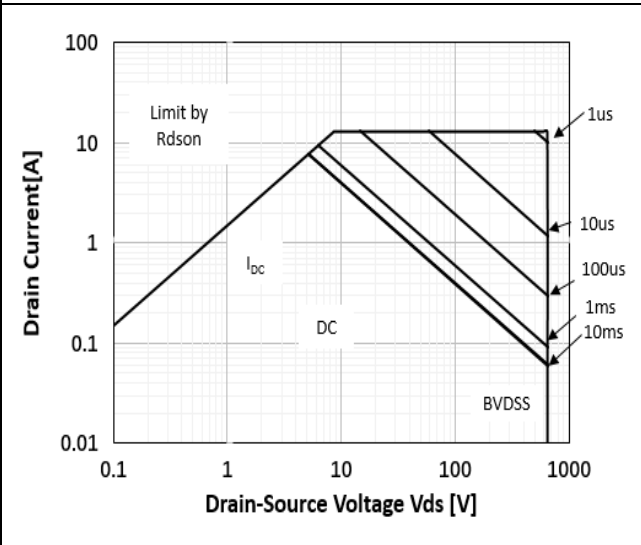
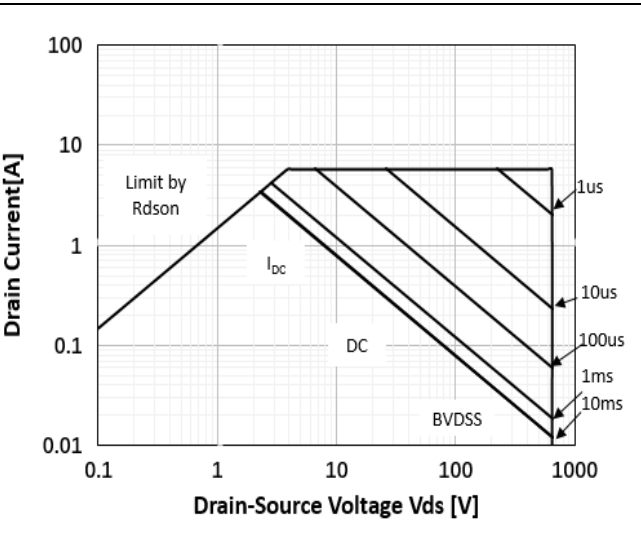
Figure 12 Gate threshold voltage  $V_{TH} = f(T_j); V_{GS} = V_{DS}; I_D = 5.2 \text{ mA}$	Figure 13 Drain-source on-state resistance  $R_{DS(on)} = f(T_j); I_D = 2 \text{ A}; V_G=6\text{V}$
Figure 14 Power dissipation  $P_{tot} = f(T_C)$	Figure 15 Max.transient thermal impedance  $Z_{thJC} = f(t_P, D)$

Figure 16 Safe operating area



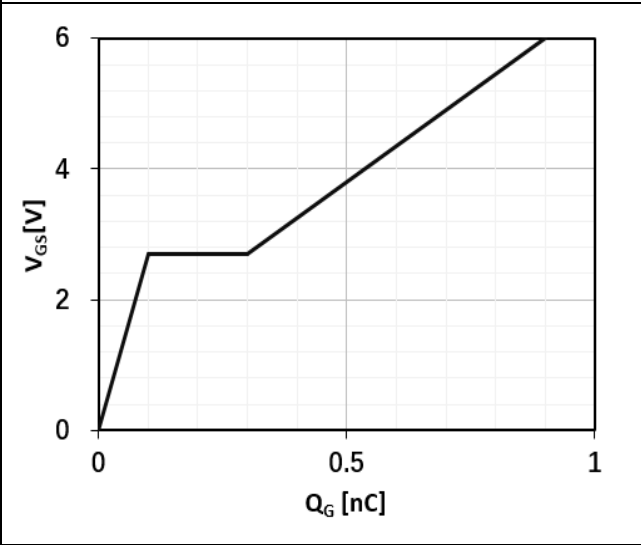
$$I_D = f(V_{DS}); T_C = 25\text{ }^{\circ}\text{C}$$

Figure 17 Safe operating area



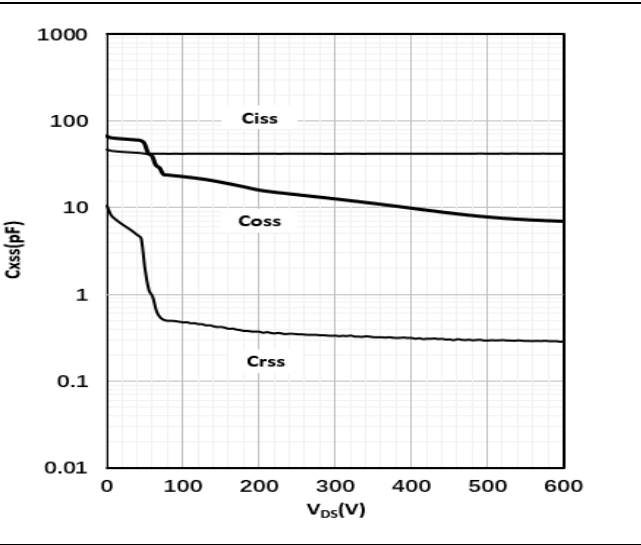
$$I_D = f(V_{DS}); T_C = 125\text{ }^{\circ}\text{C}$$

Figure 18 Typ. gate charge

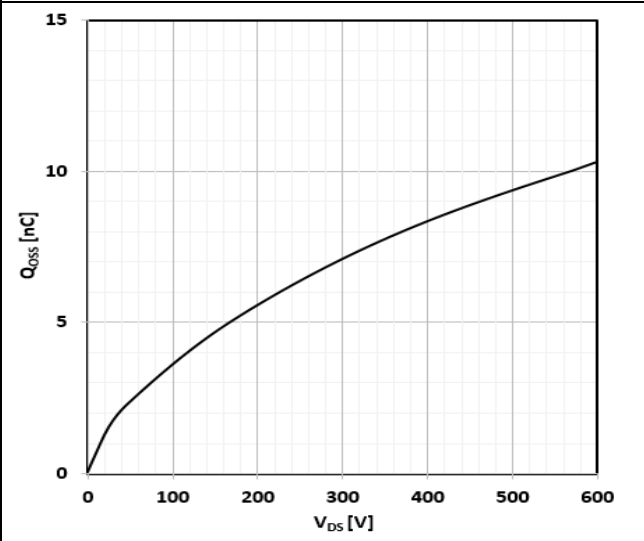
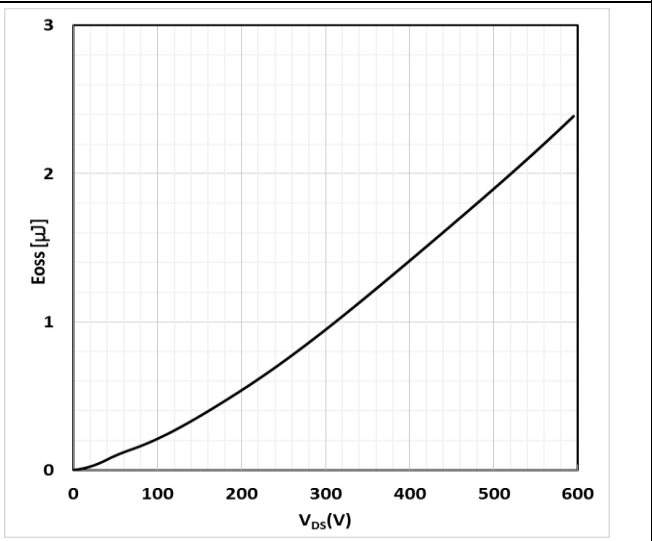
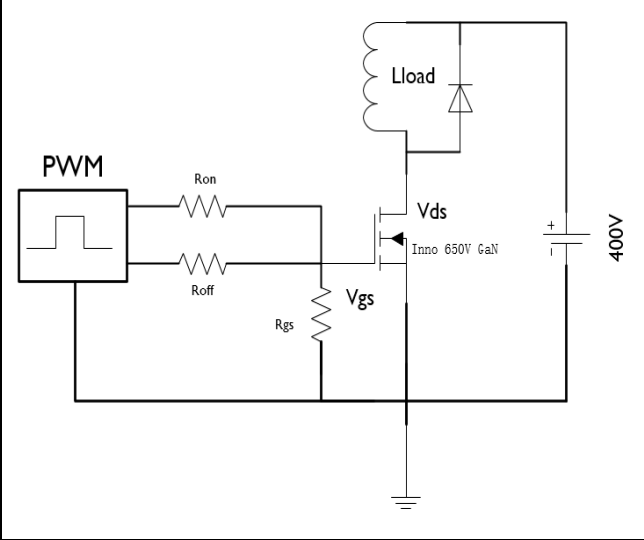
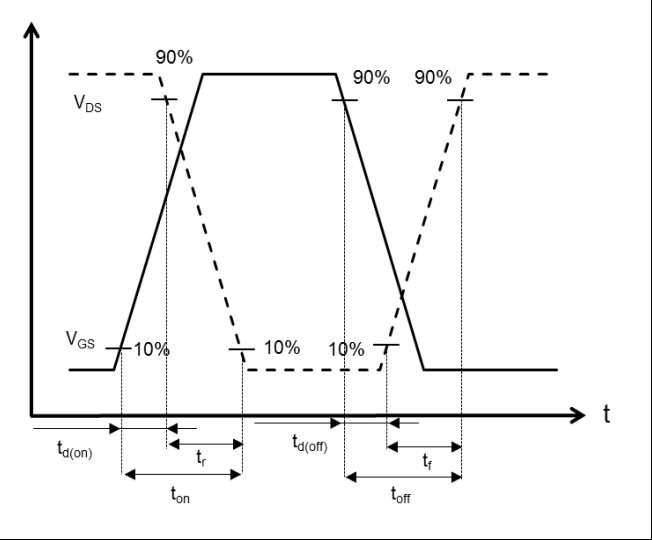


$$V_{GS} = f(Q_G); V_{DCLINK} = 400\text{ V}; I_D = 2\text{ A}$$

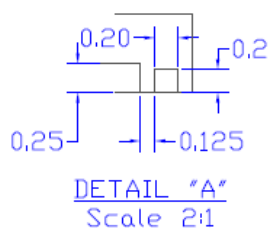
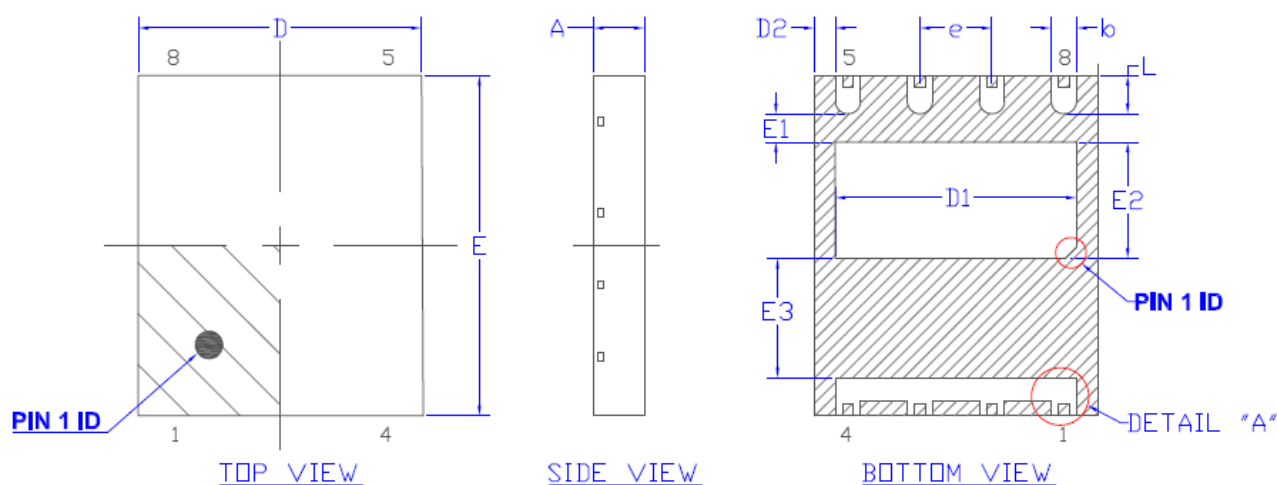
Figure 19 Typ. capacitances



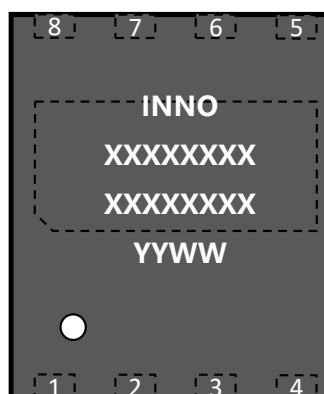
$$C_{XSS} = f(V_{DS}); \text{Freq.} = 100\text{ kHz}$$

Figure 20 Typ. output charge  $Q_{oss} = f(V_{DS})$; Freq. = 100 kHz	Figure 21 Typ. Coss stored Energy  $E_{oss} = f(V_{DS})$; Freq. = 100 kHz
Figure 22 Typ.Switching times with inductive load  $V_{DS}=400V$, $I_D=5A$, $L_{load}=800\mu H$, $V_{GS}=6V$, $R_{on}=10\Omega$, $R_{off}=2\Omega$, $R_{gs}=10k\Omega$	Figure 23 Typ.Switching times waveform 

5 Package outlines



SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2	---	0.203 Ref	---
b	0.40	0.45	0.50
D	5.00 B. S. C		
D1	4.16	4.26	4.36
D2	0.27	0.37	0.47
E	6.00 B. S. C		
E1	0.40	0.50	0.60
E2	1.95	2.05	2.15
E3	---	2.10	---
e	1.27 B. S. C		
L	0.575	0.675	0.775

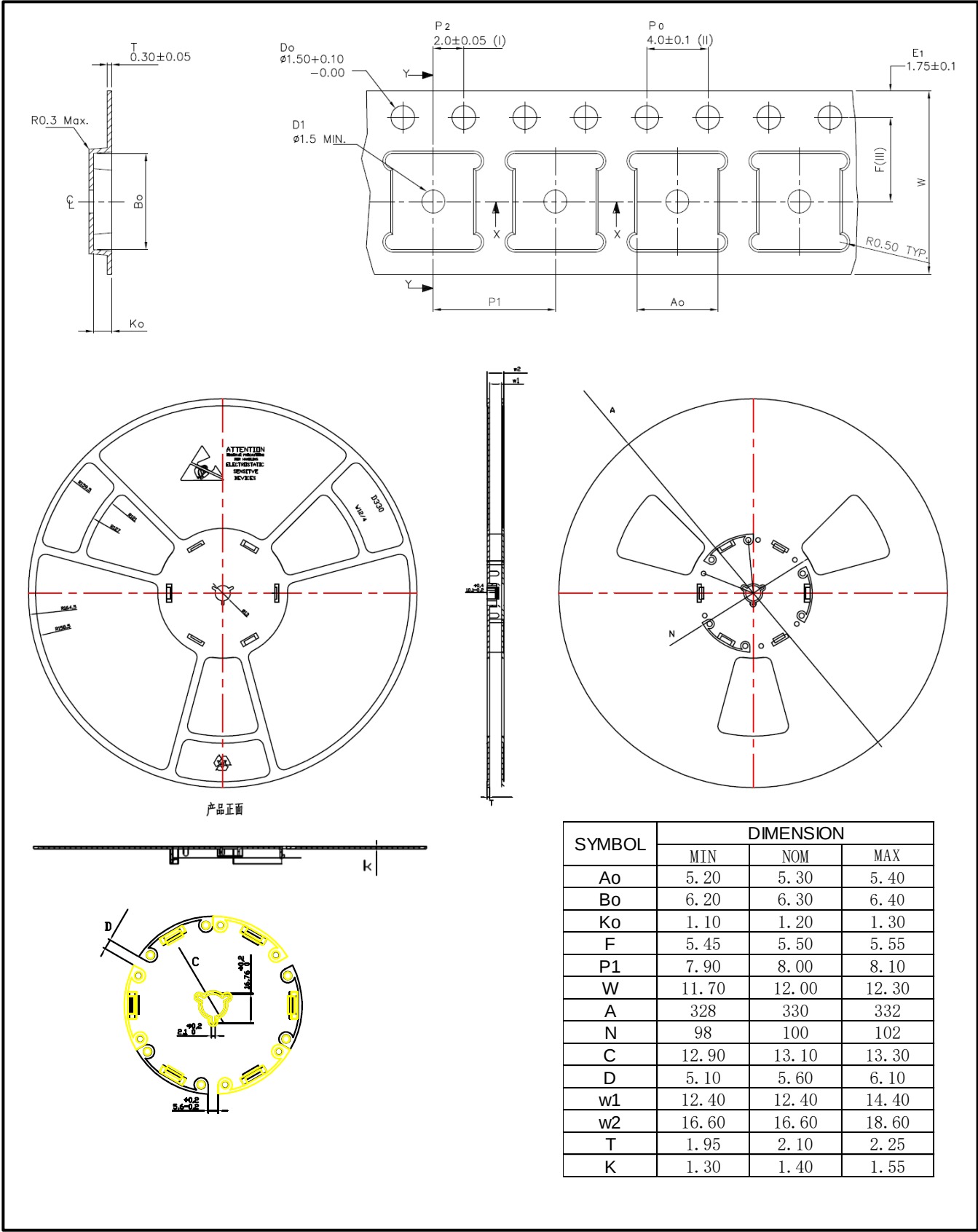


Row	Description	Example
Row1	Company name	INNO
Row2	Product Name(In short)	XXXXXXX
Row3	ASSY lot No.	XXXXXXX

Notes:

- (1) Dimension and tolerance conform to ASME Y14.5-2009.
- (2) All Dimensions are in millimeters.
- (3) Lead coplanarity shall be 0.1 millimeters max.
- (4) Complies with JEDEC MO-229.
- (5) Drawing is not to scale.

6 Reel information



7 Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2021-03-05	Final version release