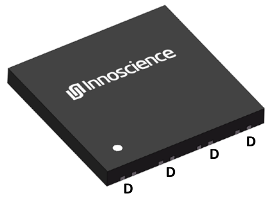
INN650D260A

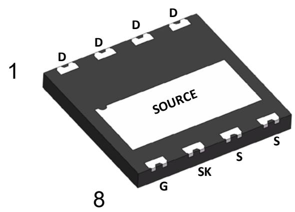
1. General description

650V GaN-on-silicon Enhancement-mode Power Transistor in Dual Flat No-lead package (DFN) with 8 mm × 8 mm size

2. Features



- Enhancement mode transistor-Normally off power switch
- Ultra high switching frequency
- No reverse-recovery charge
- Low gate charge, low output charge
- Qualified for industrial applications according to JEDEC Standards
- ESD safeguard
- RoHS, Pb-free, REACH-compliant



3. Applications

- AC-DC converters
- DC-DC converters
- Totem pole PFC
- Fast battery charging
- High density power conversion
- High efficiency power conversion

4. Key performance parameters

Table 1 Key performance parameters at T_j = 25 °C

Parameter	Value	Unit
$V_{DS,max}$	650	V
$R_{DS(on),max}$ @ V_{GS} = 6 V	260	mΩ
$Q_{G,typ}$ @ V_{DS} = 400 V	2	nC
$I_{D,pulse}$	22	A
Q_{OSS} @ V_{DS} = 400 V	19	nC
Q_{rr} @ V_{DS} = 400 V	0	nC

5. Pin information

Table 2 Pin information

Gate	Drain	Kelvin Source	Source
8	1,2,3,4	7	5,6

Table 3 Ordering information

Type/Ordering Code	Package	Marking
INN650D260A	DFN 8X8	INN65D260A

Table of contents

6. Maximum ratings

at T_j = 25 °C unless otherwise specified.

Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact Innoscience sales office.

Table 4 Maximum ratings

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Drain source voltage	$V_{DS,max}$	-	-	650	V	V_{GS} = 0 V, I_D = 20 µA
Drain source voltage transient [1]	$V_{DS(transient)}$	-	-	750	V	V_{GS} = 0 V, V_{DS} = 750 V
Continuous current, drain source	I_D	-	-	12	A	T_c = 25 °C
Pulsed current, drain source [2]	$I_{D,pulse}$	-	-	22	A	T_c = 25 °C; V_G = 6 V; See Figure 16;
Pulsed current, drain source [2]	$I_{D,pulse}$	-	-	15	A	T_c = 125 °C;V_G = 6 V; See Figure 17;
Gate source voltage, continuous [3]	V_{GS}	-1.4	-	+7	V	T_j = -55 °C to 150 °C
Gate source voltage, pulsed	$V_{GS,pulse}$	-20	-	+10	V	T_j = -55 °C to 150 °C; t_{PULSE} = 50 ns, f = 100 kHz open drain
Power dissipation	P_{tot}	-	-	75	W	T_c = 25 °C
Operating temperature	T_j	-55	-	+150	˚C	
Storage temperature	T_{stg}	-55	-	+150	˚C	

1 $V_{DS(transient)}$ is intended for surge rating during non-repetitive events, t_{PULSE} < 1 µs

2 Pulse = 300 µs

3 The minimum V_{GS} is clamped by ESD protection circuit, as show n in Figure 10

7. Thermal characteristics

Table 5 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction-case	R_{thJC}	-	-	1.65	°C/W	
Reflow soldering temperature	T_{sold}	-	-	260	°C	MSL3

8. Electric characteristics

at T_j = 25 °C, unless specified otherwise

Table 6 Static characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	1.2	1.6	2.2	V	I_D = 11 mA; V_{DS} = V_{GS}; T_j = 25 °C
		-	1.9	-		I_D = 11 mA; V_{DS} = V_{GS}; T_j = 125 °C
Drain-source leakage current	I_{DSS}	-	2	20	µA	V_{DS} = 650 V; V_{GS} = 0 V; T_j = 25 °C
		-	10	120		V_{DS} = 650 V; V_{GS} = 0 V; T_j = 150 °C
Gate-source leakage current	I_{GSS}	-	40	-	µA	V_{GS} = 6 V; V_{DS} = 0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	165	260	mΩ	V_{GS} = 6 V; I_D = 3 A; T_j = 25 °C
		-	322	-	mΩ	V_{GS} = 6 V; I_D = 3 A; T_j = 150 °C
Gate resistance	R_G	-	2	-	Ω	f = 5 MHz; open drain

Table 7 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	73	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Output capacitance	C_{oss}	-	20	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Reverse transfer capacitance	C_{rss}	-	0.2	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Effective output capacitance, energy related [1]	$C_{o(er)}$	-	27	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Effective output capacitance, time related [2]	$C_{o(tr)}$	-	43	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Output charge	Q_{OSS}	-	19	-	nC	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Turn-on delay time	$t_{d(on)}$	-	3	-	nS	See Figure 22
Turn-off delay time	$t_{d(off)}$	-	4	-	nS	See Figure 22
Rise time	t_r	-	7	-	nS	See Figure 22
Fall time	t_f	-	4	-	nS	See Figure 22

1 $C_{O(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V

2 $C_{O(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V

Table 8 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate charge	Q_G	-	2	-	nC	V_{GS} = 0 to 6 V; V_{DS} = 400 V; I_D= 3 A
Gate-source charge	Q_{GS}	-	0.18	-	nC	
Gate-drain charge	Q_{GD}	-	0.62	-	nC	
Gate Plateau Voltage	V_{Plat}	-	2.3	-	V	V_{DS} = 400 V; I_D= 3 A

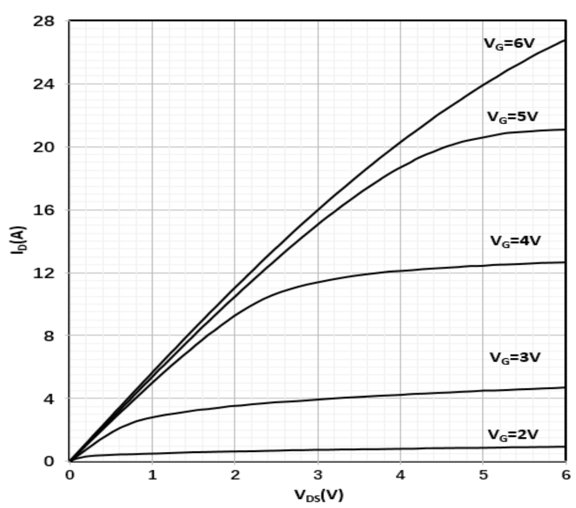
Table 9 Reverse conduction characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	V_{SD}	-	2.7	-	V	V_{GS} = 0 V; I_{SD}= 3 A
Pulsed current, reverse	$I_{S,pulse}$	-	-	22	A	V_G = 6 V
Reverse recovery charge	Q_{rr}	-	0	-	nC	I_{SD} = 3 A; V_{DS} = 400 V
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

9. Electric characteristics diagrams

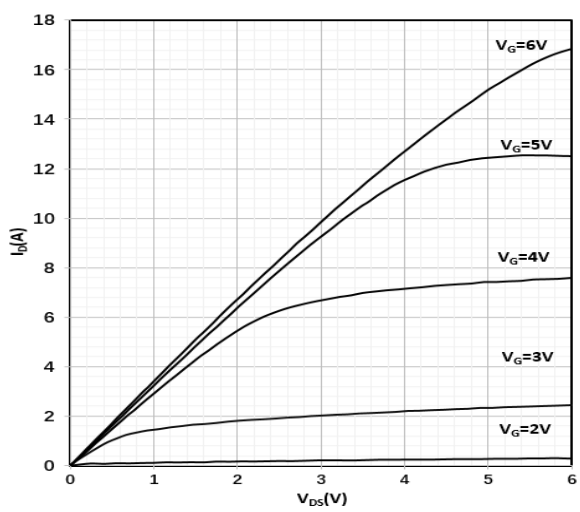
at T_j = 25 °C, unless specified otherwise

Figure 1 Typ. output characteristics



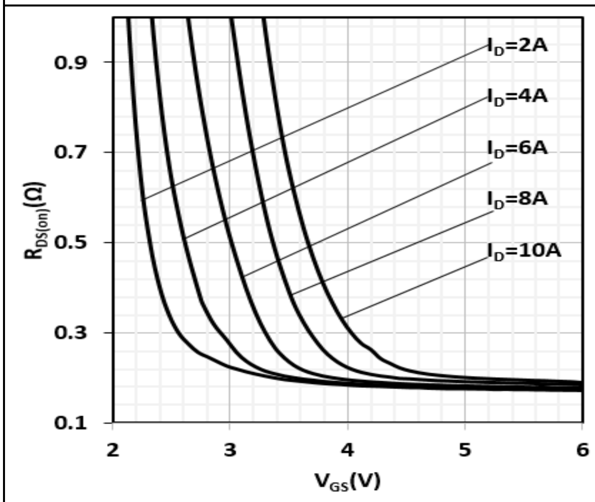
$I_D = f(V_{DS},V_{GS})$; T_j = 25 °C

Figure 2 Typ. output characteristics



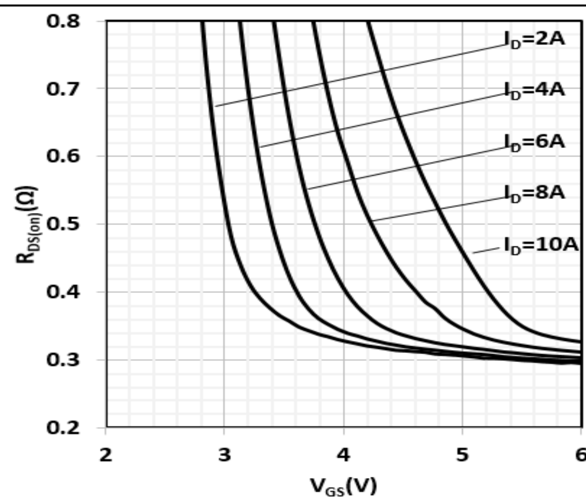
$I_D = f(V_{DS},V_{GS})$; T_j = 125 °C

Figure 3 Typ. Drain-source on-state resistance



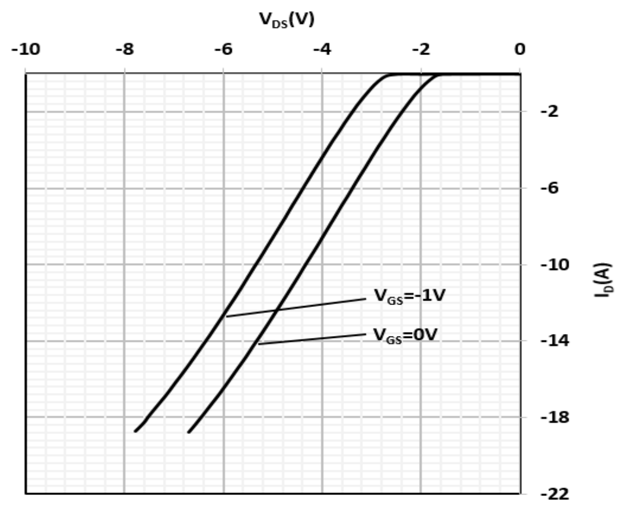
$R_{DS(on)} = f(I_{DS},V_{GS})$; T_j = 25 °C

Figure 4 Typ. Drain-source on-state resistance



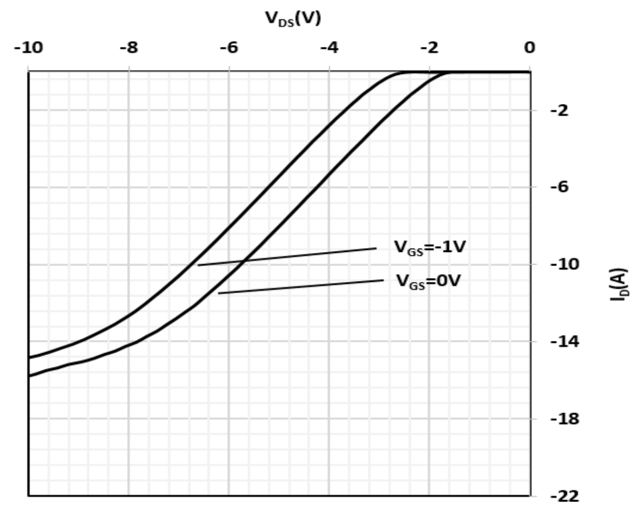
$R_{DS(on)} = f(I_{DS},V_{GS})$; T_j = 125 °C

Figure 5 Typ. channel reverse characteristics



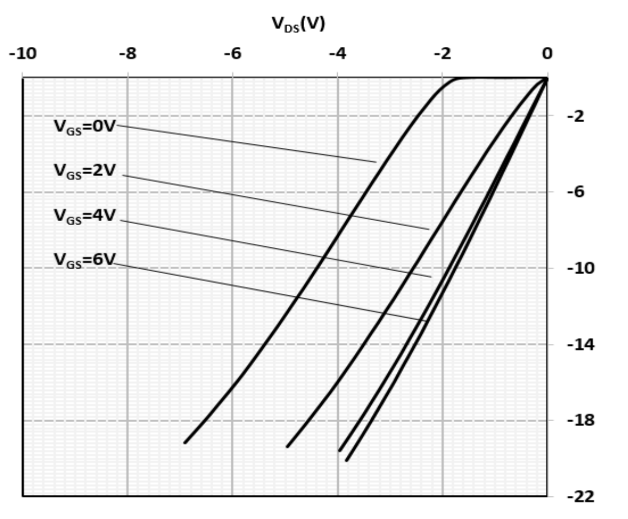
ID = f(VDS,VGS); Tj= 25 °C

Figure 6 Typ. channel reverse characteristics



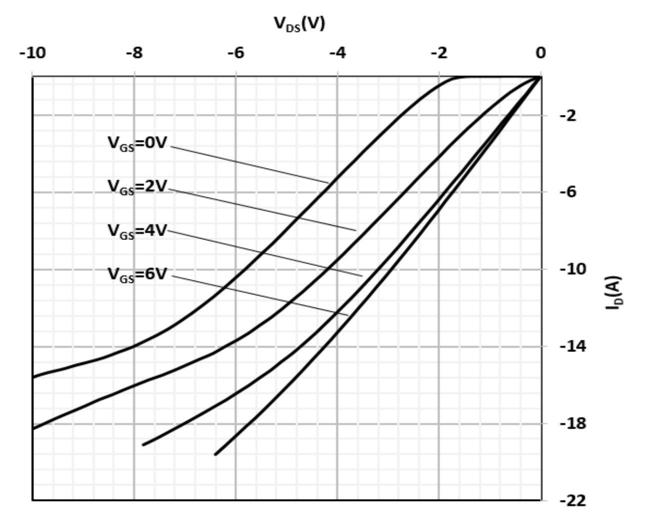
ID = f(VDS,VGS); Tj = 125 °C

Figure 7 Typ. channel reverse characteristics



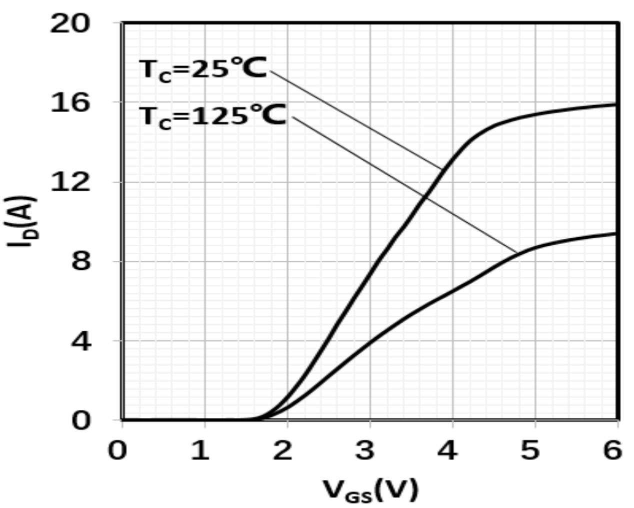
ID = f(VDS,VGS); Tj = 25 °C

Figure 8 Typ. channel reverse characteristics



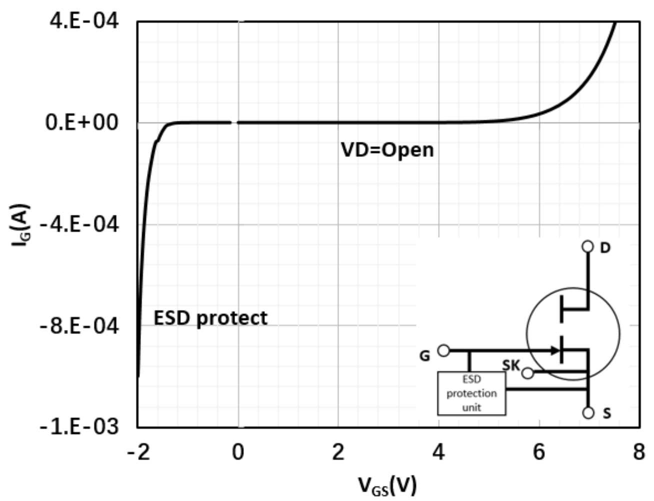
ID = f(VDS,VGS); Tj = 125 °C

Figure 9 Typ. transfer characteristics



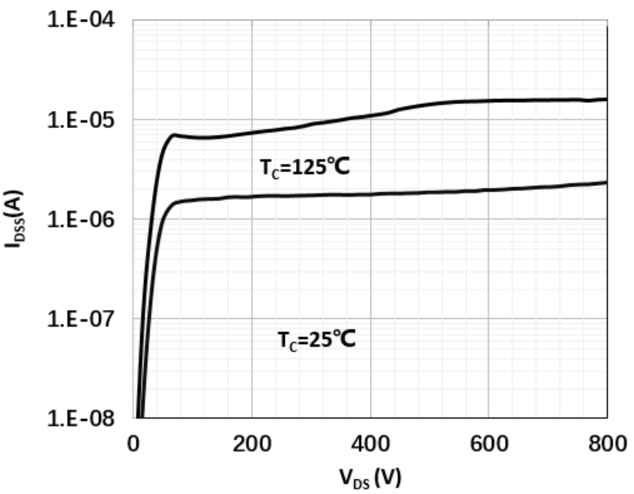
$I_D = f(V_{GS})$; V_{DS}= 3 V

Figure 10 Typ. Gate-to-Source leakage



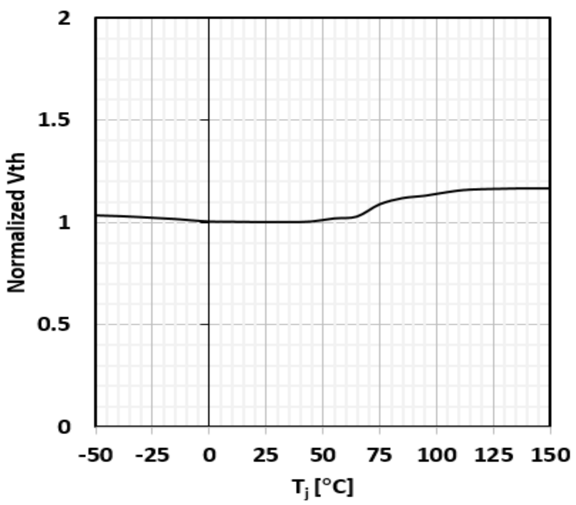
$I_G = f(V_{GS})$; Ig reverse turn on by ESD unit

Figure 11 Drain-source leakage characteristics



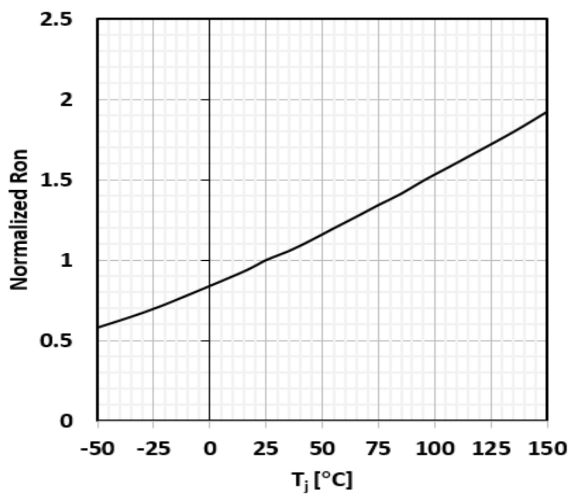
$I_{DSS} = f(V_{DS})$; V_{GS} = 0 V

Figure 12 Gate threshold voltage



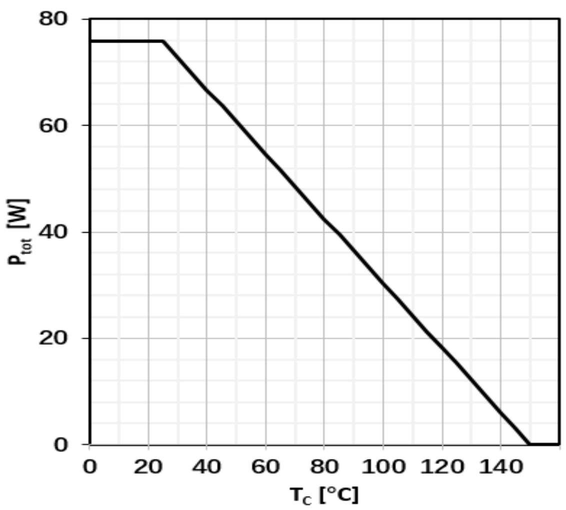
$V_{TH} = f(T_j)$; $V_{GS} = V_{DS}$; $I_D = 11$ mA

Figure 13 Drain-source on-state resistance



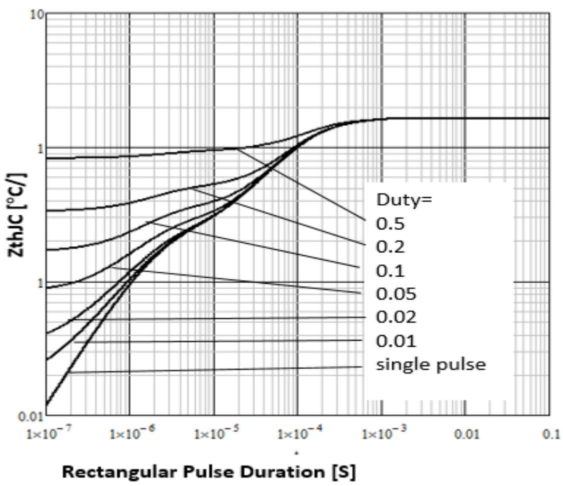
$R_{DS(on)} = f(T_j)$; $I_D = 3$ A; V_G=6V

Figure 14 Power dissipation



$P_{tot} = f(T_C)$

Figure 15 Max.transient thermal impedance



$Z_{thJC} = f(t_P, D)$

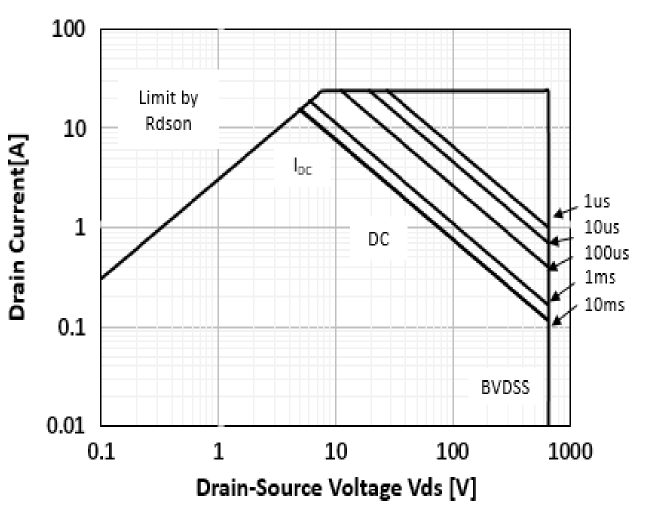
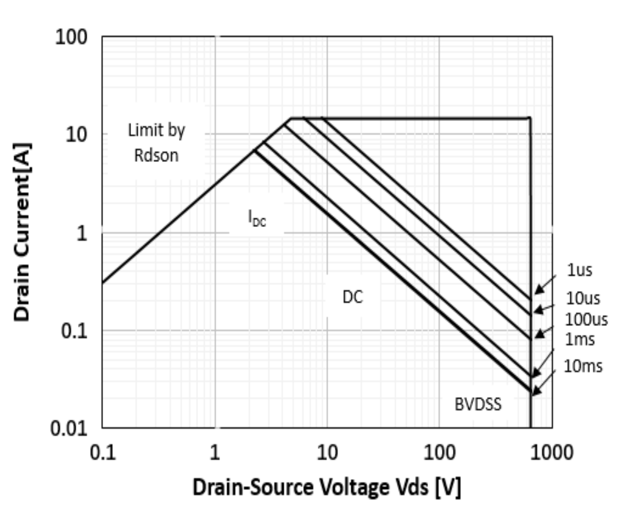
Figure 16 Safe operating area	Figure 17 Safe operating area
	
$I_D = f(V_{DS})$; $T_C = 25$ °C	$I_D = f(V_{DS})$; $T_C = 125$ °C

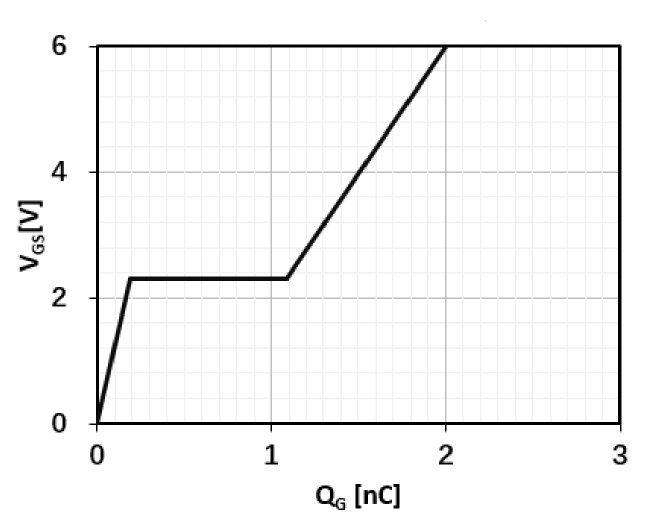
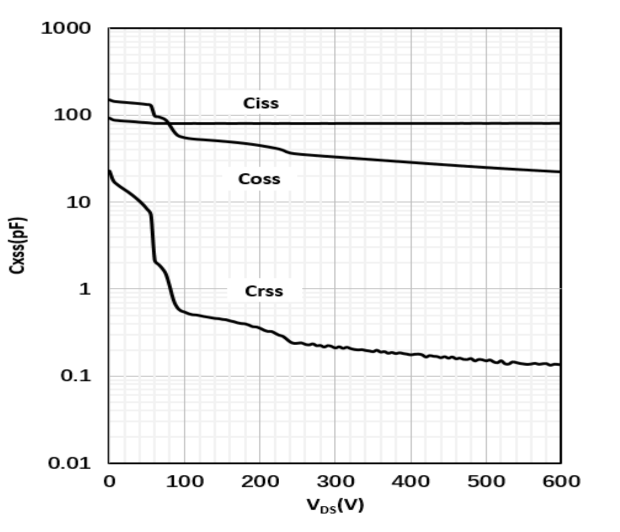
Figure 18 Typ. gate charge	Figure 19 Typ. capacitances
	
$V_{GS} = f(Q_G)$; $V_{DCLINK} = 400$ V; $I_D = 3$ A	$C_{XSS} = f(V_{DS})$; Freq. = 100 kHz

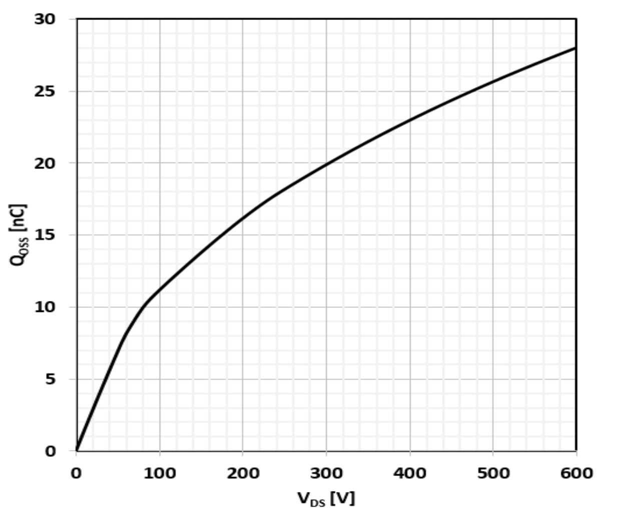
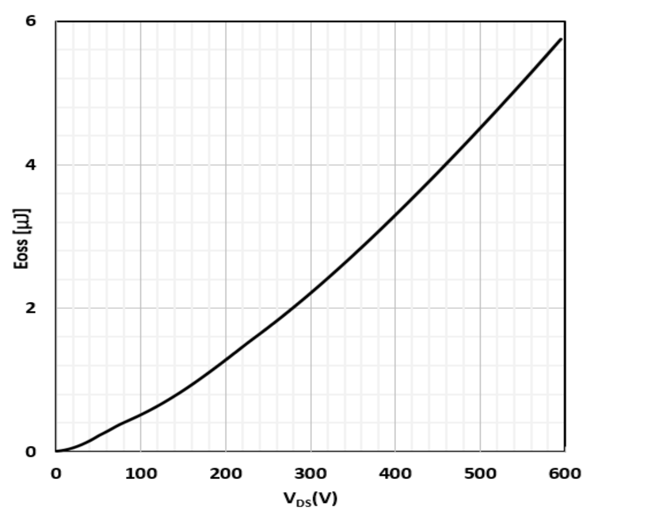
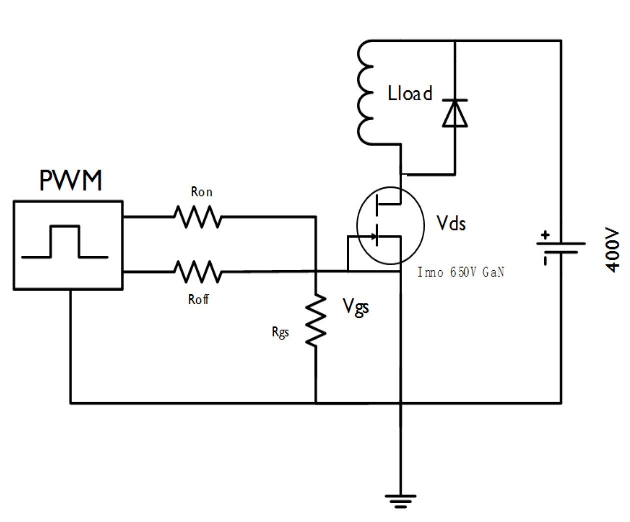
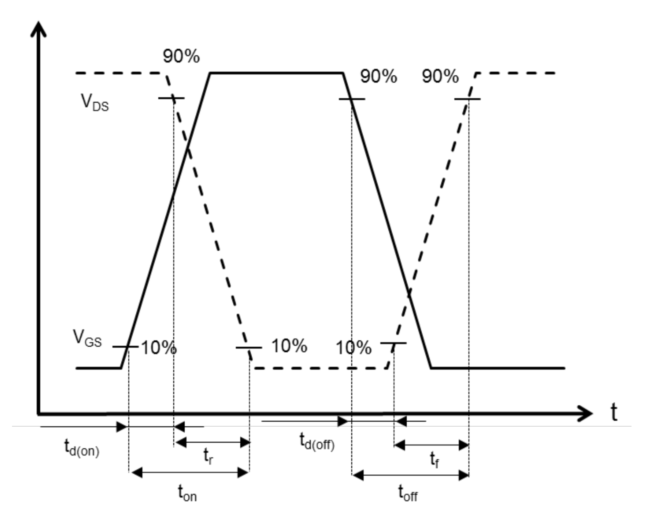
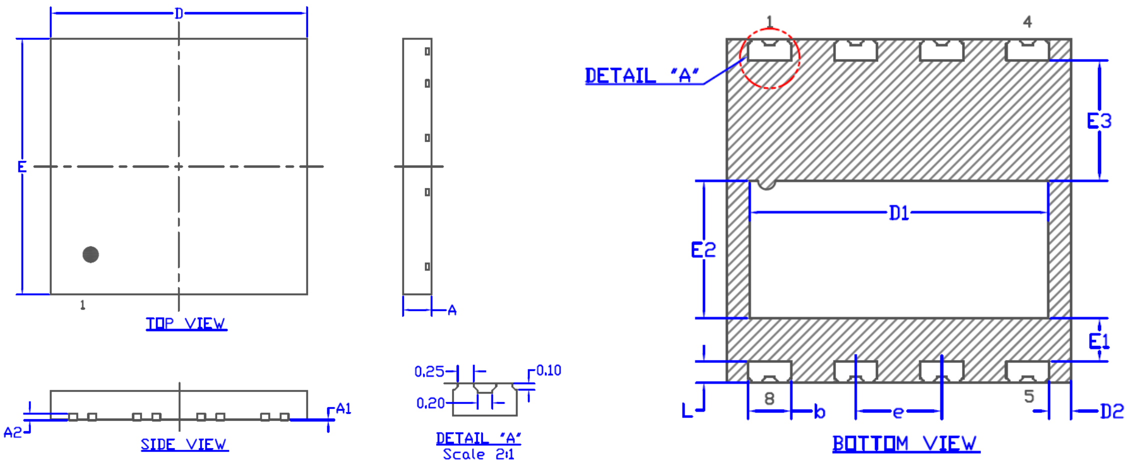
Figure 20 Typ. output charge	Figure 21 Typ. Coss stored Energy
	
$Q_{OSS} = f(V_{DS})$; Freq. = 100 kHz	$E_{OSS} = f(V_{DS})$; Freq. = 100 kHz

Figure 22 Typ.Switching times with inductive load	Figure 23 Typ.Switching times waveform
	
V_{DS}=400V, I_D=5A, L_{load}=800uH, V_{GS}=6V, R_{on}=10Ω, R_{off}=2Ω, R_{gs}=10kΩ	

10.Package outlines



SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2	---	0.203 Ref	---
b	0.95	1.00	1.05
D	8.00 B.S.C		
D1	6.84	6.94	7.04
D2	0.40	0.50	0.60
E	8.00 B.S.C		
E1	0.90	1.00	1.10
E2	3.10	3.20	3.30
E3	2.70	2.80	2.90
e	2.00 B.S.C		
L	0.40	0.50	0.60
NOTE: All dimensions in mm			

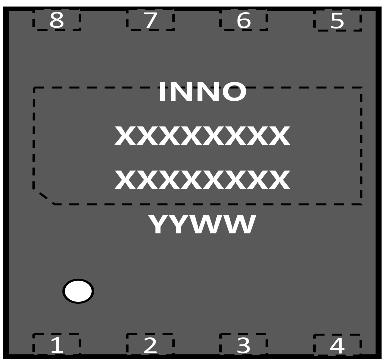
Pad 1,2,3,4 is Drain

Pad 5,6 is Source

Pad 7 is Kelvin Source

Pad 8 is Gate

Pad 9 is Attach Pad



Row	Description	Example
Row1	Company name	INNO
Row2	Product Name(In short)	XXXXXXXX
Row3	ASSY lot No.	XXXXXXXX

Notes:
(1) Dimension and tolerance conform to ASME Y14.5-2009.
(2) All Dimensions are in millimeters.
(3) Lead coplanarity shall be 0.1 millimeters max.
(4) Complies with JEDEC MO-229.
(5) Drawing is not to scale.

11. Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2021-4-13	1.0 version release