Datasheet

Single-phase BLDC Motor Controller with Built-in Hall Sensor FA1611S

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Contents

FA1611S Single-phase BLDC Motor Controller with Built-in Hall Sensor

1 System Introduction

1.1 Overview

FA1611S is a fully integrated IC with built-in MOS and Hall-based sensor for single-phase BLDC motor driver applications. It supports soft-switching square-wave control mode, and features with low noise. Motor control parameters, such as soft-switching slope, lead angle, etc., can be flexibly configured via GUI to achieve required efficiency and reduce noise, in order to meet different application requirements. Moreover, the chip supports multi-segment speed control curve, protection restart configurations and FG/RD output to fulfill different input and output requirements.

1.2 Applications

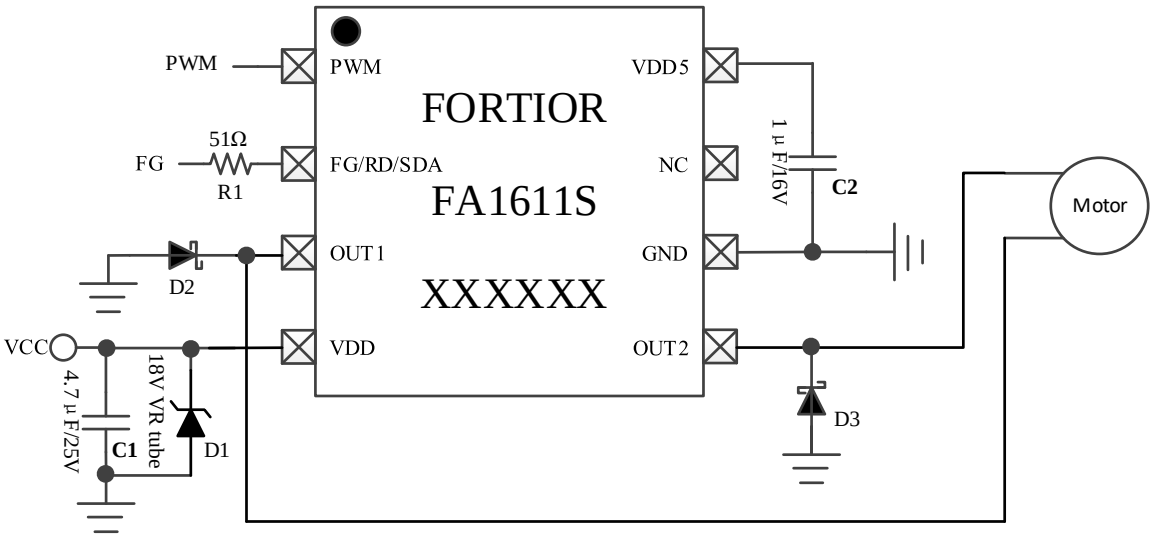
Cooling fans, water-cooling fans, refrigerator fans, etc.

1.3 Features

- VCC range: 3.3V ~ 16V
- Drive current: 450mA@85℃
- High level of integration with built-in MOS and Hall-based sensor
- Highly sensitive Hall-based sensor
- Soft-switching square-wave control for single-phase motor
- FG and RD output
- SPEED and I^2C modes for motor speed regulation
- Built-in EFUSE
- Configurable multi-segment output curve
- Forward and reverse direction control
- Soft-on feature protects the motor from abrupt startup and reduces current shock and noise
- Support protection features, including current limiting protection (CLP), over-current protection (OCP), temperature sensor detect (TSD), motor lock protection (MLP), etc.

1.4 Typical Application Diagram

1.4.1 FA1611S



C1 and C2 shall be mounted close to IC PIN on the PCB.

Figure 1-1 Typical Application Diagram of FA1611S

1.5 Functional Block Diagram

1.5.1 FA1611S

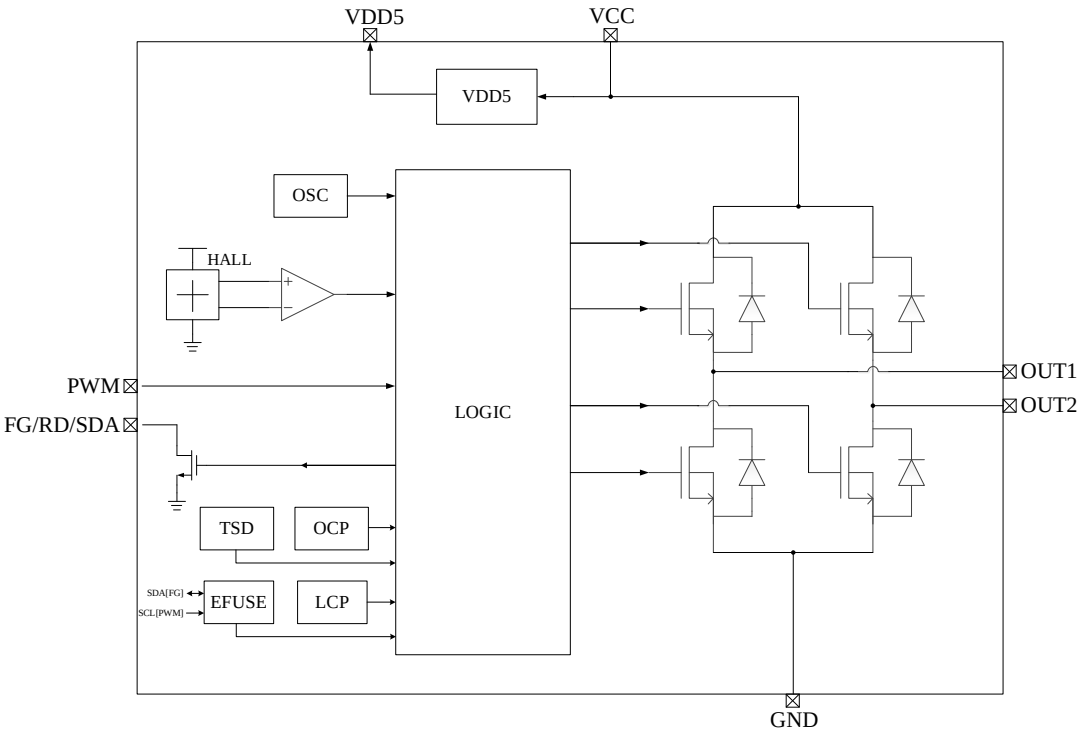


Figure 1-2 Functional Block Diagram of FA1611S

1.5.2 Pinout Diagram

1.5.3 FA1611S SOP8

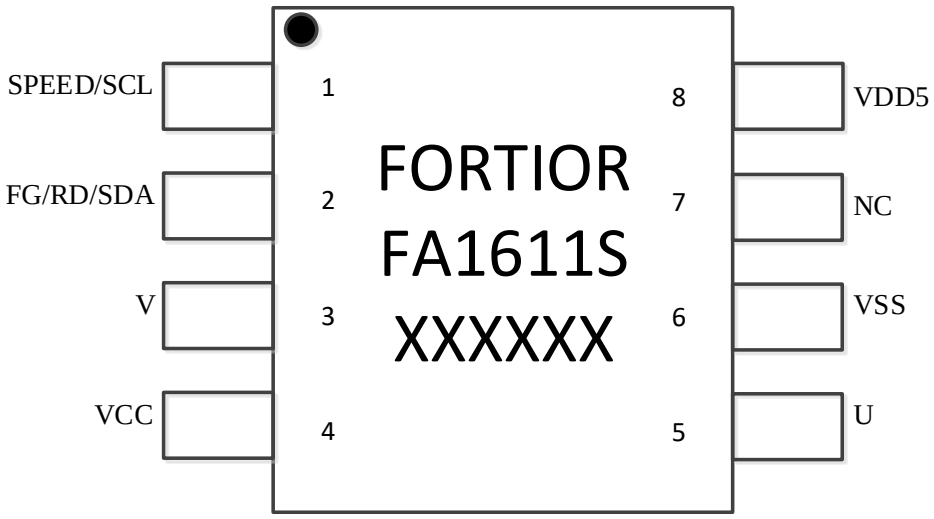


Figure 1-3 FA1611S SOP8 Pinout Diagram

1.6 Pin Definitions

The IO types are defined as follows:

- DI = Digital Input
- DB = Digital Bidirectional
- DO = Digital Output
- P = Power Supply

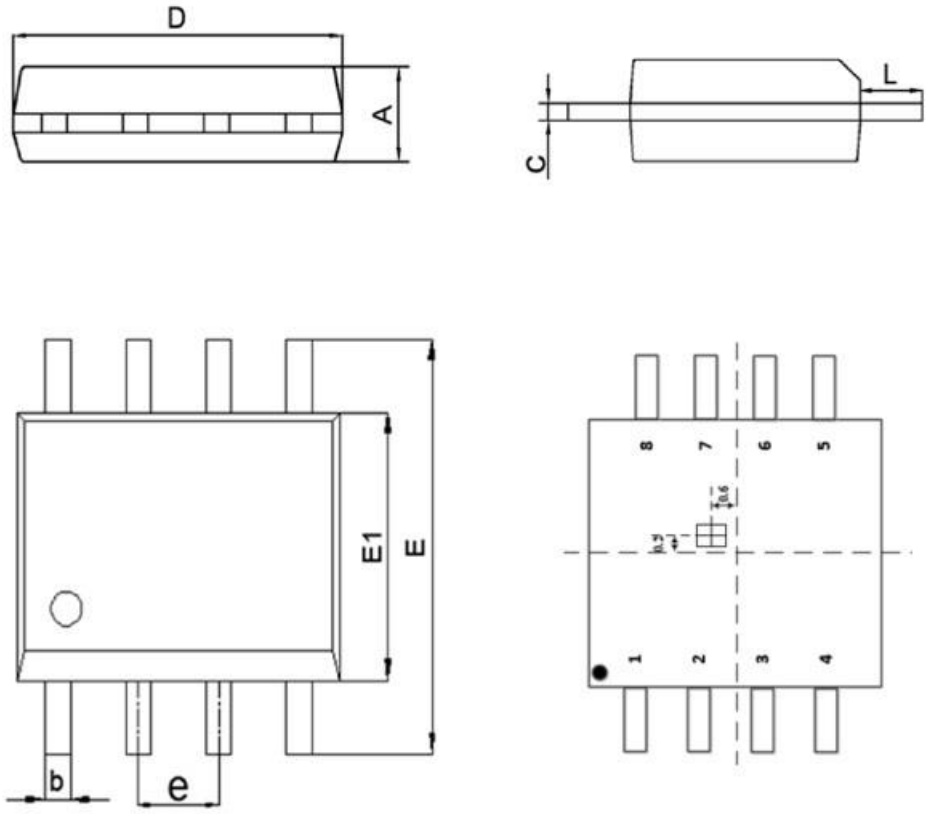
1.6.1 FA1611S SOP8 Pins

Table 1-1 FA1611S SOP8 Pin Descriptions

Pin	FA1611S SOP8	IO Type	Function Description
SPEED/ SCL	1	DI/ DB	Speed control input; PWM speed regulation; Frequency ranges: 0.1 ~ 100kHz I^2C SCL
FG/RD/ SDA	2	DO/ DB	Speed indication output, configured as collector open-drain output I^2C SDA, configured as collector open-drain output
V	3	DO	V-phase output from H bridge
VCC	4	P	Power supply. The input voltage range is 3.3V ~ 16V, with a capacitor of 4.7μF or above connected to ground
U	5	DO	U-phase output from H bridge
VSS	6	P	Ground
NC	7	-	Not connected
VDD5	8	P	Internal LDO output, with a 1μF ~ 4.7μF capacitor connected to ground

2 Package Information

2.1 FA1611S SOP8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.30	1.40	1.50
b	0.33	0.40	0.47
c	0.20	-	0.25
D	4.70	4.90	5.10
E	5.90	6.00	6.10
E1	3.80	3.90	4.00
e	1.27(BSC)		
L	0.90	1.00	1.10

Figure 2-1 FA1611S SOP8 Package Drawings and Dimensions

3 Ordering Information

Table 3-1 Model Selections

Model	Power Supply (V)	R_{DSON} (High Side + Low Side) (Ω)	Control Features			Protection Features					Operating Temperature T_j(°C)	Lead-free	Package
			Driver Type	Speed Regulation		OCP / CLP	UVLO	OVLO	MLP	TSD			
				I²C	PWM								
FA1611S	3.3~16	1	Soft-switching Square-wave	√	√	√	-	-	√	√	-40 ~ 150	√	SOP8

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4-1 Absolute Maximum Ratings[1]

(T_A = 25℃ and VCC = 12V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Operating Ambient Temperature T_A		-40	-	85	℃
Operating Junction Temperature T_J		-40	-	150	℃
Storage Temperature		-55	-	150	℃
VCC to VSS Voltage		-0.3	-	20	V
VDD5 to VSS Voltage		-0.3	5	6.5	V
U/V to VSS Voltage		-0.3	-	VCC + 0.3	V
SPEED/SCL, FG/RD/SDA, NC to VSS Voltage		-0.3	-	VDD5 + 0.3	V

Note: Stress values greater than "Absolute Maximum Ratings" listed above may cause irremediable damages to the device. These are stress ratings only, and it is NOT recommended to use your device in conditions that go beyond these stress ratings. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

4.2 Global Electrical Characteristics

Table 4-2 Global Electrical Characteristics

(T_A = 25℃ and VCC = 12V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC Operating Voltage		3.3	-	16	V
VDD5 Operating Voltage	I = 0~10mA	4.8	5	5.2	V
I_{VCC} Operating Current	T_A = 85℃	-	-	450	mA
I_{VCC} Standby Current		-	2.5	-	mA
Rdson (H+L)		-	1	-	Ω
Output Signal Wave		22	24	26	kHz
Positive Magnetic Threshold		-	1.5	3	mT
Negative Magnetic Threshold		-3	-1.5	-	mT

4.3 Protection Electrical Characteristics

Table 4-3 Protection Electrical Characteristics

(T_A = 25℃ and VCC = 12V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Motor Lock Protection ON Time during Startup T_{ON_START}		-	0.75	-	s
Motor Lock Protection ON Time during Normal Operation T_{ON_RUN}		-	0.3	-	s

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Motor Lock Protection OFF Time T_{OFF}		-	4	-	s
CLP Current I_{LCP}		-	1.2	-	A
OCP Current I_{OCP}		-	1.6	-	A
TSD Threshold Temperature		-	165	-	℃
TSD Recovery Temperature		-	140	-	℃

4.4 IO Electrical Characteristics (DIR/SPEED/FG)

Table 4-4 IO Electrical Characteristics (DIR/SPEED/FG)

(T_A = 25℃ and VCC = 12V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
High-level Input Voltage V_{IH}	VCC ≥ 5.5V	2.8	-	5.5	V
High-level Input Voltage V_{IH}	VCC < 5.5V	2.8	-	VCC	
Low-level Input Voltage V_{IL}		-0.3	-	1	V
SPEED Pull-up Resistor[1]		-	33	-	kΩ
SPEED Pull-down Resistor[1]		-	33	-	kΩ

Note:

[1] SPEED pull-up resistor or pull-down resistor is selected according to internal configurations.

4.5 Package Thermal Resistance

Table 4-5 SOP8 Package Thermal Resistance

Parameter	Test Conditions	Value	Unit
Junction-to-ambient Temperature Thermal Resistance θ_{JA}[1]	JEDEC standard, 1S0P PCB	150	℃/W

Note: The actual measurements may vary depending on the conditions.

5 Function Description

5.1 Speed Control

5.1.1 Speed Control Modes

The chip supports two types of speed control input interface: SPEED and I^2C, and only one of them can be chosen at a time. If SPEED is selected, the speed signal is input to SPEED pin, and if I^2C is selected, SPEED pin serves as the clock line (SCL) and FG/RD/SDA pin as the data line (SDA).

5.1.2 Speed Control Curve

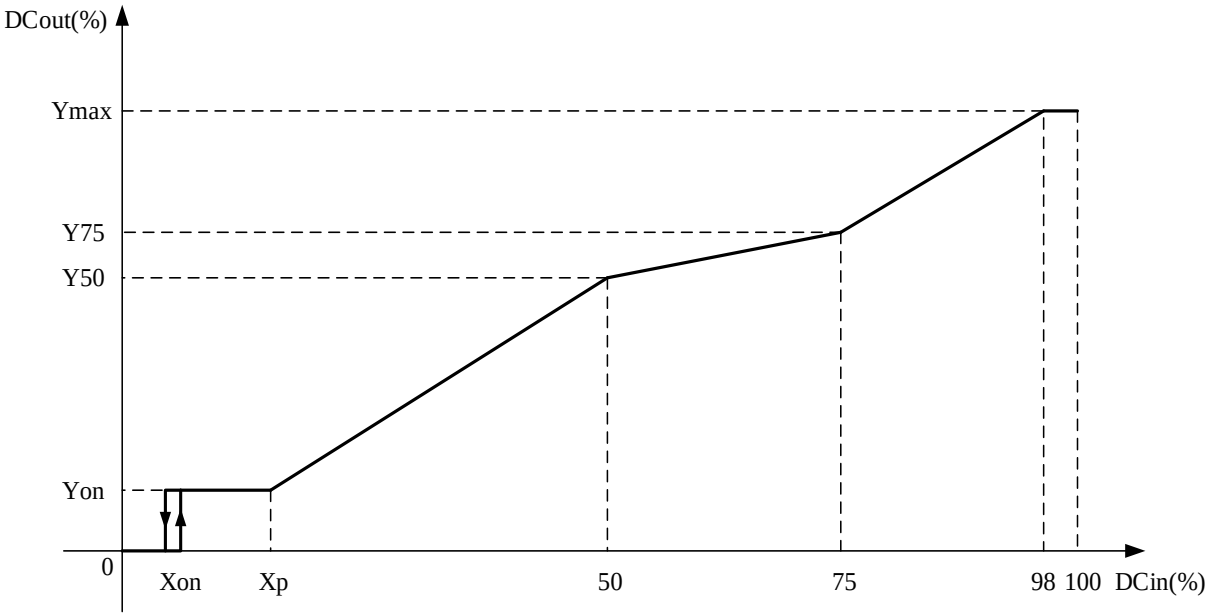


Figure 5-1 Speed Control Curve

The chip outputs four-segment speed control curves, where Xon ranges from 0 to 50%, Xp from 0 to 50%, Yon from 0 to 50%, Y50 from 25 to 75%, Y75 from 50 to 100% and Ymax from 75 to 100%, and the slope of each curve must be positive.

5.2 Lead Angle Settings

The lead angle is controlled by Lead_Lag0/1/2/3 and ranges from -11° to 40°. The output lead angle is determined by SPEED input.

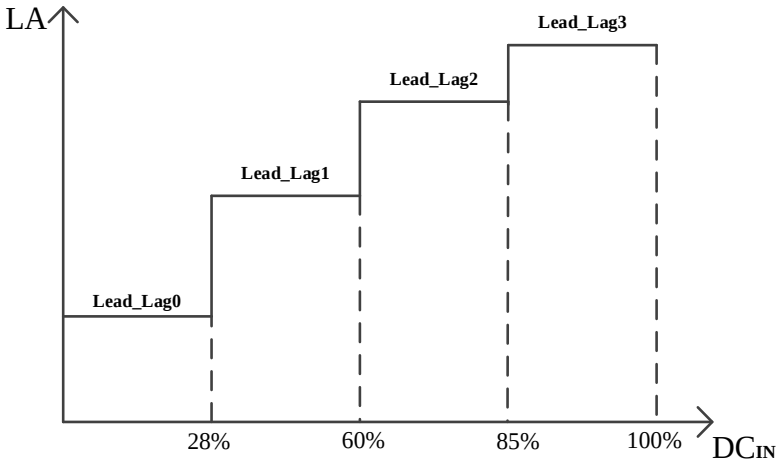


Figure 5-2 Lead Angle Settings

5.3 Startup and Output Control

The startup duty cycle can be set as 0~50% or 30~70%, and startup acceleration as 90%/s, 65%/s, 45%/s or 25%/s.

Speed detection and fault indication (FG/RD/SDA) pin is an open-drain output. Frequency multiplication of the FG signals can be set as 1, 1/2, 1/3 or to follow Hall output. RD signals can be output as STABLE, ~STABLE or ~RUN signal.

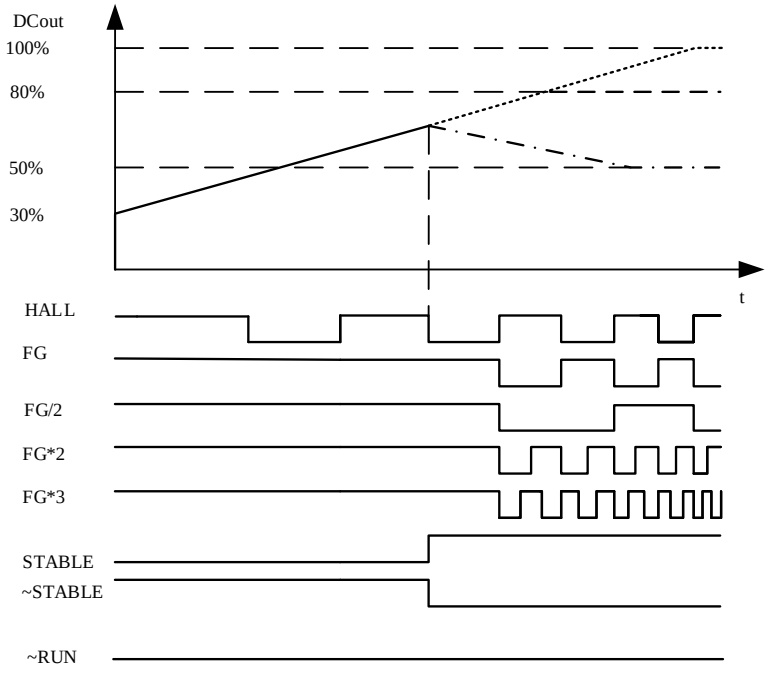


Figure 5-3 Output Waveform during Startup

(Startup Duty Cycle at 30~70% and Acceleration at 95%/s)

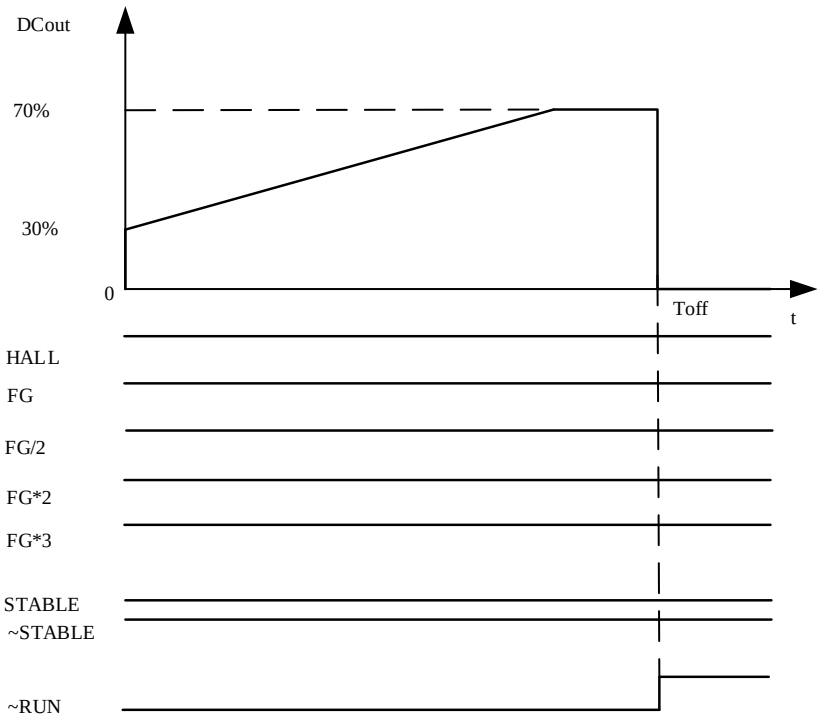


Figure 5-4 Output Waveform of Motor Lock Detection during Startup

(Startup Duty Cycle at 30~70% and Acceleration at 95%/s)

5.4 SPEED

Speed control (SPEED) pin is used to input duty cycle for speed regulation depending on the settings. In addition, SPEED pin serves as the clock line (SCL) for I^2C communication.

5.5 Motor Lock Protection

Motor lock protection circuitry monitors operating state of the motor. Motor lock protection ON time during startup is 0.75s, and motor lock protection ON time during normal operation is 0.3s. When the conditions (Hall-based duration) for motor lock are satisfied, the chip shuts down and waits for 4s to decide whether to restart (depending on software settings).

5.6 Current Limiting Protection

The chip turns off the high-side output when it detects the current limiting protection signal, and releases the high-side output until the protection signal returns to the normal.

5.7 Overcurrent Protection

When the sampling current exceeds the overcurrent protection threshold, the chip shuts down and waits for 4s to decide whether to restart (depending on software settings).

6 Revision History

Rev.	Description	Date	Prepared By
V1.2	First release, translated from Chinese version 1.2	2023/10/20	Eric Deng
V1.3	1. Added test condition "VCC ≥ 5.5V" to the parameter "High-level Input Voltage V_{IH}" in Table 4-4 IO Electrical Characteristics (DIR/SPEED/FG), modified the minimum value "0.7*VDD5" as 2.8V and added the maximum value 5.5V; 2. Added the parameter "High-level Input Voltage V_{IH}" (test condition VCC < 5.5V) in Table 4-4 IO Electrical Characteristics (DIR/SPEED/FG); 3. Modified the maximum value "0.2*VDD5" of Low-level Input Voltage V_{IL} in Table 4-4 IO Electrical Characteristics (DIR/SPEED/FG) as "1V" and added the minimum value 0.3V.	2024/03/07	Eric Deng

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