SDM100PL06SV

-60V P-Channel MOSFETs

Rev A.0

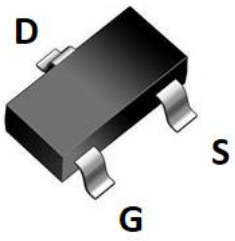
Feature

- ✧ Low $R_{DS(ON)}$
- ✧ Low Gate Charge
- ✧ Green product (RoHS compliant) , lead free
- ✧ 100% UIS Tested, 100% Rg Tested
- ✧ AEC-Q101 qualified

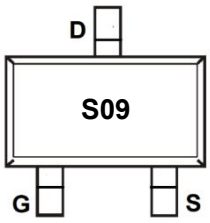
Product Summary

V_{DS}	-60	V
$V_{GS(th)\_Max}$	-2.5	V
$R_{DS(ON)\_Tpy}$ (at V_{GS} =-10V)	75	mΩ
I_D (at V_{GS} =-10V) (1)	-3.4	A

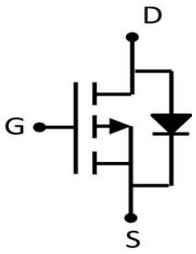
Type	Package	Marking	Outline	Media	Quantity (pcs)
SDM100PL06SV	SOT-23	S09	Tape	7'' Reel	3000



SOT-23 top view



Marking and Pin Assignment



Schematic Diagram

Absolute Maximum Ratings (Rating at T_a=25°C unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DS}	-60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (1)	T_C=25°C	I_D	-3.4	A
Pulsed Drain Current (1)		I_{DM}	-12	A
Power Dissipation	T_C=25°C	P_D	1.25	W
Junction and Storage Temperature Range		T_J, T_{stg}	-55 ~150	°C

Electrical Characteristics (Rating at T_a=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250μA, V_{GS} =0V	-60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-48V, V_{GS} =0V	-	-	-1	μA
I_{GSS}	Gate-Body Leakage Current	V_{DS}=0V, V_{GS} =±20V	-	-	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D=-250μA	-1	-	-2.5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-10V, I_D=-4A	-	75	100	mΩ
		V_{GS}=-4.5V, I_D=-4A	-	85	120	
V_{SD}	Diode Forward Voltage	I_S=-0.75A, V_{GS}=0V	-	-	-1.3	V
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-30V, f=1MHz	-	835	-	pF
C_{oss}	Output Capacitance		-	41	-	pF
C_{rss}	Reverse Transfer Capacitance		-	33	-	pF
R_g	Gate Resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	-	15.1	-	Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}=-10V, V_{DS}=-30V, I_D=-2A	-	17	-	nC
Q_{gs}	Gate Source Charge	V_{GS}=-10V, V_{DS}=-15V, I_D=-1.7A	-	3.3	-	nC
Q_{gd}	Gate Drain Charge		-	1.7	-	nC
$t_{D(on)}$	Turn-On Delay Time	V_{GS}=-10V,V_{DD}=-30V,I_D=-2A, R_G=4.5Ω, R_L=15Ω	-	8.3	-	ns
t_r	Turn-On Rise Time		-	23	-	ns
$t_{D(off)}$	Turn-Off Delay Time		-	103	-	ns
t_f	Turn-Off Fall Time		-	43	-	ns
t_{rr}	Body Diode Reverse Recovery Time	I_{SD}=-2A, di/dt=100A/μs	-	17	-	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_{SD}=-2A, di/dt=100A/μs	-	15	-	nC

Thermal Resistances

Symbol	Parameter	Typ	Max	Unit
$R_{\theta JC}$	Thermal resistance from junction to Case	-	2.5	°C /W
$R_{\theta JA}$	Thermal Resistance from Junction to Ambient (2)	-	100	°C /W

Notes:

1. Pulse width ≤100us, duty cycle ≤1%, limited by Tjmax.
2. Device mounted on FR-4 substrate PC board, 2ozcopper, with 1-inch square copper plate in still air

Typical Electrical and Thermal Characteristics

Figure 1: Saturation Characteristics

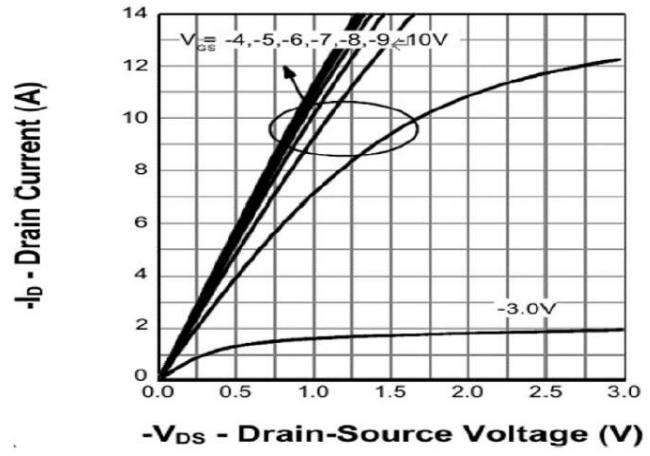


Figure 2: Transfer Characteristics

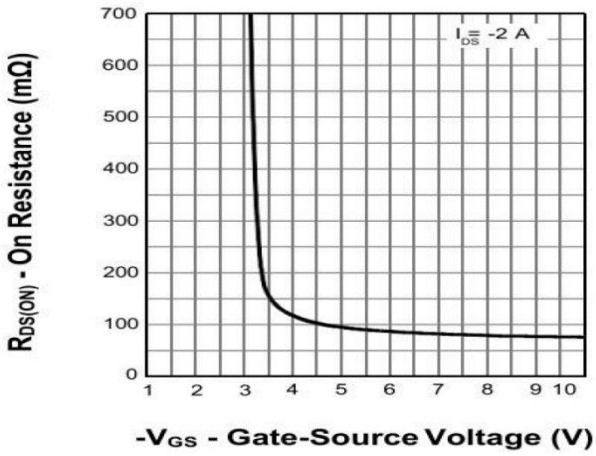


Figure 3: $R_{DS(ON)}$ vs. Drain Current

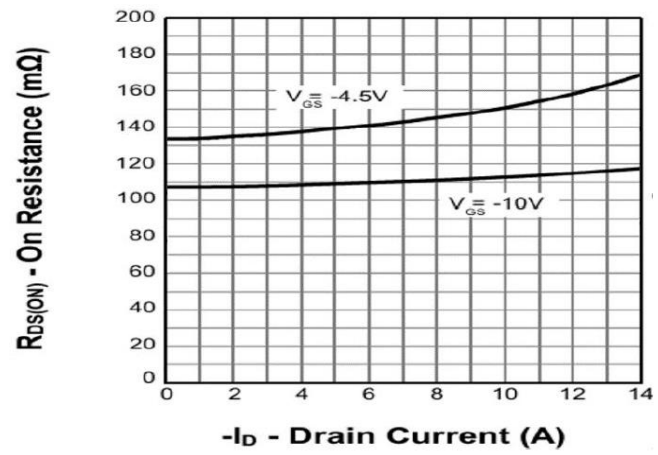


Figure 4: $R_{DS(ON)}$ vs. Junction Temperature

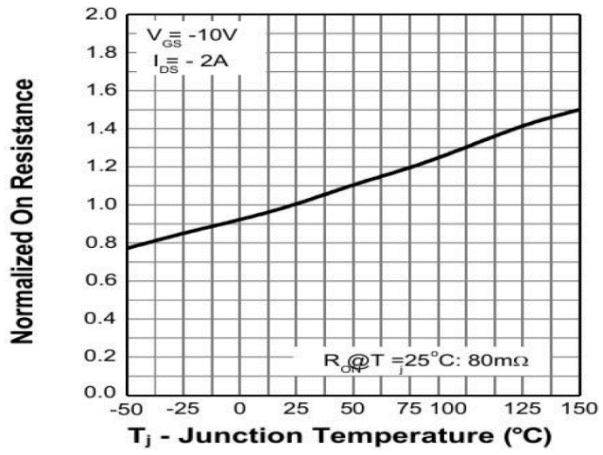


Figure 5: Normalized Threshold Voltage vs. Junction Temperature

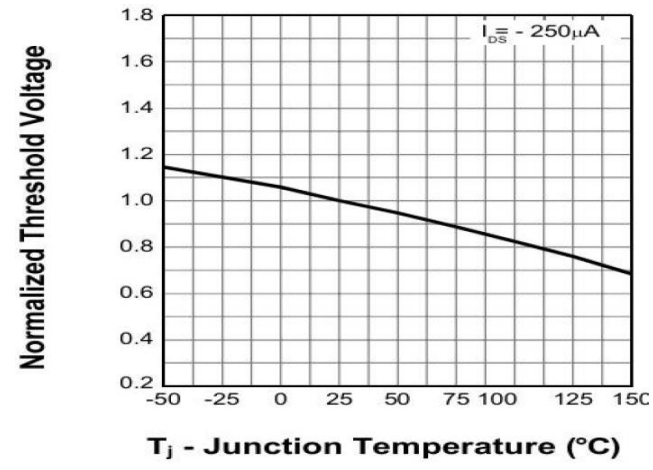
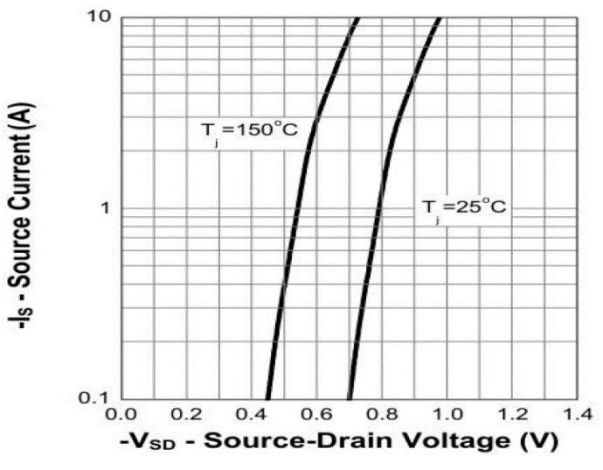


Figure 6: Body-Diode Characteristics



Typical Electrical and Thermal Characteristics

Figure 7: Gate-Charge characteristics

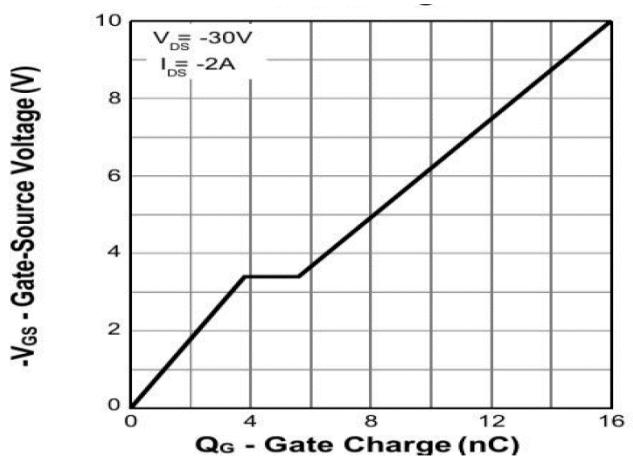


Figure 8: Capacitance characteristics

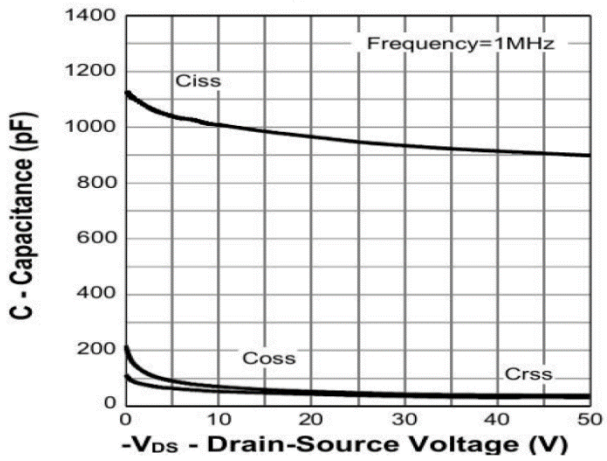


Figure 9: Current De-rating

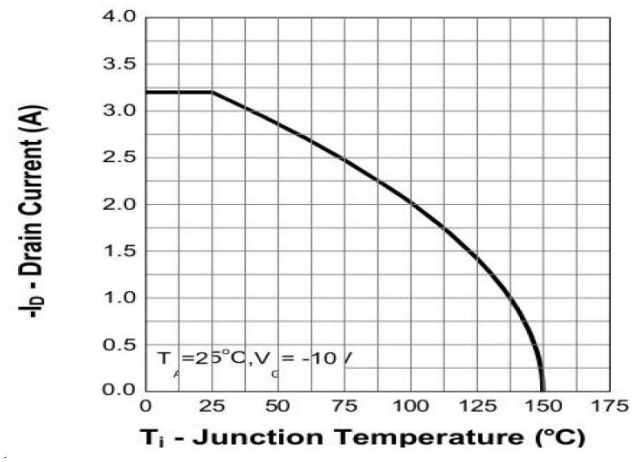


Figure 10: Power De-rating

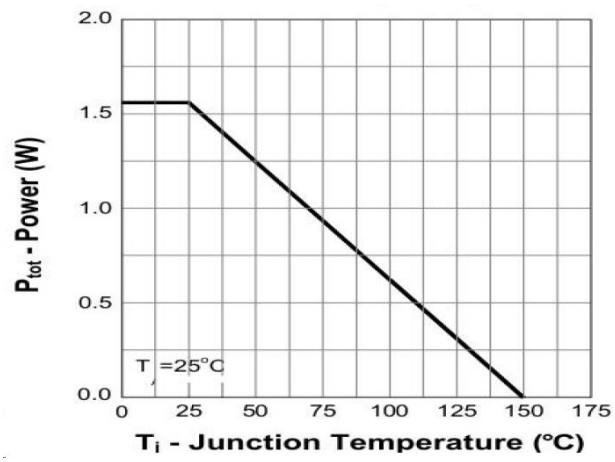


Figure 11: Maximum Safe Operating Area

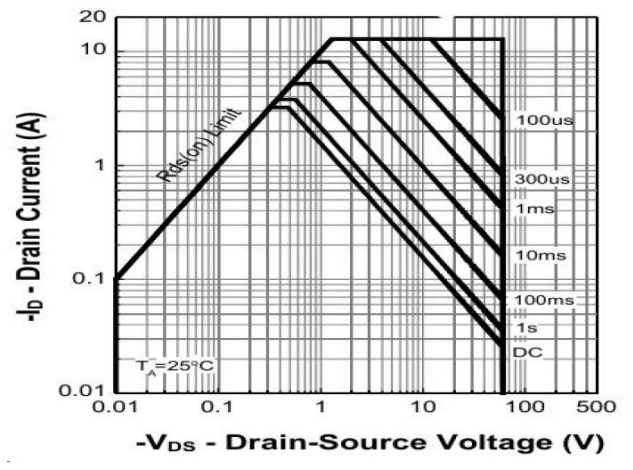
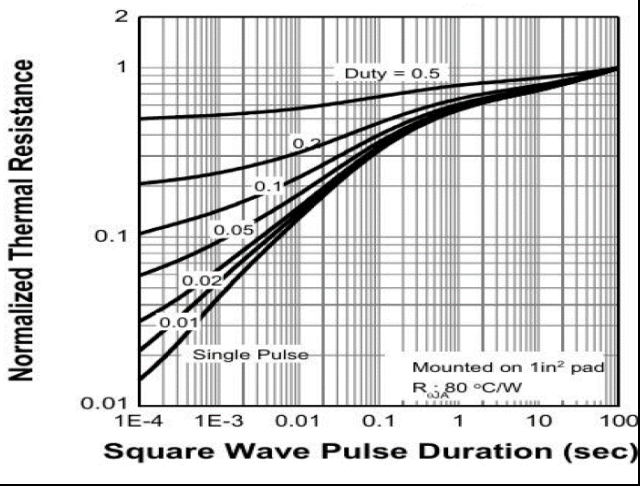


Figure 12: Normalized Maximum Transient Thermal Impedance



Test Circuit

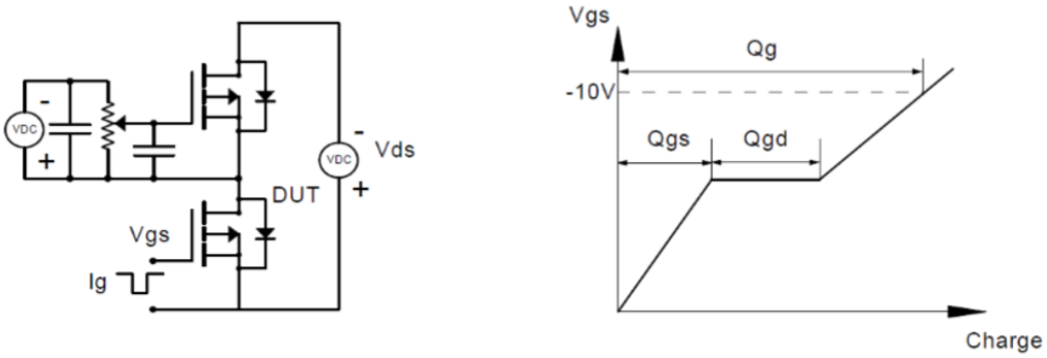


Figure1: Gate Charge Test Circuit & Waveforms

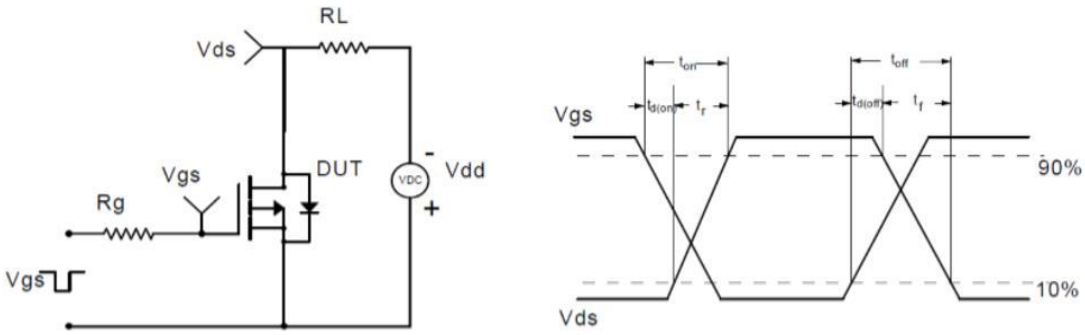


Figure2: Resistive Switching Test Circuit & Waveforms

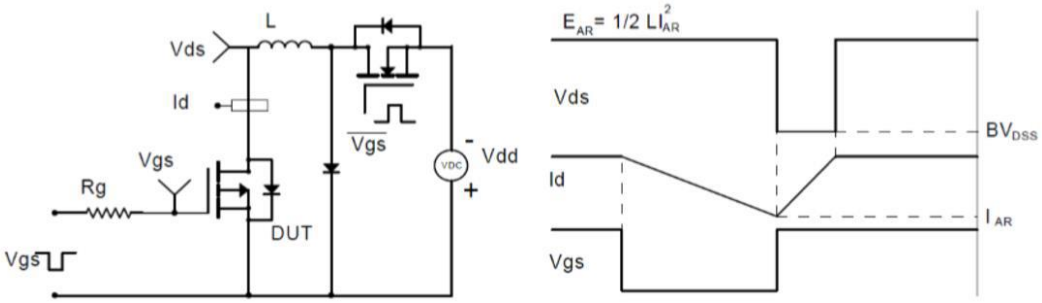


Figure3: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

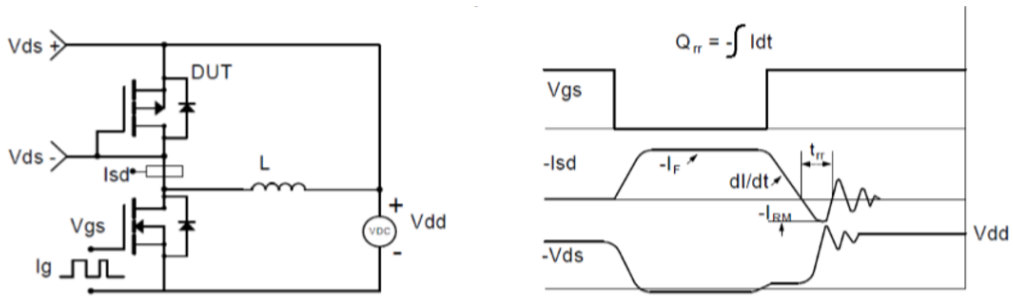
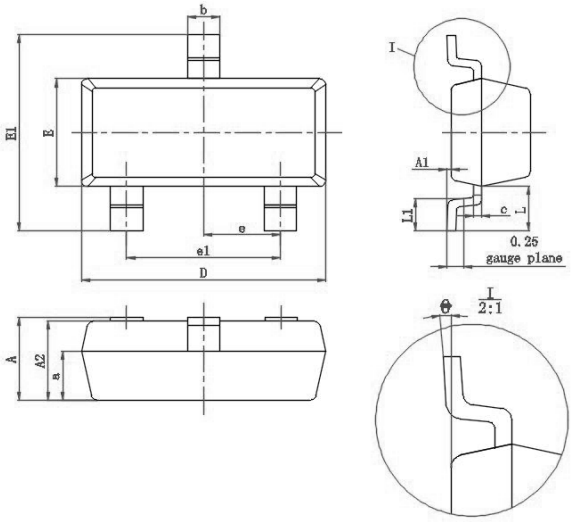


Figure4: Diode Recovery Test Circuit & Waveforms

SOT-23 Package Information

Package Outline Dimensions (Units: mm)



符号	尺寸		符号	尺寸		符号	尺寸	
	Min	Max		Min	Max		Min	Max
A	0.9	1.15	E	1.2	1.4	c	0.08	0.15
A1	0	0.1	E1	2.25	2.55	L	(0.55)	
A2	0.9	1.05	e	(0.95)		L1	0.3	0.5
a	(0.6)		e1	1.8	2.0	θ	0°	8°
D	2.8	3.0	b	0.3	0.5			