MOSFET Silicon N-Channel MOS

1. Applications

Soft Switching Boost PFC switch, Half bridge or Asymmetric half bridge or Series resonance half bridge and full bridge topologies.
Such as phase-shift-bridge(ZVS),LLC Application-Server Power, Telecom Power, EV Charging, Solar inverter.

2. Features

Low drain-source on-resistance: RDS(ON) = 0.060Ω (typ.)
Easy to control Gate switching
Enhancement mode: Vth = 3 to 5 V

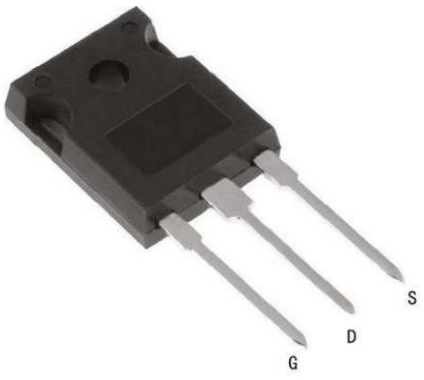
Table 1 Key Performance Parameters

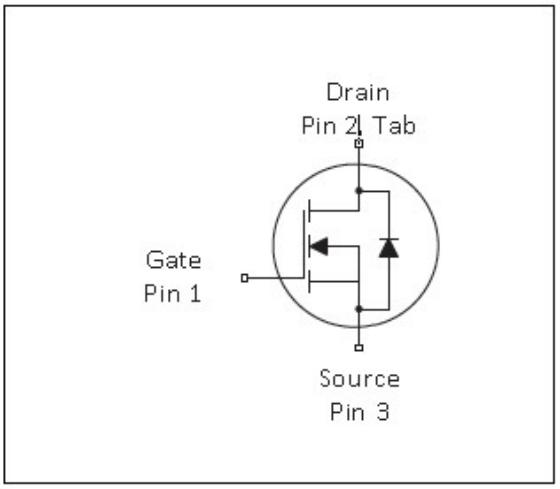
Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	700	V
$R_{DS(on),max}$	72	mΩ
$Q_{g,typ}$	93.87	nC
$I_{D,pulse}$	162	A
Body diode dv/dt	50	V/ns

3. Packaging and Internal Circuit

Part Name	Package	Marking
ASW65R072EFDA	TO247	ASW65R072EFDA

TO247





1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1)]	I_D		-	54	A	T_C=25°C
Pulsed drain current[2)]	$I_{D,pulse}$	-	-	162	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	793	mJ	Tc=25°C, V_{DD}=50V, L=10mH, RG=25Ω
MOSFET dv/dt ruggedness	dv/dt	-	-	36	V/ns	V_{DS}=0...400V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	172	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	150	°C	
Operating junction temperature	T_j	-55	-	150	°C	
Reverse diode dv/dt[3)]	dv/dt	-	-	50	V/s	V_R=400V, I_F=25 A, di_F/dt=100A/µs; see table 8

[1)] Limited by $T_{j,max}$. Maximum Duty Cycle D = 0.50
[2)] Pulse width t_p limited by $T_{j,max}$
[3)] Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.73	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint

3 Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	655	-	-	V	V_{GS}=0V, I_D=250uA
Gate threshold voltage	$V_{(GS)th}$	3		5	V	V_{DS}=V_{GS}, I_D=250uA
Zero gate voltage drain current	I_{DSS}	-	-	2	uA	V_{DS}=650V, V_{GS}=0V, T_j=25°C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=30V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	-	0.060	0.072	Ω	V_{GS}=10V, I_D=14A, T_j=25°C
Gate resistance	R_G	-	1	-	Ω	f=1MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	4528	-	pF	V_{GS}=0V, V_{DS}=50V, f=1MHz
Output capacitance	C_{oss}	-	414.3	-	pF	V_{GS}=0V, V_{DS}=50V, f=1MHz
Reverse transfer capacitance	C_{rss}		3.08		pF	V_{GS}=0V, V_{DS}=50V, f=1MHz
Turn-on delay time	$t_{d(on)}$	-	21.6	-	ns	V_{DD}=400V,V_{GS}=13V,I_D=17.1A, R_G=5.3Ω;see table 9
Rise time	t_r	-	10.7	-	ns	V_{DD}=400V,V_{GS}=13V,I_D=17.1A, R_G=5.3Ω;see table 9
Turn-off delay time	$t_{d(off)}$	-	86.6	-	ns	V_{DD}=400V,V_{GS}=13V,I_D=17.1A, R_G=5.3Ω;see table 9
Fall time	t_f	-	8.6	-	ns	V_{DD}=400V,V_{GS}=13V,I_D=17.1A, R_G=5.3Ω;see table 9

Table 6 Gate charge characteristics

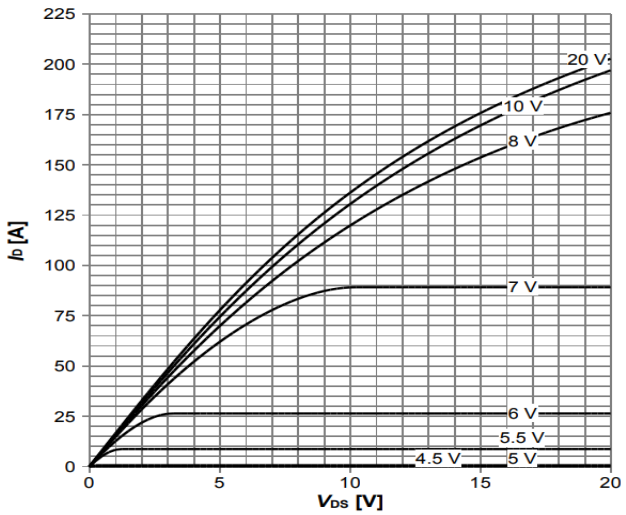
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	24.79	-	nC	V_{DD}=400V, I_D=17.1A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	34.94	-	nC	V_{DD}=400V, I_D=17.1A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	93.87	-	nC	V_{DD}=400V, I_D=17.1A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	6.01	-	V	V_{DD}=400V, I_D=17.1A, V_{GS}=0 to 10V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.64	-	V	V_{GS}=0V, I_F=1A, T_j=25°C
Reverse recovery time	t_{rr}	-	224.4	-	ns	V_R=400V, I_F=33A, di_F/dt=60A/µs; see table 8
Reverse recovery charge	Q_{rr}	-	1.09	-	uC	V_R=400V, I_F=33A, di_F/dt=60A/µs; see table 8
Peak reverse recovery current	I_{rrm}	-	8.89	-	A	V_R=400V, I_F=33A, di_F/dt=60A/µs; see table 8

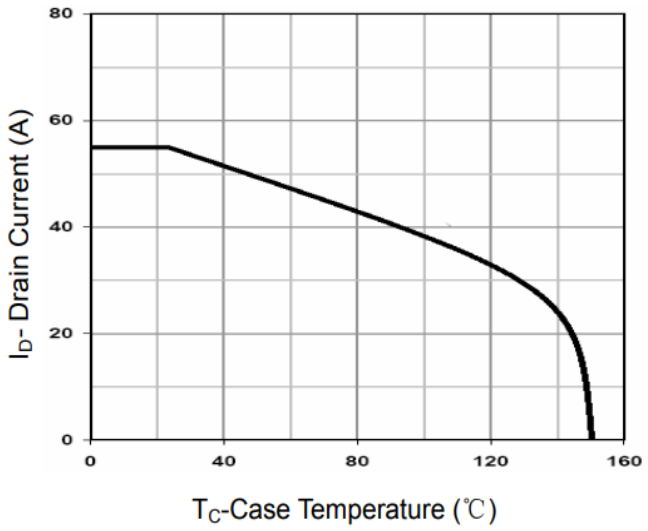
4 Electrical characteristics diagram

Diagram 1: Typ. Output characteristics



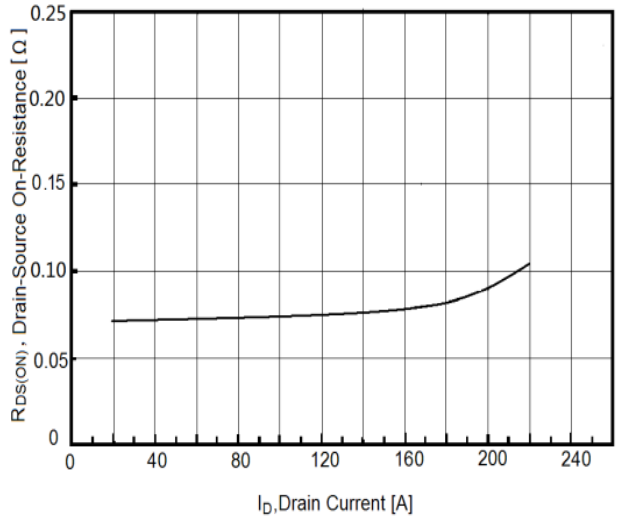
I_D=f(V_{DS});T_j=25 °C; parameter: V_{GS}

Diagram 2: Typ. Drain Current De-rating



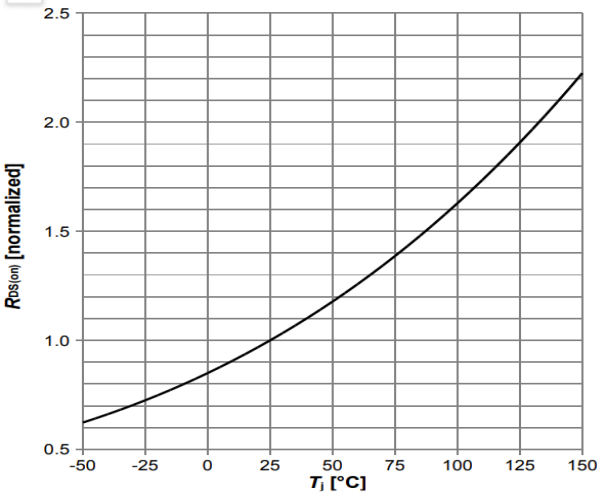
Id=f(T_C);

Diagram 3: Typ. Rdson vs. Drain Current



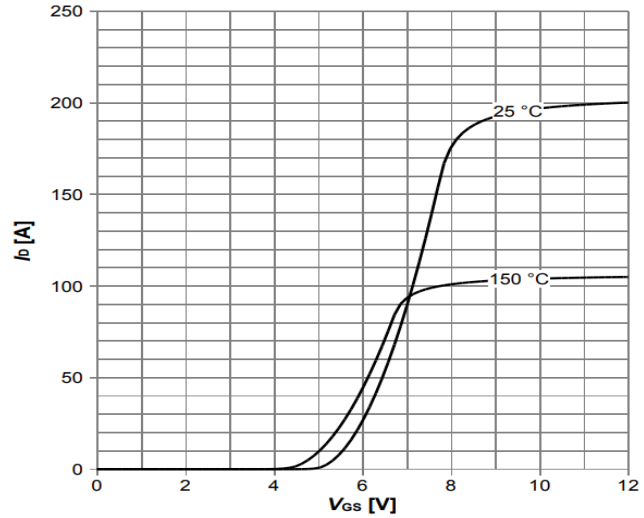
$R_{ds(on)}$=f(*Id*);Vgs=10V

Diagram 4: Typ. Rdson – Junction Temperature



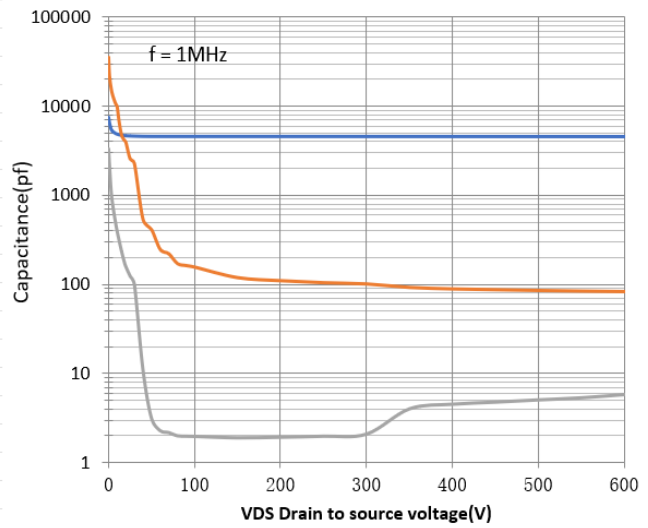
$R_{ds(on)}$=f(T_j);Vgs=10V/I_D=14A

Diagram 5: Typ. transfer characteristics



I_D=f(V_{DS});T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. Capacitance vs. Vds



C=f(V_{DS});V_{GS}=0V; *f*=1MHz

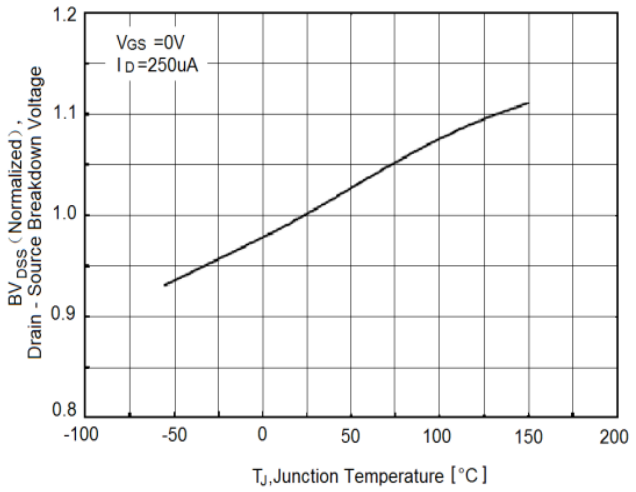
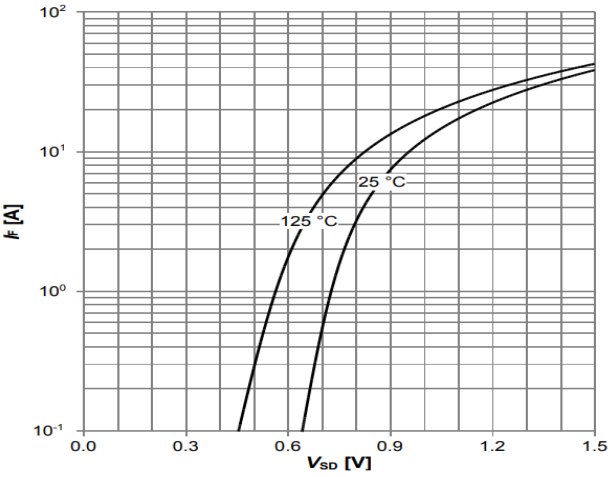
Diagram 7: Typ. BVDSS voltage vs. Temperature	Diagram 8: Typ. Source-Drain Diode Forward
	
V_{GS}=f(T_j);I_D=250uA	I_{SD}=f(V_{DS}); T_C=25 °C;

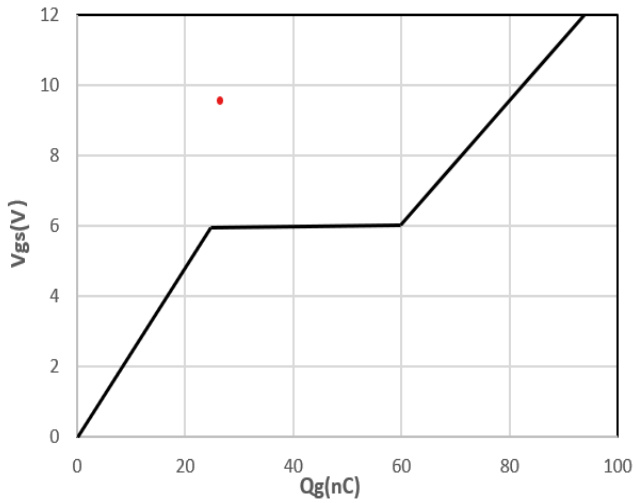
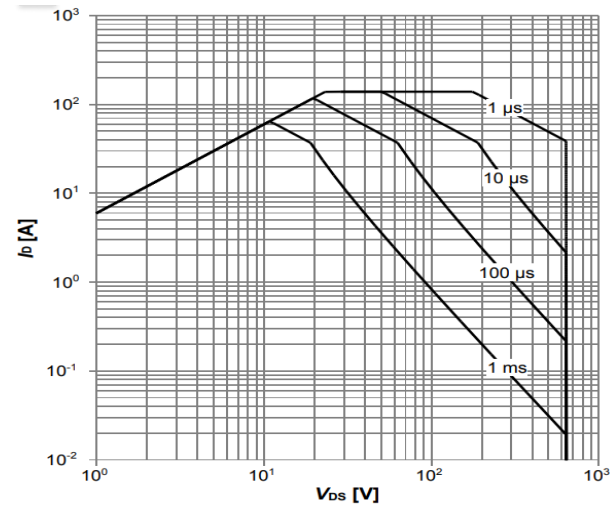
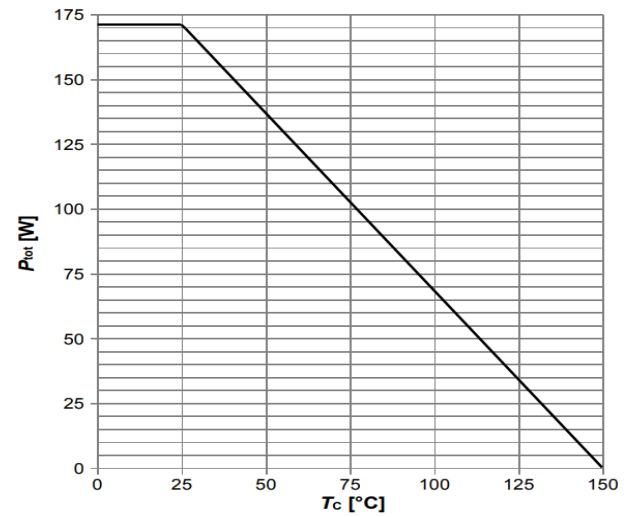
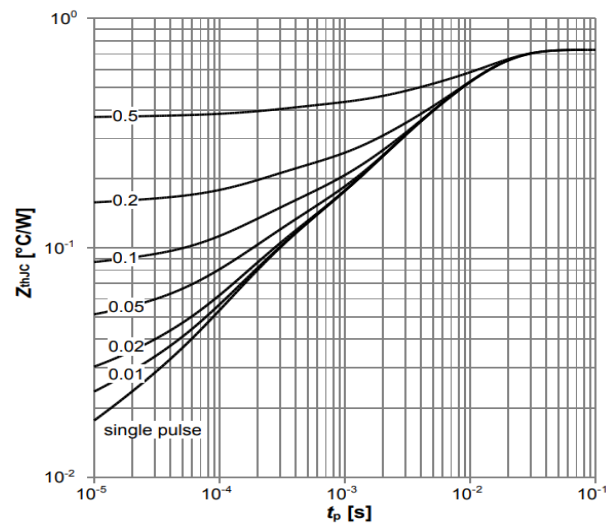
Diagram 9: Typ. Gate charge	Diagram 10: Typ. Maximum Safe Operating Area
	
V_{GS}=f(Q_{gate});I_D=17.1A pulsed; parameter: V_{DD}	I_D=f(V_{DS}); T_C=25 °C; V_{GS}> 7V; D=0; parameter tp

Diagram 11: Typ. Power Dissipation	Diagram 12: Normalized Transient Impedance
	
P_{tot}=f(T_C);	

5 Test Circuits

Table 8 Diode characteristics

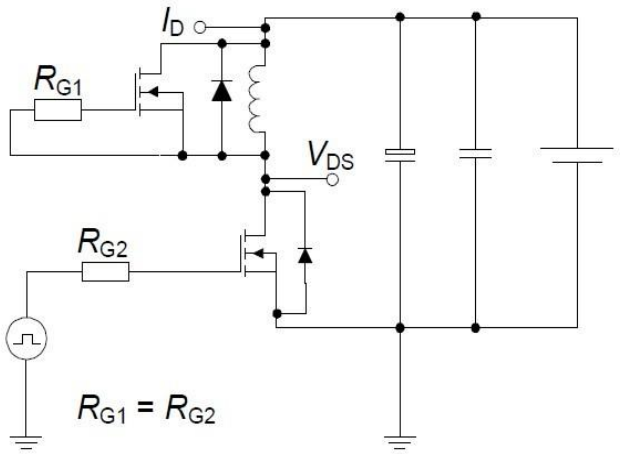
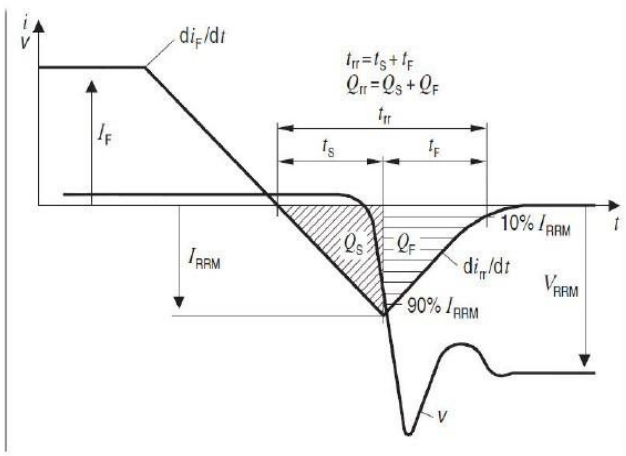
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times

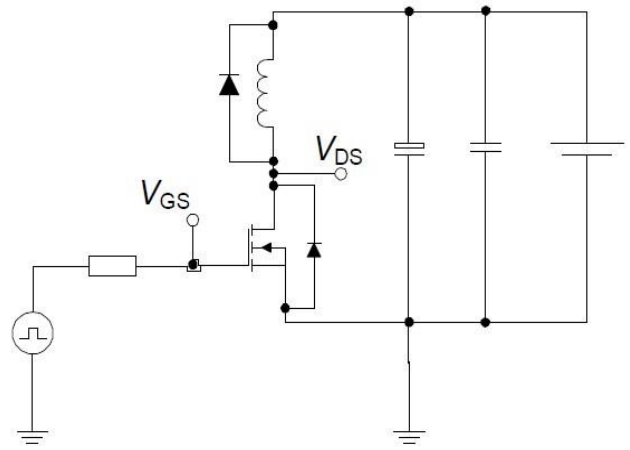
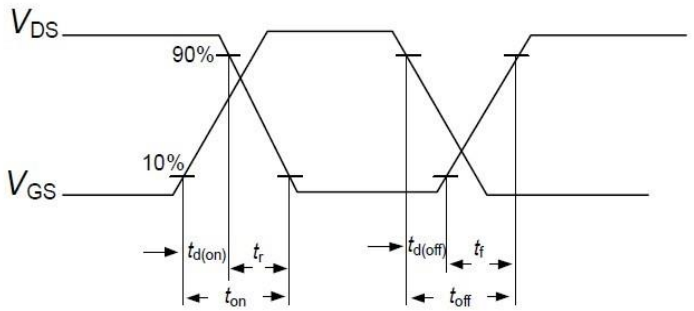
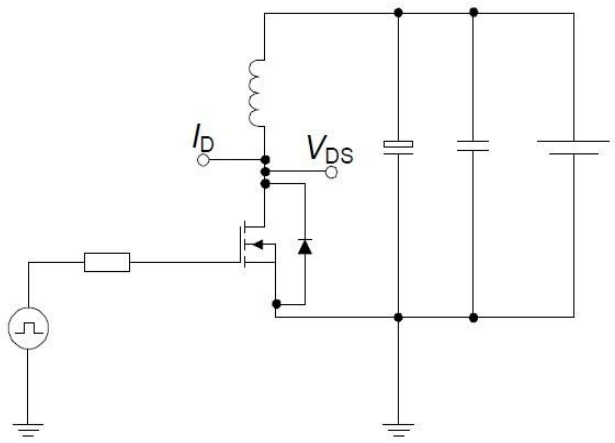
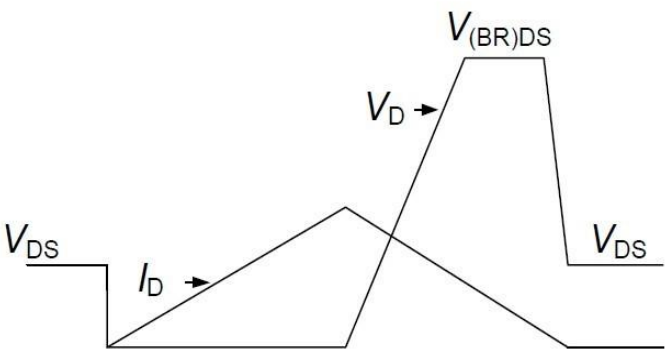
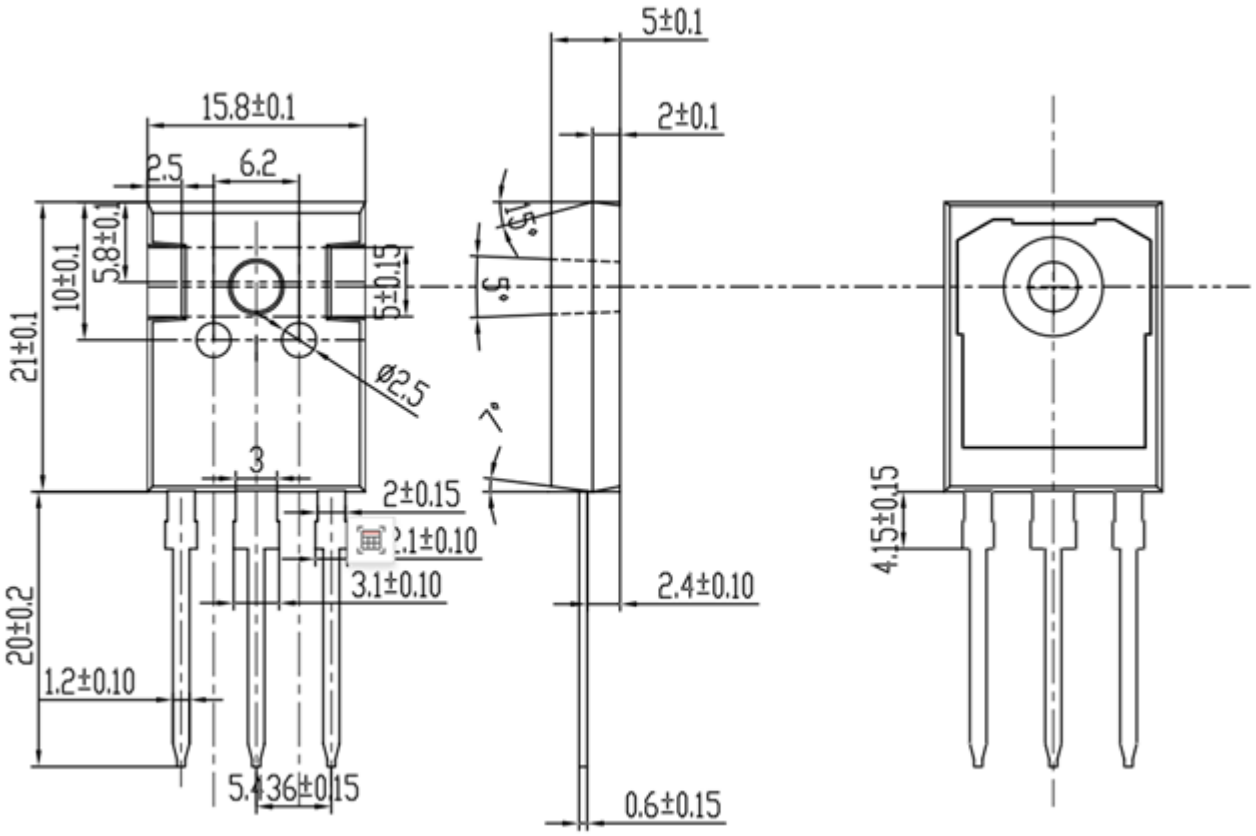
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package Outlines



Figure： Outline PG-TO247(HT)

Revision History

Revision	Date	Subjects (major changes since last revision)
1.0	2023-07-25	Preliminary version