

## 650V N-Channel Silicon Carbide Power MOSFET

### 1. Applications

Asymmetrical Bridge  
Converter  
Inverter  
Single Switch Forward  
Flyback



### 2. Features

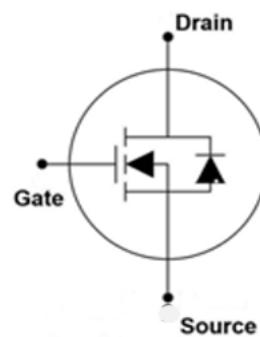
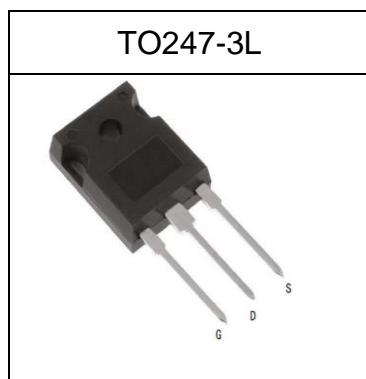
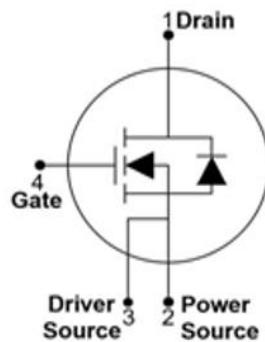
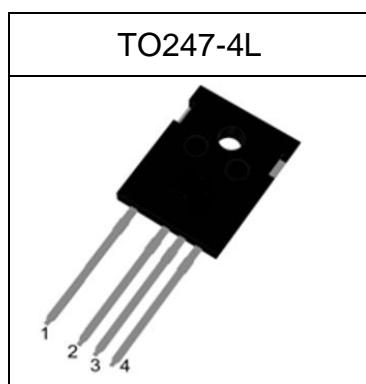
Low drain-source on-resistance:  $R_{DS(ON)} = 30\text{m}\Omega$  (typ.)  
Easy to control Gate switching  
Enhancement mode:  $V_{th} = 2.2$  to  $5\text{V}$

**Table 1 Key Performance Parameters**

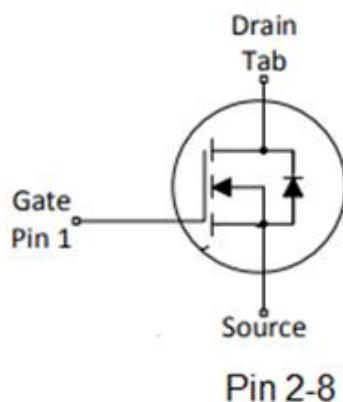
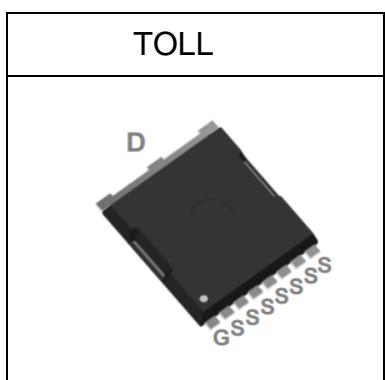
Parameter	Value	Unit
$V_{DS}$ @ $T_{j,max}$	650	V
$R_{DS(on),max}$	42	$\text{m}\Omega$
$Q_{g,typ}$	97.6	nC
$I_{D,pulse}$	250	A

### 3. Packaging and Internal Circuit

Part Name	Package	Marking
ADQ065N028AH	TO-247-4L	ADQ065N028AH
ADW065N028AH	TO-247-3L	ADW065N028AH
ADR065N028AH	TOLL	ADR065N028AH



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## 1 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	80	A	TC=25°C
		-	-	58	A	TC=100°C
Avalanche energy, single pulse	$E_{AS}$	-	-	605	mJ	Tc=25°C, VDD=50V, L=10mH, RG=25Ω
Gate source voltage (dynamic)	$V_{GS}$	-5	-	20	V	Absolute maximum values
Gate source voltage (static)	$V_{GS}$	-4	-	18	V	Recommended operational values
Power dissipation	$P_{tot}$	-	-	294	W	TC=25°C
Storage temperature	$T_{stg}$	-55	-	175	°C	
Operating junction temperature	$T_j$	-55	-	175	°C	
Soldering Temperature	$T_L$			260	°C	
Distance of 1.6mm from case for 10s						
Transconductance	GFS	-	20.9	-	S	VDS=20V IDS=33.5A
			21.6			VDS=20V IDS=33.5A, Tj=175°C

<sup>1)</sup>Limited by  $T_{j,max}$ . Maximum Duty Cycle D = 0.50

<sup>2)</sup>Pulse width  $t_p$  limited by  $T_{j,max}$

<sup>3)</sup>Identical low side and high side switch with identical RG

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## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	0.51	0.7	°C/W	-
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	62	°C/W	device on PCB, minimal footprint

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### 3 Electrical characteristics

at  $T_j=25^\circ\text{C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	650	-	-	V	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=100\mu\text{A}$
Gate threshold voltage	$V_{(\text{GS})\text{th}}$	2.2	2.8	5.0	V	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=5\text{mA}$
Zero gate voltage drain current	$I_{\text{DSS}}$	-	-	100	$\mu\text{A}$	$V_{\text{DS}}=650\text{V}, V_{\text{GS}}=0\text{V}$
Gate-source leakage current	$I_{\text{GSS+}}$	-	-	250	nA	$V_{\text{GS}}=20\text{V}, V_{\text{DS}}=0\text{V}$
Gate-source leakage current	$I_{\text{GSS-}}$	-	-	-100	nA	$V_{\text{GS}}=-5\text{V}, V_{\text{DS}}=0\text{V}$
Drain-source on-state resistance	$R_{\text{DS(on)}}$	-	30	45	$\text{m}\Omega$	$V_{\text{GS}}=18\text{V}, I_{\text{D}}=30\text{A}, T_j=25^\circ\text{C}$
			33			$V_{\text{GS}}=18\text{V}, I_{\text{D}}=30\text{A}, T_j=150^\circ\text{C}$
Gate resistance (Intrinsic)	$R_{\text{G}}$	-	5.1	-	$\Omega$	$f=1\text{MHz}$ , open drain

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{\text{iss}}$	-	2333	-	pF	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=400\text{V}, f=1\text{MHz}$
Output capacitance	$C_{\text{oss}}$	-	226.7	-	pF	
Reverse transfer capacitance	$C_{\text{rss}}$	-	12.9	-	pF	
Turn-on delay time	$t_{\text{d(on)}}$	-	11.5	-	ns	
Rise time	$t_r$	-	17.5	-	ns	
Turn-off delay time	$t_{\text{d(off)}}$	-	32.5	-	ns	
Fall time	$t_f$	-	8.6	-	ns	
Turn-on Switching Energy	$E_{\text{on}}$		71.2		$\mu\text{J}$	
Turn-off Switching Energy	$E_{\text{off}}$		83.9		$\mu\text{J}$	

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{\text{gs}}$	-	28.2	-	$\text{nC}$	$V_{\text{DD}}=400\text{V}, I_{\text{D}}=33.5\text{A}, V_{\text{GS}}=-4/18\text{V}$
Gate to drain charge	$Q_{\text{gd}}$	-	26.1	-	$\text{nC}$	
Gate charge total	$Q_g$	-	97.6	-	$\text{nC}$	

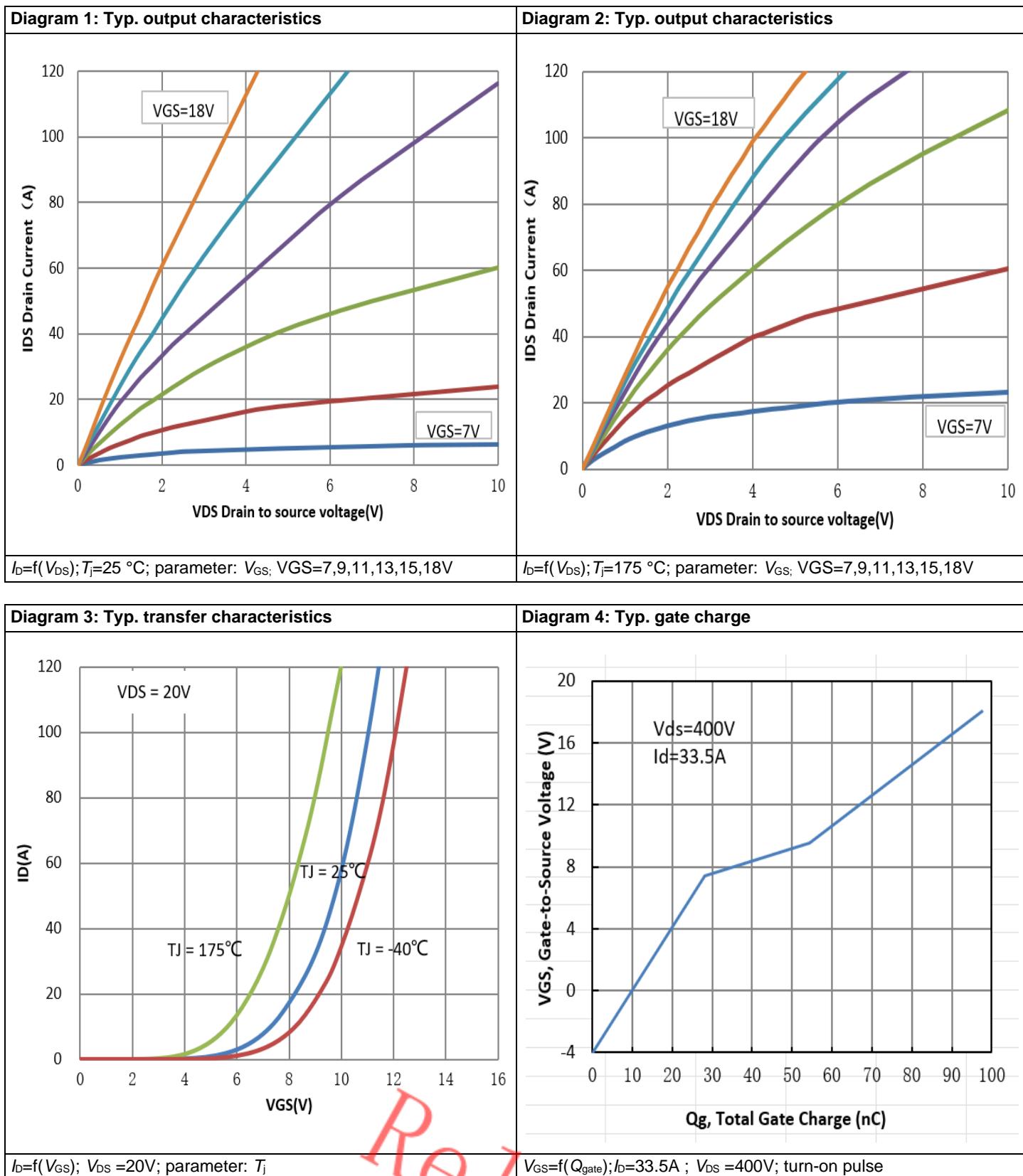
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**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous Source Current	$I_{SD}$	-	-	80	A	
Diode forward voltage	$V_{SD}$	-	3.75	-	V	$I_S=20A, V_{GS}=-4V, T_j=25^\circ C$
Reverse recovery time	$t_{rr}$	-	19.52	-	ns	$V_{GS}=-4V, ISD=33.5A, VR=400\text{ V}$ $dif/dt = 1630\text{A}/\mu\text{s}, TJ=25^\circ C$
Reverse recovery charge	$Q_{rr}$	-	230	-	nC	
Peak reverse recovery current	$I_{rrm}$	-	20.44	-	A	
Reverse recovery time	$t_{rr}$	-	15.04	-	ns	$V_{GS}=-4V, ISD=33.5A, VR=400\text{ V}$ $dif/dt = 5665\text{A}/\mu\text{s}, TJ=25^\circ C$
Reverse recovery charge	$Q_{rr}$	-	400	-	nC	
Peak reverse recovery current	$I_{rrm}$	-	46.46	-	A	

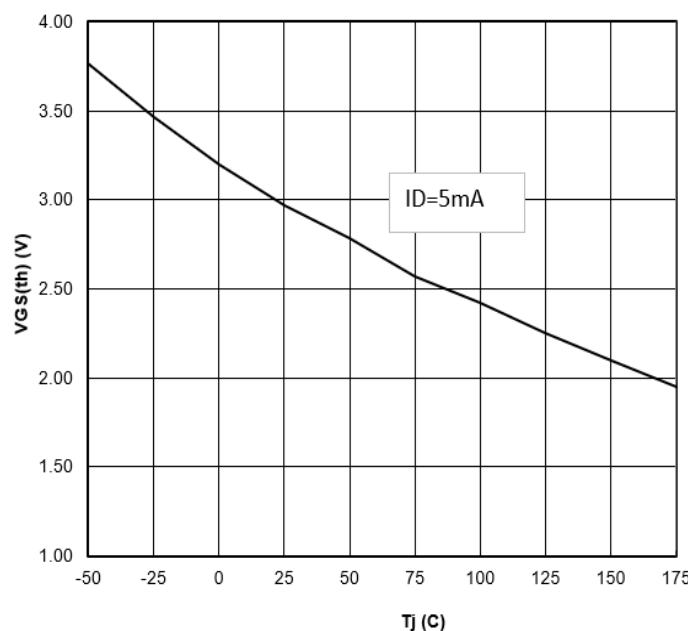
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## 4 Electrical characteristics diagram



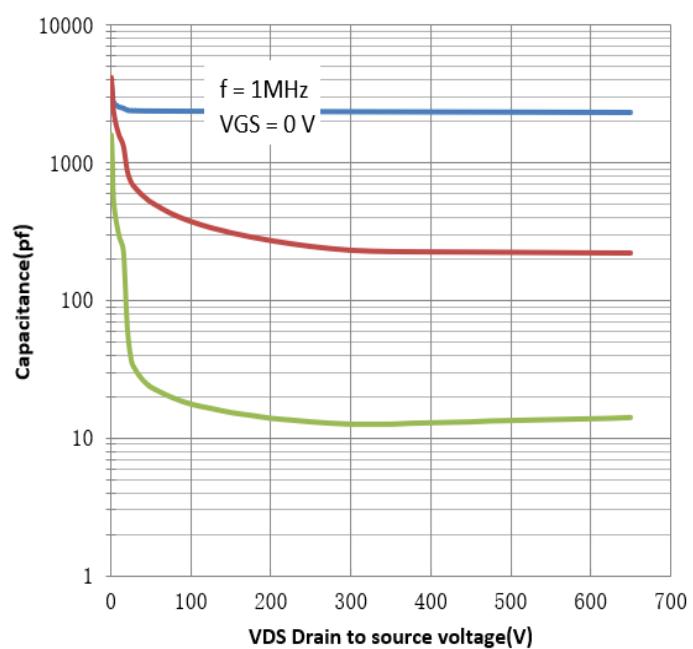
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**Diagram 5: Typical gate-source threshold voltage as a function of junction temperature**



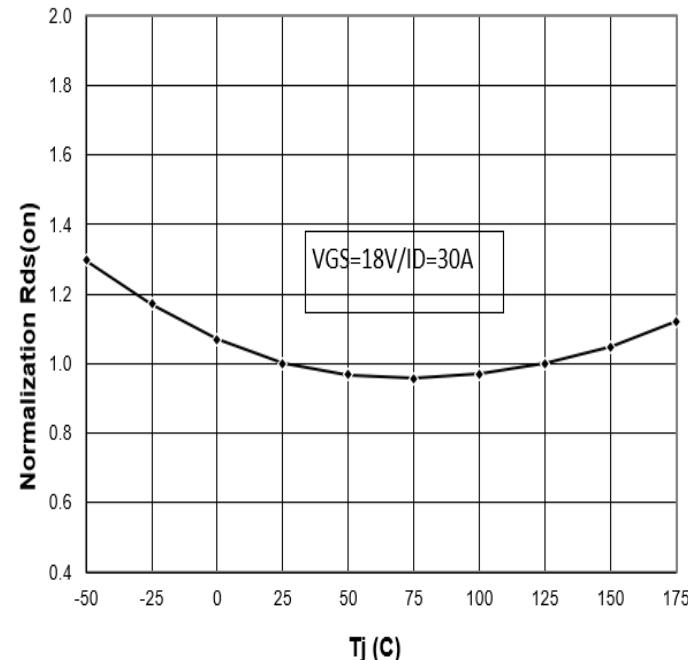
$V_{GS(th)} = f(T_j); I_{DS} = 5\text{mA}; V_{GS} = V_{DS}$

**Diagram 6: Typ. Capacitance as a function of drain-source voltage**



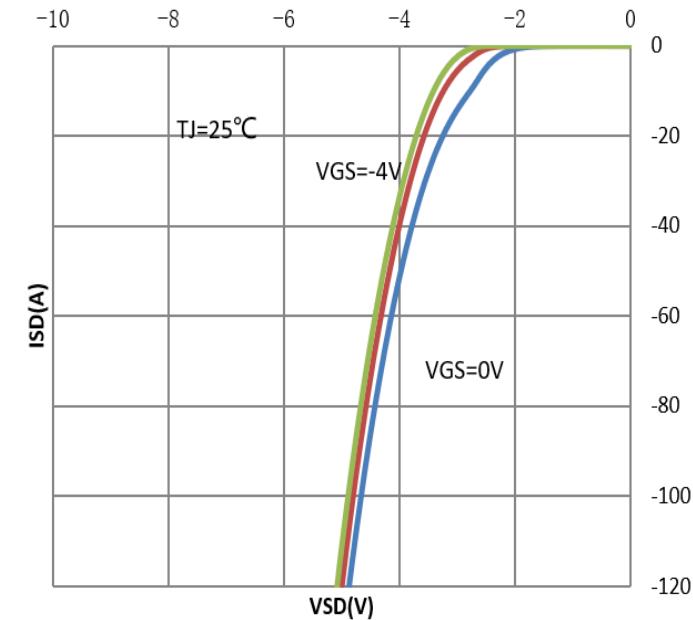
$C = f(V_{DS}); V_{GS} = 0\text{V}; f = 1\text{MHz}$

**Diagram 7: Normalized on-resistance vs. junction temperature**



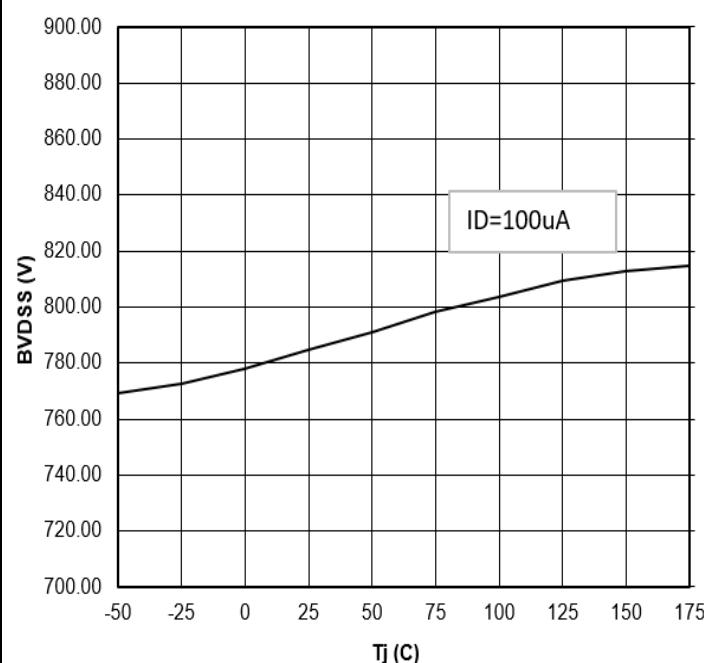
$R_{DS(on)} = f(T_j); I_{DS} = 30\text{A}$

**Diagram 8: Typical body diodes Characteristics at 25°C**



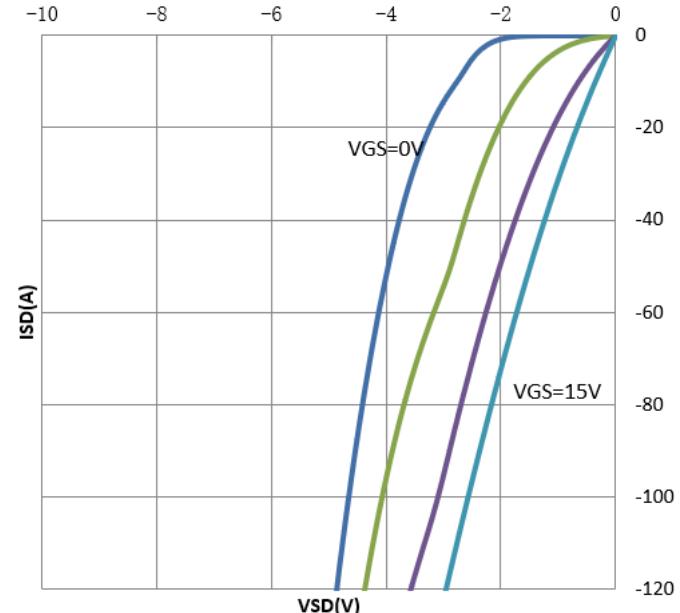
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Diagram 9: BVDSS VS junction temperature



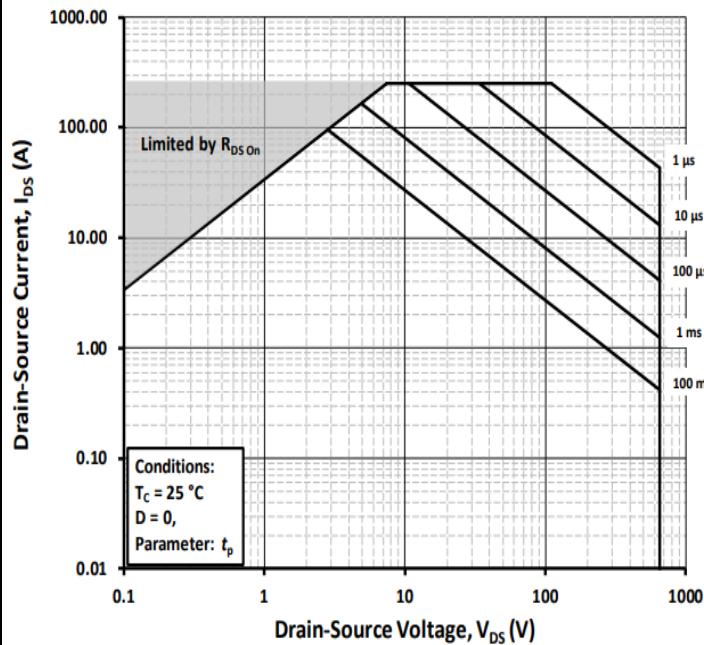
$$Bvdss=f(T_j)$$

Diagram 10: 3rd Quadrant Characteristic at 25 °C



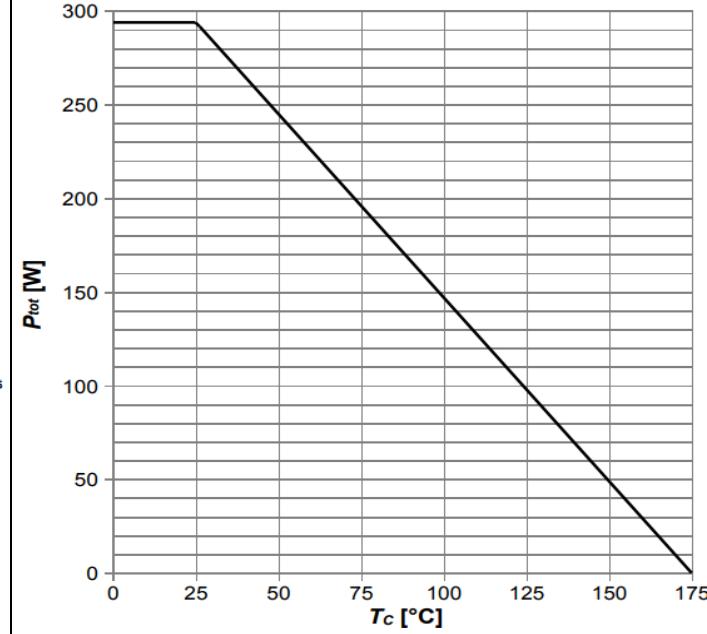
$$I_{SD}=f(V_{SD})$$

Diagram 11: Safe operating area(SOA)



$$V_{GS}=0/18V; T_c=25^\circ C; T_j<175^\circ C$$

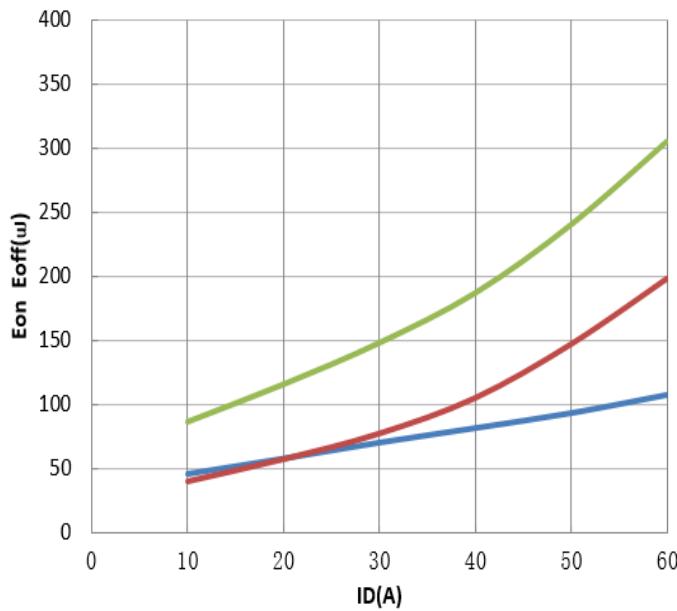
Diagram 12: Power dissipation as a function of case temperature limited by bond wire



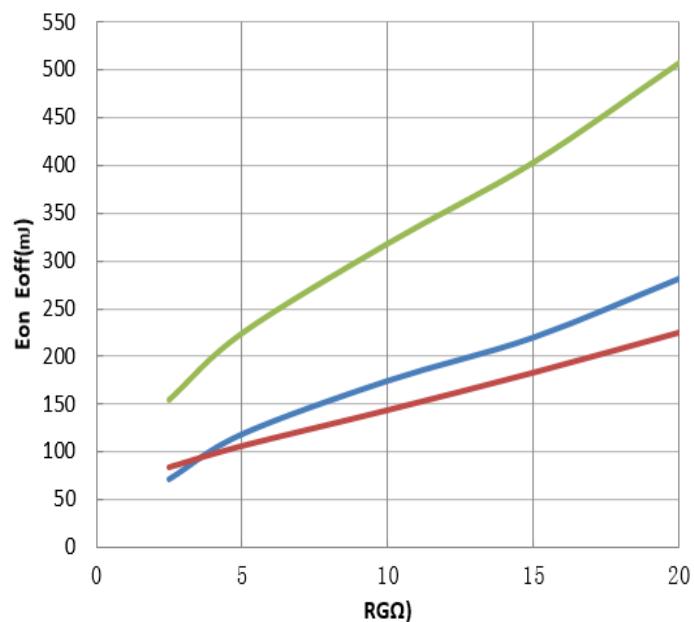
$$P_{tot}=f(T_c)$$

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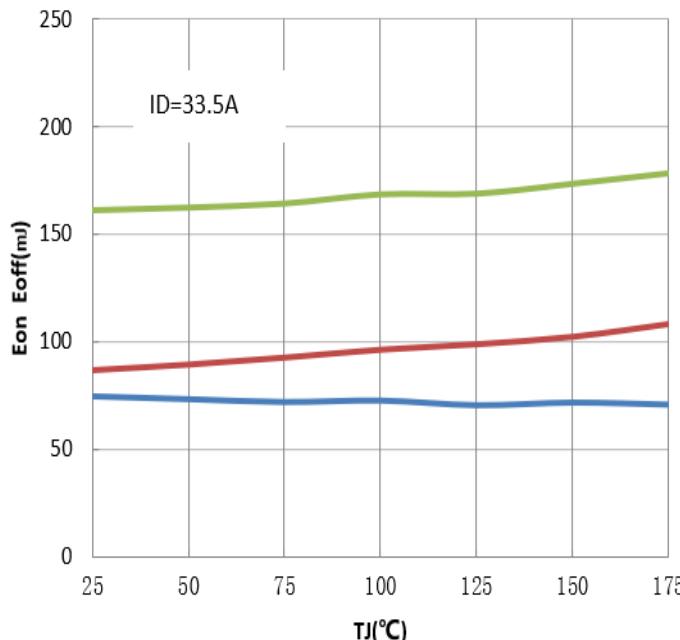
**Diagram 13: Clamped Inductive Switching Energy vs. Drain Current (VDD = 400V)**



**Diagram 14: Clamped Inductive Switching Energy vs. RG(ext)**



**Diagram 15: Clamped Inductive Switching Energy vs. Temperature**



**Diagram 16: Switching Times vs. RG(ext)**

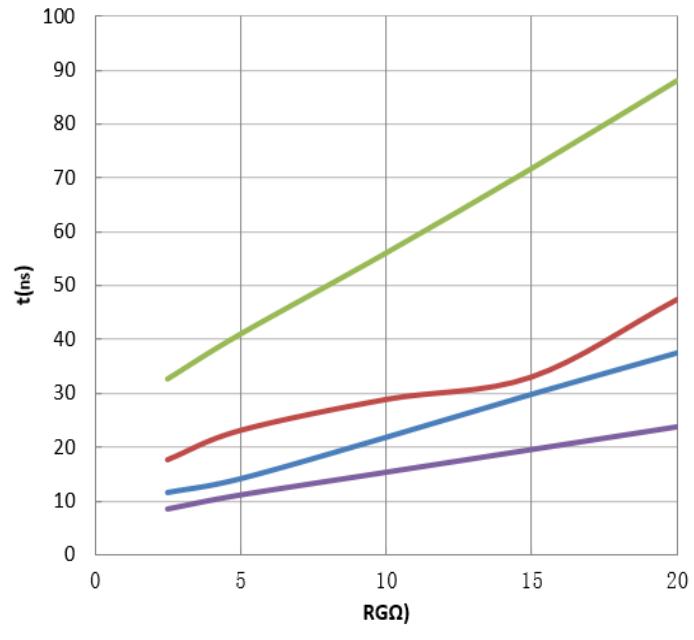


Diagram 17: Continuous Drian Current Derating vs. Case Temperature

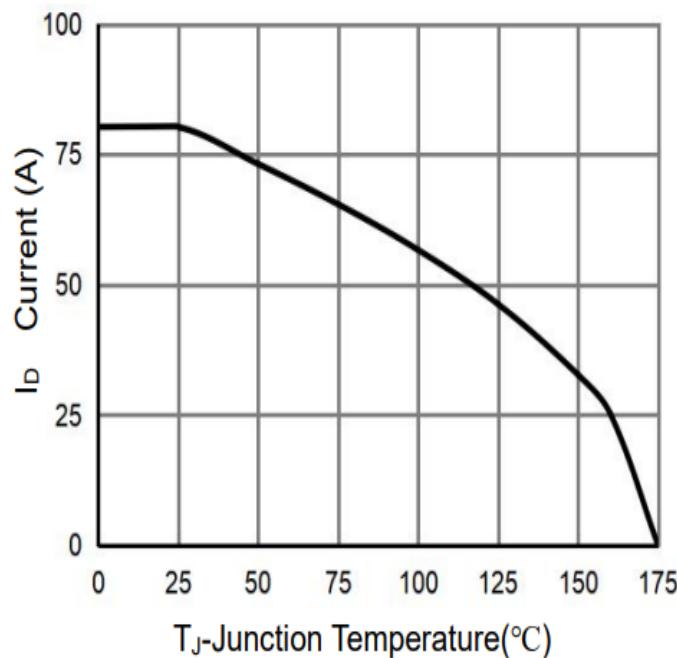


Diagram 18: Output Capacitor Stored Energy

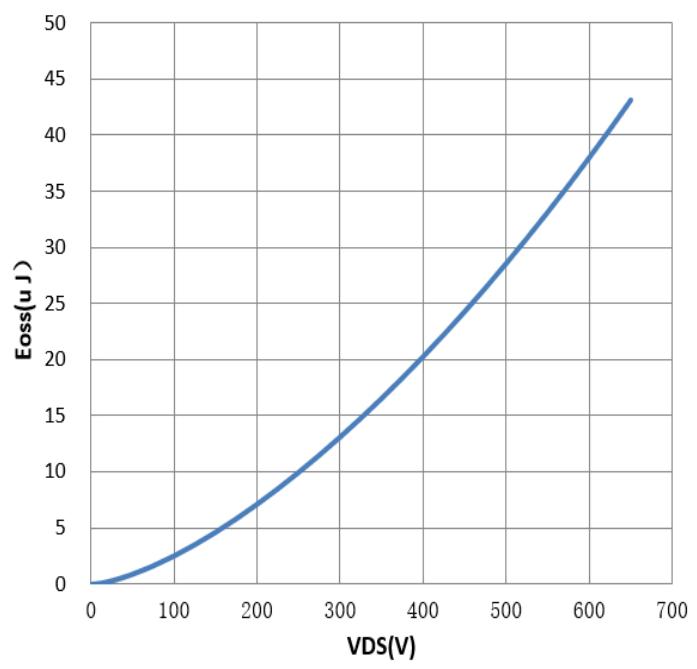
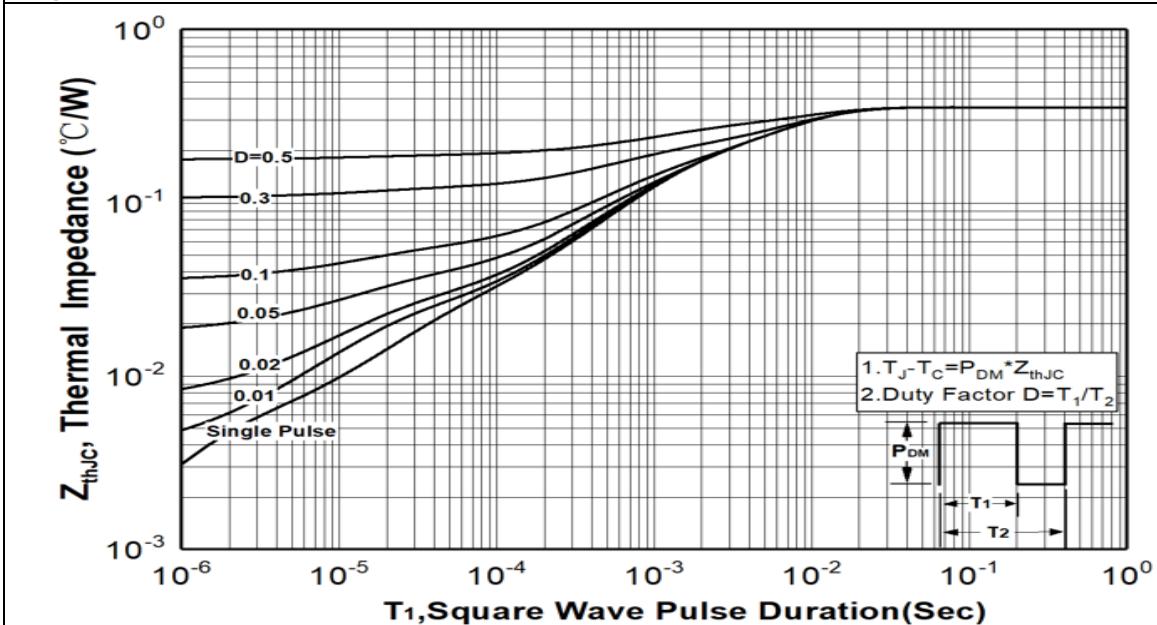
 $I_{DS} = f(T_C)$  $E_{oss} = f(V_{DS})$ 

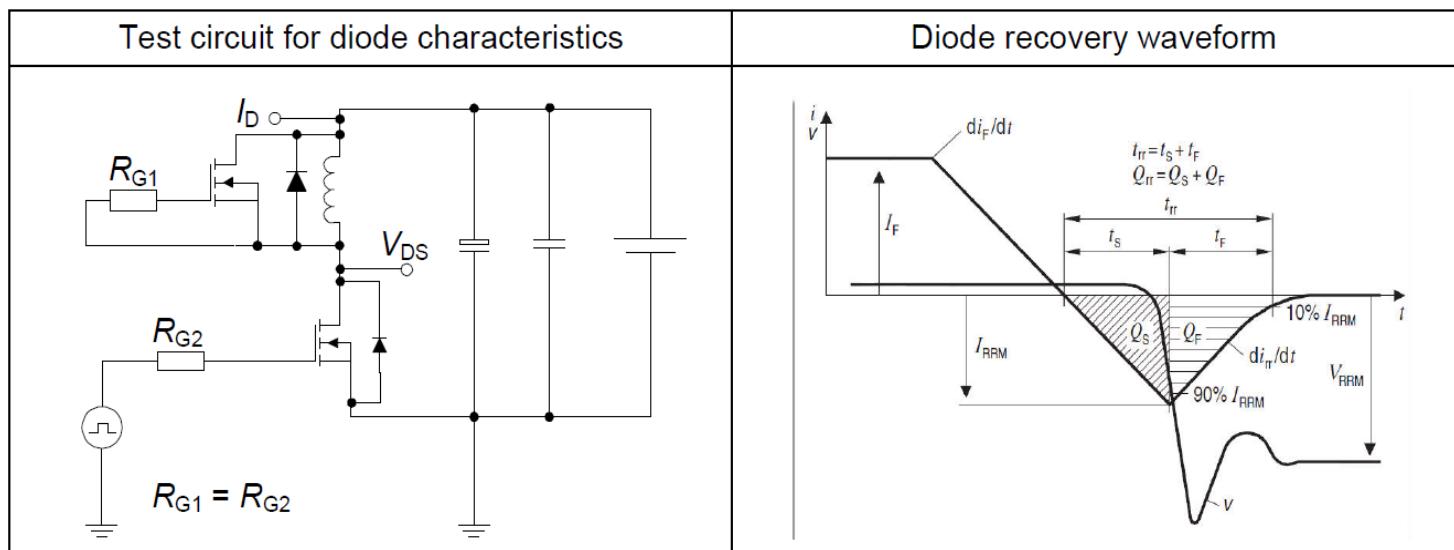
Diagram 19: Max. transient thermal resistance(MOSFET/diodes)

 $Z_{th(j-c,max)} = f(t_p)$ , parameter  $D = t_p/T$ 

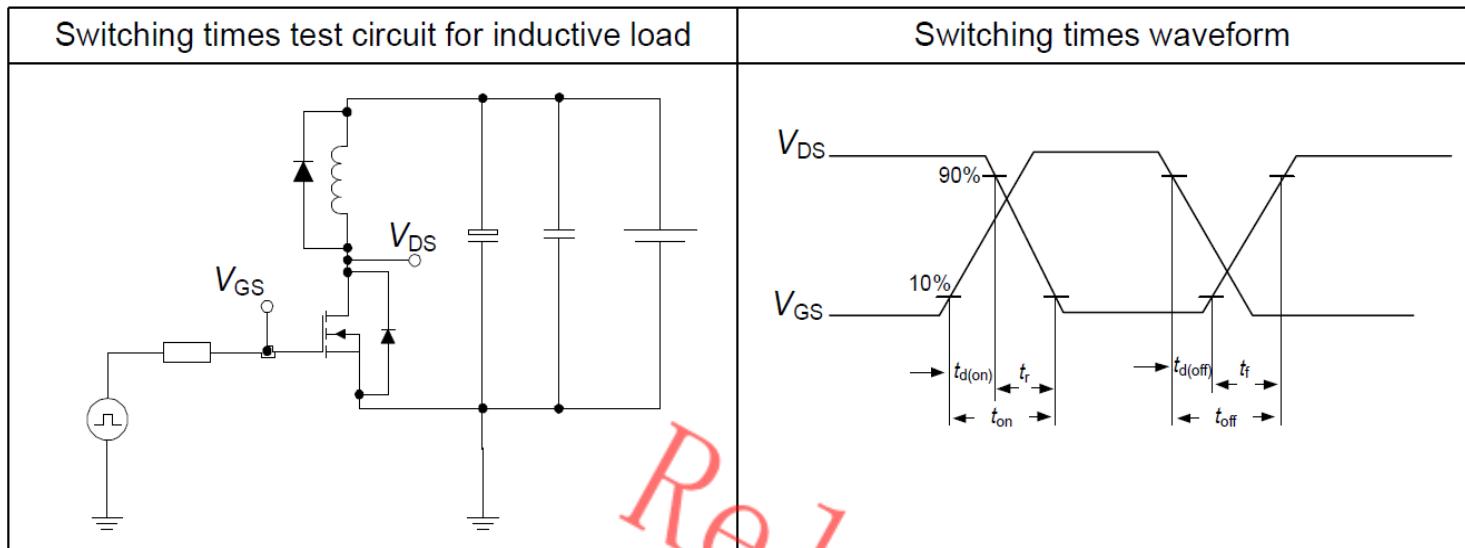
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## 5 Test Circuits

**Table 8 Diode characteristics**

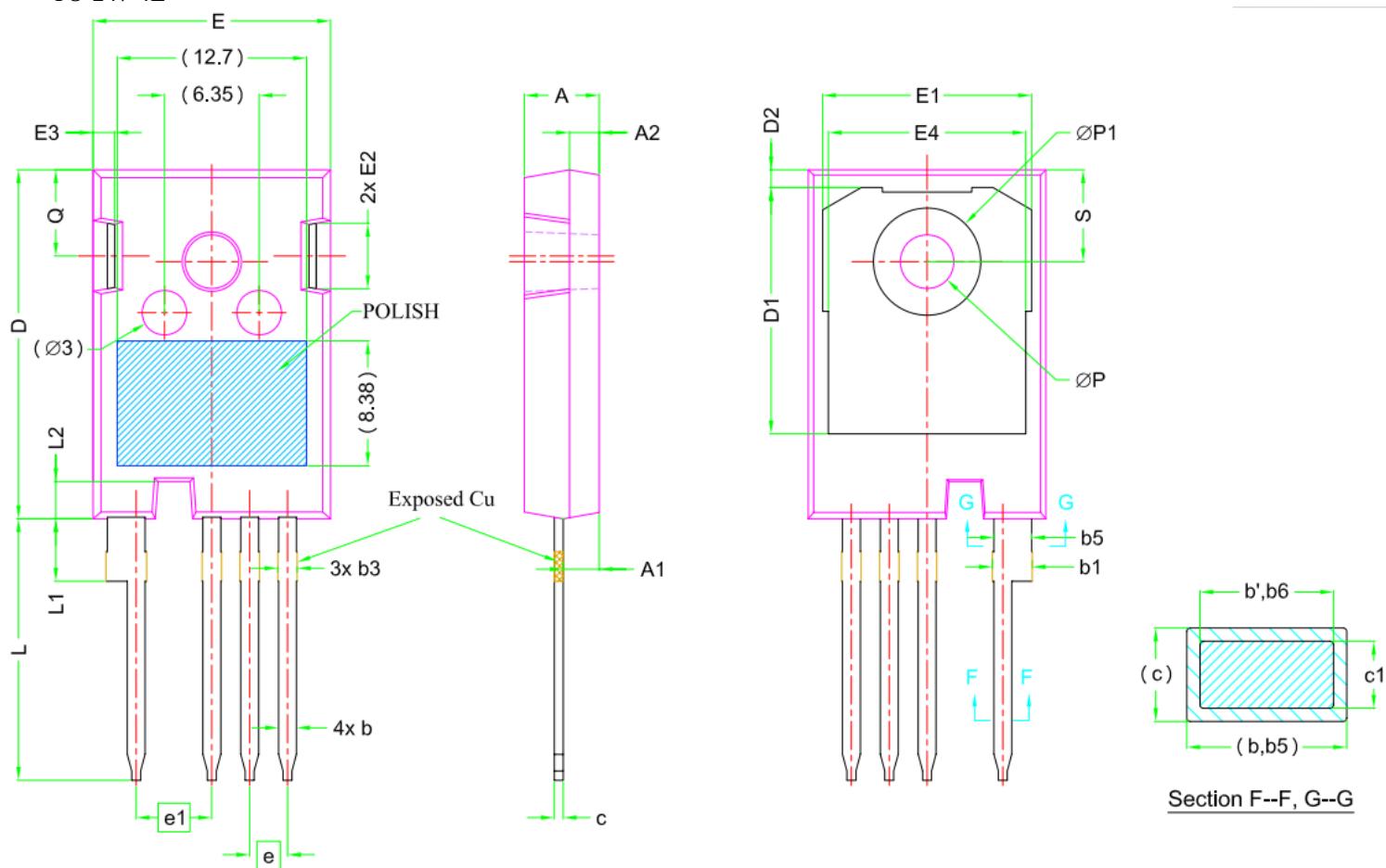


**Table 9 Switching times**



## 6 Package Outlines

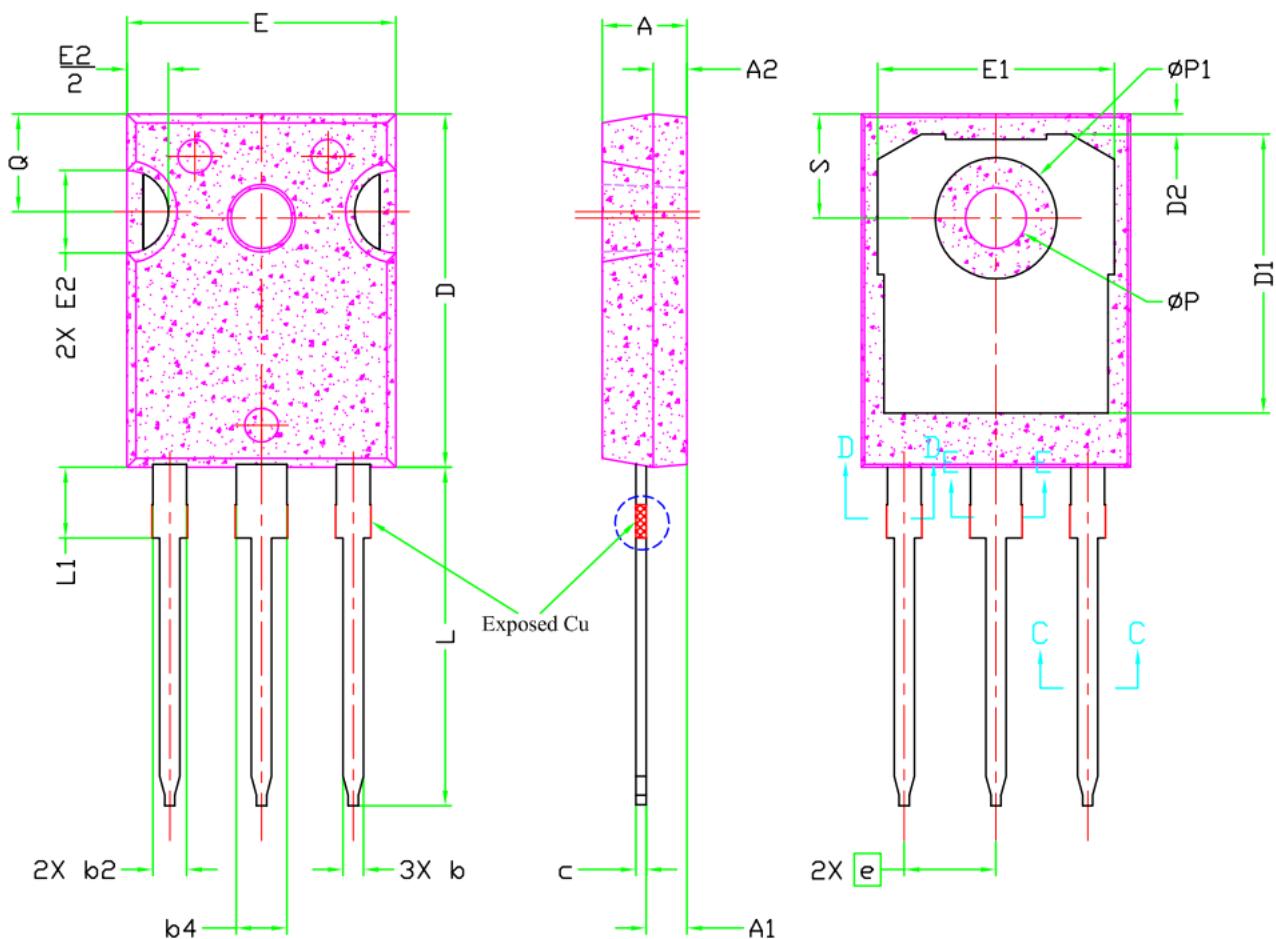
TO-247-4L



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	4.83	5.02	5.21
A1	2.29	2.41	2.54
A2	1.91	2.00	2.16
b'	1.07	1.20	1.28
b	1.07	1.20	1.33
b1	2.39	2.67	2.94
b3	1.07	1.30	1.60
b5	2.39	2.53	2.69
b6	2.39	2.53	2.64
c	0.55	0.60	0.68
c1	0.55	0.60	0.65
D	23.30	23.45	23.60
D1	16.25	16.55	17.65
D2	0.95	1.19	1.25
E	15.75	15.94	16.13
E1	13.10	14.02	14.15
E2	3.68	4.40	5.10
E3	1.00	1.45	1.90
E4	12.38	13.26	13.43
e	2.54 BSC		
e1	5.08 BSC		
L	17.31	17.57	17.82
L1	3.97	4.19	4.37
L2	2.35	2.50	2.65
ØP	3.51	3.61	3.65
ØP1	7.19 REF.		
Q	5.49	5.79	6.00
S	6.04	6.17	6.30

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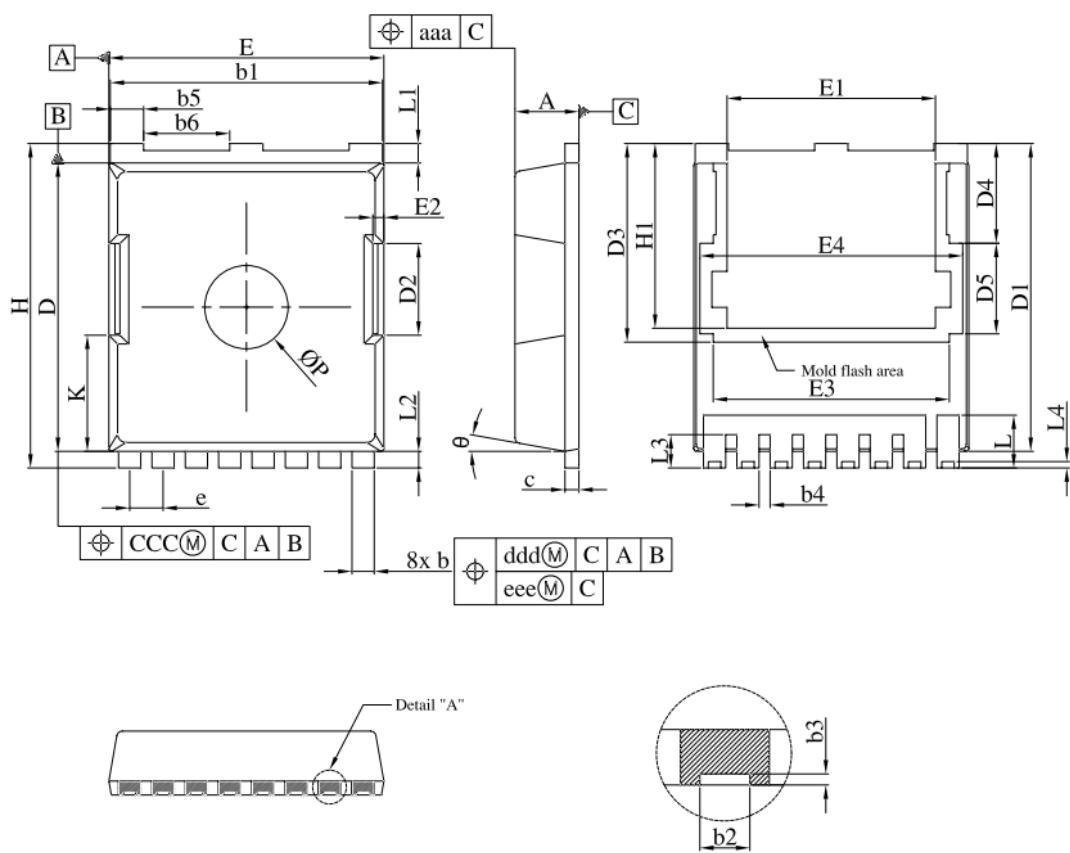
TO-247-3L



SYMBOL	DIMENSIONS			NOTES
	MIN.	NOM.	MAX.	
A	4.83	5.02	5.21	
A1	2.29	2.41	2.55	
A2	1.50	2.00	2.49	
b	1.12	1.20	1.33	
b1	1.12	1.20	1.28	
b2	1.91	2.00	2.39	6
b3	1.91	2.00	2.34	
b4	2.87	3.00	3.22	6, 8
b5	2.87	3.00	3.18	
c	0.55	0.60	0.69	6
c1	0.55	0.60	0.65	
D	20.80	20.95	21.10	4
D1	16.25	16.55	17.65	5
D2	0.51	1.19	1.35	
E	15.75	15.94	16.13	4
E1	13.46	14.02	14.16	5
E2	4.32	4.91	5.49	3
e	5.44BSC			
L	19.81	20.07	20.32	
L1	4.10	4.19	4.40	6
ØP	3.56	3.61	3.65	7
ØP1	7.19REF.			
Q	5.39	5.79	6.20	
S	6.04	6.17	6.30	

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SYMBOL	COMMON		
	MILLIMETER		
	MIN.	NOMINAL	MAX.
A	2.20	2.30	2.40
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.36	0.45	0.55
b3	0.05	0.100	/
b4	0.30	0.40	0.50
b5	1.10	1.20	1.30
b6	3.00	3.10	3.20
c	0.40	0.50	0.60
D	10.28	10.38	10.55
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	7.15		
D4	3.59		
D5	3.26		
e	1.10	1.20	1.30
E	9.80	9.90	10.00
E1	7.40	7.50	7.60
E2	0.30	0.40	0.50
E3	8.50		
E4	9.46		
H	11.50	11.68	11.85
H1	6.55	6.65	6.75
K	4.08	4.18	4.28
L	1.60	1.90	2.10
L1	0.50	0.70	0.90
L2	0.50	0.60	0.70
L3	1.00	1.20	1.30
L4	0.13	0.23	0.33
P	2.85	3.00	3.15
θ	$10^\circ$ REF		
aaa	0.20		
ccc	0.20		
ddd	0.25		
eee	0.20		

Outline PG-TOLL(JQ)

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**Revision History**

Revision	Date	Subjects (major changes since last revision)
1.0	2024-03-12	Preliminary version
1.1	2024-04-22	Added TOLL package

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