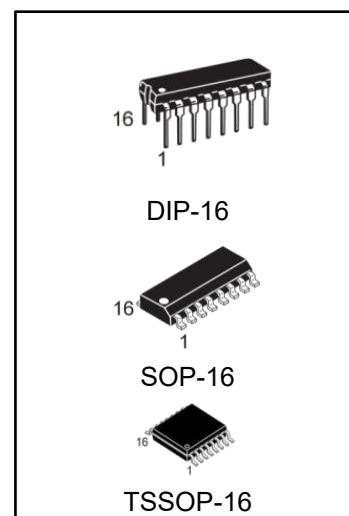


DS34C86 Quad CMOS Differential Line Receiver

Features

- Low power CMOS design
- $\pm 0.2V$ sensitivity over the entire common mode range
- Typical propagation delays: 20 ns
- Typical input hysteresis: 50 mV
- Inputs won't load line when $V_{cc} = 0V$
- Meets the requirements of EIA standard RS-422
- TRI-STATE outputs for connection to system buses



Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
DS34C86PG	DIP-16	DS34C86	TUBE	1000pcs/box
DS34C86DRG	SOP-16	DS34C86	REEL	2500pcs/reel
DS34C86PWRG	TSSOP-16	34C86	REEL	2500pcs/reel

The DS34C86 is a quad differential line receiver designed to meet the RS-422, RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission, while retaining the low power characteristics of CMOS.

The DS34C86 has an input sensitivity of 200 mV over the common mode input voltage range of $\pm 7V$. Hysteresis is provided to improve noise margin and discourage output instability for slowly changing input waveforms.

Separate enable pins allow independent control of receiver pairs. The TRI-STATE® outputs have 6 mA source and sink capability. The DS34C86 is pin compatible with the DS3486.

The diagram shows the internal logic of the 74VHC04M, which consists of six inverters. The pins are numbered 1 through 16. The connections are as follows:

- Pin 16:** V_{CC}
- Pin 15:** Inverter 1 (top right) output (-)
- Pin 14:** Inverter 1 (top right) input (+)
- Pin 13:** Inverter 1 (top right) output (+)
- Pin 12:** Inverter 2 (bottom right) output (-)
- Pin 11:** Inverter 2 (bottom right) input (+)
- Pin 10:** Inverter 2 (bottom right) output (+)
- Pin 9:** Inverter 2 (bottom right) input (-)
- Pin 8:** GND
- Pin 7:** Inverter 3 (bottom left) input (+)
- Pin 6:** Inverter 3 (bottom left) output (+)
- Pin 5:** Inverter 3 (bottom left) output (-)
- Pin 4:** Inverter 4 (top left) output (-)
- Pin 3:** Inverter 4 (top left) input (+)
- Pin 2:** Inverter 4 (top left) output (+)
- Pin 1:** Inverter 4 (top left) input (-)

Labels for inputs and outputs are provided for each inverter:

- INPUTS A:** Pins 1 and 2
- OUTPUT A:** Pin 3
- TRI-STATE CONTROL A/C:** Pin 4
- OUTPUT C:** Pin 5
- INPUTS B:** Pins 14 and 15
- OUTPUT B:** Pin 13
- TRI-STATE CONTROL B/D:** Pin 12
- OUTPUT D:** Pin 11
- INPUTS C:** Pins 6 and 7
- INPUTS D:** Pins 9 and 10

Top View

Absolute Maximum Ratings (Notes 1 & 2)

Condition	Min	Max	UNITS
Supply Voltage (V _{CC})	-	7	V
Common Mode Range (V _{CM})	-14	+14	V
Differential Input Voltage (V _{DIFF})	-14	+14	V
Enable Input Voltage (V _{IN})	-	7	V
Storage Temperature Range (T _{STG})	-65	+150	°C
Lead Temperature (Soldering 10 sec)	-	245	°C
Current Per Output	-25	+25	mA
Operating Conditions			
Supply Voltage (V _{CC})	4.75	5.25	V
Operating Temperature Range (T _A)	-40	+85	°C
Enable Input Rise or Fall Times	-	500	ns

DC Electrical Characteristics

V_{CC} = 5V +5% (unless otherwise specified) (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V _{TH}	Minimum Differential Input Voltage	V _{OUT} = V _{OH} or V _{OL} -7V < V _{CM} < +7V	-0.2		+0.2	V
R _{IN}	Input Resistance	-7V < V _{CM} < +7V (One Input AC GND)		10		kΩ
I _{IN}	Input Current (Under Test)	V _{IN} = +10V, Other Input GND V _{IN} = -10V, Other Input = GND		+1.1 -1.6		mA mA
V _{OH}	Minimum High Level Output Voltage	V _{CC} =Min, V _(DIFF) =+1V I _{OUT} =6.0mA	3.84	4.2		V
V _{OL}	Maximum Low Level Output Voltage	V _{CC} =Max, V _(DIFF) =+1V I _{OUT} =6.0mA				V
V _{IH}	Minimum Enable High Input Level Voltage		2.0			V
V _{IL}	Maximum Enable Low Input Level Voltage				0.8	V
I _{OZ}	Maximum TRI-STATE Output Leakage Current	V _{OUT} =V _{CC} or GND, TRI-STATE Control=VIL		±0.5	±5.0	μA
I _I	Maximum Enable Input Current	V _{IN} =V _{CC} or GND			±1.0	μA
I _{CC}	Quiescent Power Supply Current	V _{CC} =Max, V _(DIFF) =+1V		12		mA
V _{HYST}	Input Hysteresis			50		mV

AC Electrical Characteristics

$V_{CC} = 5V \pm 5\%$ (unless otherwise specified) (Note 3)

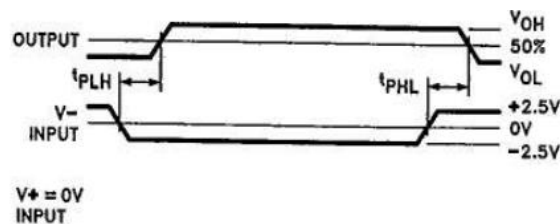
Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{PLH} , t_{PHL}	Propagation Delay Input to Output	$C_L = 50pF$ $V_{DIFF} = 2.5V$		20		ns
t_{PLZ} , t_{PHZ}	Propagation Delay TRI-STATE Control to Output	$C_L = 50pF$ $R_L + 1000\Omega$ $V_{DIFF} = 2.5V$		12		ns
t_{PZL} , t_{PZH}	Propagation Delay TRI-STATE Control to Output	$C_L = 50pF$ $R_L = 1000\Omega$ $V_{DIFF} = 2.5V$		14		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured.

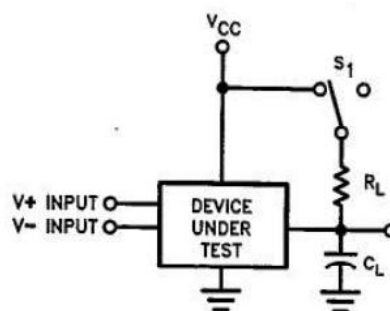
Note 2: Unless otherwise specified, all voltages are referenced to ground.

Note 3: Unless otherwise specified, Min/Max limits apply across the $-40^{\circ}C$ to $+65^{\circ}C$ temperature range. All typicals are given for $V_{CC} = 5V$ and $T_A = 25^{\circ}C$.

Propagation Delay



Test Circuit for TRI-STATE Output Tests

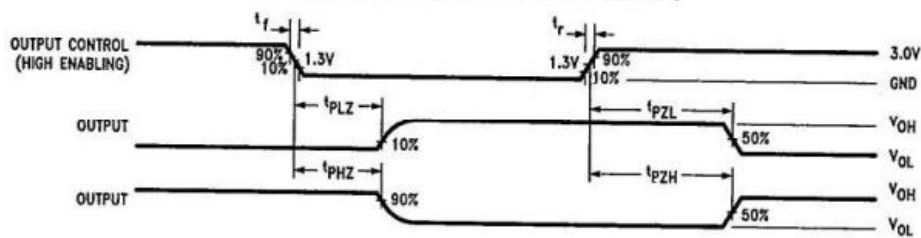


C_L = Includes load and test jig capacitance.

$S1 = V_{CC}$ for t_{PZL} , and t_{PLZ} measurements.

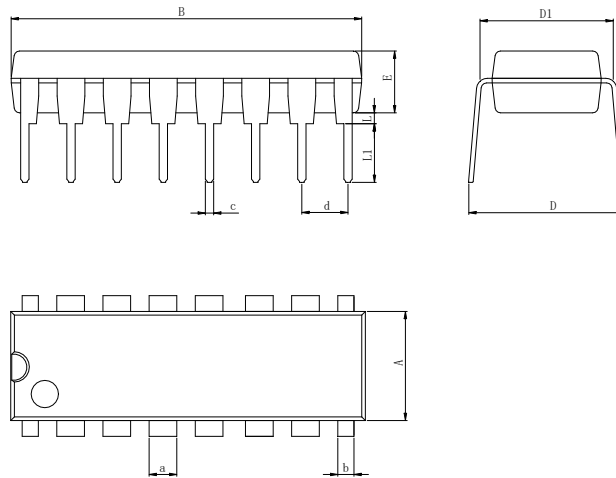
$S1 = GND$ for t_{PZH} , and t_{PHZ} measurements.

TRI-STATE Output Enable and Disable Waveforms



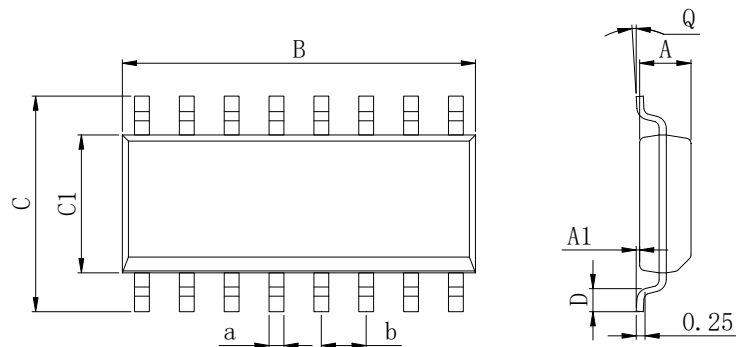
Physical Dimensions

DIP-16



Dimensions In Millimeters(DIP-16)											
Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	18.94	8.10	7.42	3.10	0.50	300	1.50	0.85	0.40	2.54 BSC
Max:	6.68	19.56	10.9	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

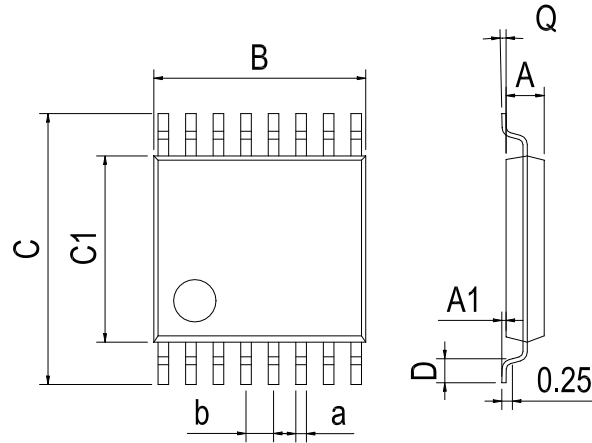
SOP-16



Dimensions In Millimeters(SOP-16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	9.80	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	10.0	6.20	4.00	0.80	8°	0.45	

Physical Dimensions

TSSOP-16



Dimensions In Millimeters(TSSOP-16)

Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.85	0.05	4.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	5.10	6.60	4.50	0.80	8°	0.25	

Revision History

DATE	REVISION	PAGE
2014-6-9	New	1-8
2023-9-15	Modify the package dimension diagram TSSOP-16、Update encapsulation type、Update Lead Temperature、Updated DIP-16 dimension、Add annotation for Maximum Ratings.	1、 3、 5、 6

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