

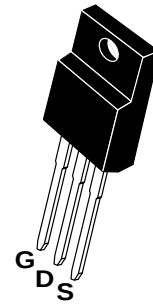


General Description

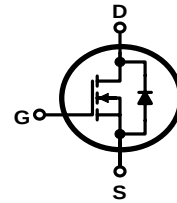
FIR7N60F, the silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-220F, which accords with the RoHS standard.

Features

- I Fast Switching
- I Low ON Resistance($R_{dson} \leq 1.3 \Omega$)
- I Low Gate Charge (Typical Data:24nC)
- I Low Reverse transfer capacitances(Typical:5.5pF)
- I 100% Single Pulse avalanche energy Test



Schematic diagram



- Y = Year
- A = Assembly Location
- WW = Work Week
- VT = Version & Thickness
- FIR7N60F = Specific Device Code

Applications

Power switch circuit of adaptor and charger.

Absolute ($T_c = 25^\circ\text{C}$ unless otherwise specified):

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	600	V
I_D	Continuous Drain Current	7	A
	Continuous Drain Current $T_c = 100^\circ\text{C}$	4.4	A
I_{DM}^{a1}	Pulsed Drain Current	28	A
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}^{a2}	Single Pulse Avalanche Energy	400	mJ
dv/dt^{a3}	Peak Diode Recovery dv/dt	5.0	V/ns
P_D	Power Dissipation	35	W
	Derating Factor above 25°C	0.28	W/ $^\circ\text{C}$
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, -55 to 150	$^\circ\text{C}$
T_L	Maximum Temperature for Soldering	300	$^\circ\text{C}$

**Electrical Characteristics** (Tc= 25℃ unless otherwise specified):

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Unit s
			Min.	Typ.	Max.	
V _{DSS}	Drain to Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	600	--	--	V
ΔBV _{DSS} /ΔT _J	Bvdss Temperature Coefficient	ID=250uA,Reference25℃	--	0.67	--	V/℃
I _{DSS}	Drain to Source Leakage Current	V _{DS} =600V, V _{GS} = 0V, T _a = 25℃	--	--	1	μA
		V _{DS} =480V, V _{GS} = 0V, T _a = 125℃	--	--	100	μA
I _{GSS(F)}	Gate to Source Forward Leakage	V _{GS} =+30V	--	--	100	nA
I _{GSS(R)}	Gate to Source Reverse Leakage	V _{GS} =-30V	--	--	-100	nA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
R _{DS(ON)}	Drain-to-Source On-Resistance	V _{GS} =10V,I _D =3.5A	--	1.0	1.3	Ω
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	2.0	--	4.0	V
Pulse width tp ≤ 300μs, δ ≤ 2%						

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g _{fs}	Forward Transconductance	V _{DS} =15V, I _D =3.5A	--	6.5	--	S
C _{iss}	Input Capacitance	V _{GS} = 0V V _{DS} = 25V f = 1.0MHz	--	1121	--	pF
C _{oss}	Output Capacitance		--	96	--	
C _{rss}	Reverse Transfer Capacitance		--	5.5	--	

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
t _{d(ON)}	Turn-on Delay Time	I _D =7A V _{DD} = 300V R _G =10	--	18	--	ns
t _r	Rise Time		--	22	--	
t _{d(OFF)}	Turn-Off Delay Time		--	40	--	
t _f	Fall Time		--	19	--	
Q _g	Total Gate Charge	I _D =7A V _{DD} =480V V _{GS} = 10V	--	24	--	nC
Q _{gs}	Gate to Source Charge		--	4.8	--	
Q _{gd}	Gate to Drain ("Miller")Charge		--	9.5	--	



Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I _S	Continuous Source Current (Body Diode)		--	--	7	A
I _{SM}	Maximum Pulsed Current (Body Diode)		--	--	28	A
V _{SD}	Diode Forward Voltage	I _S =7A,V _{GS} =0V	--	--	1.5	V
t _{rr}	Reverse Recovery Time	I _S =7A,T _J = 25℃ dI _F /dt=100A/us, V _{GS} =0V	--	363	--	ns
Q _{rr}	Reverse Recovery Charge		--	1920	--	nC
I _{R_{RM}}	Reverse Recovery Current		--	10.6	--	A
Pulse width tp≤300μs, δ ≤2%						

Symbol	Parameter	Typ.	Units
$R_{\theta JC}$	Junction-to-Case	3.57	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient	120	$^\circ C/W$

^{a1}: Repetitive rating; pulse width limited by maximum junction temperature

^{a2}: $L=10mH, I_D=9A, \text{Start } T_J=25^\circ C$

^{a3}: $I_{SD}=7A, di/dt \leq 100A/us, V_{DD} \leq BV_{DS}, \text{Start } T_J=25^\circ C$

Characteristics Curve:

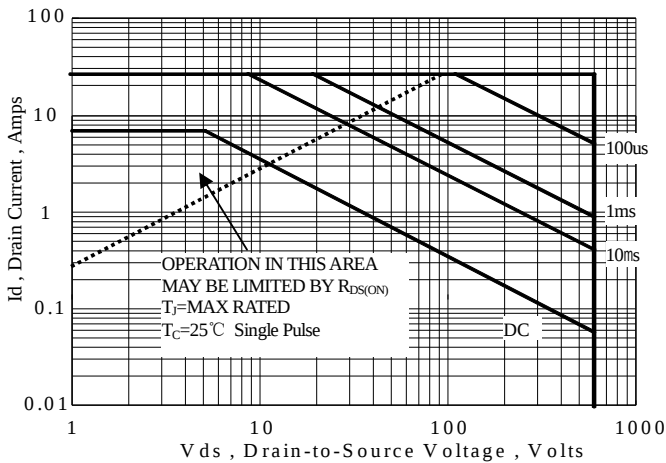


Figure 1 Maximum Forward Bias Safe Operating Area

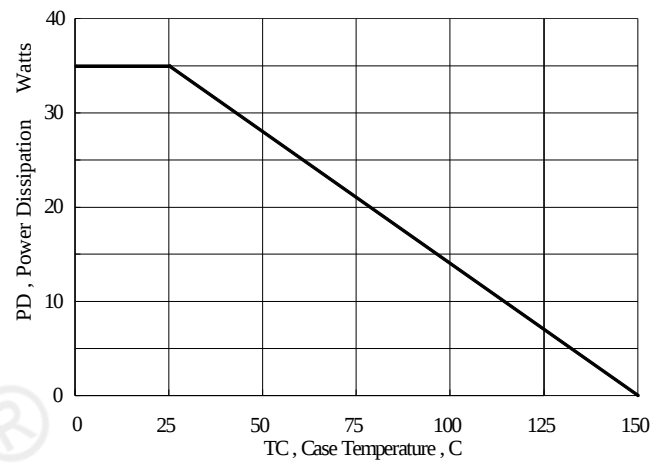


Figure 2 Maximum Power Dissipation vs Case Temperature

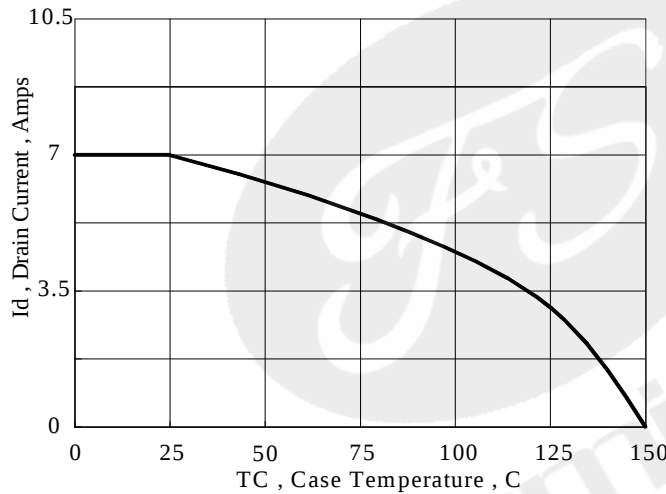


Figure 3 Maximum Continuous Drain Current vs Case Temperature

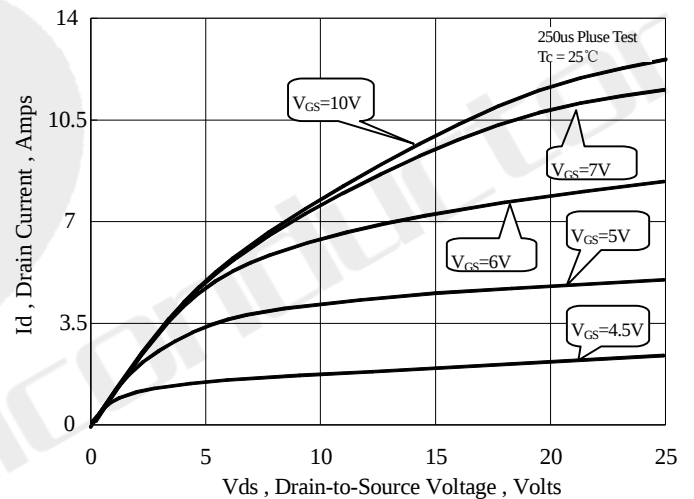


Figure 4 Typical Output Characteristics

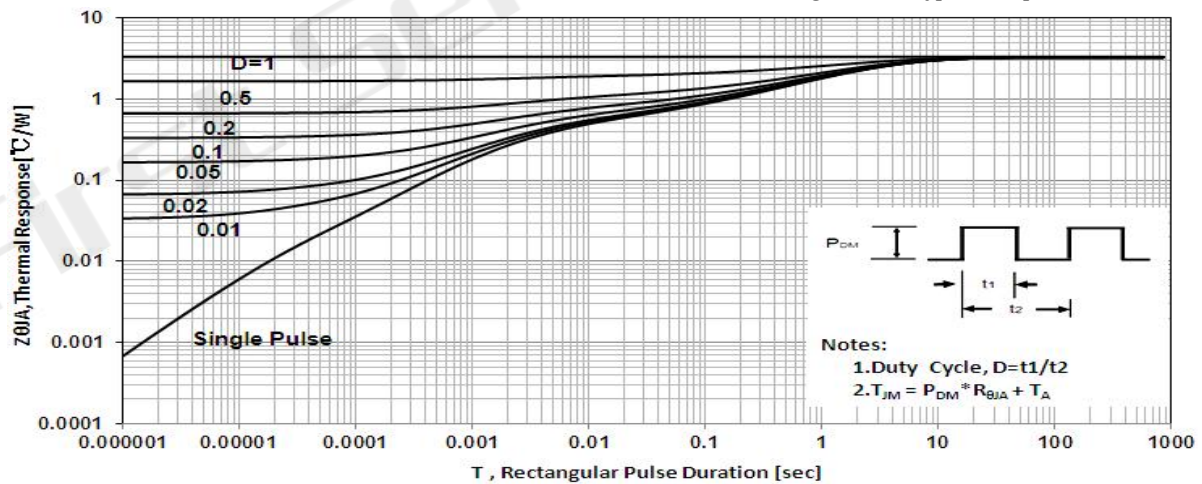


Figure 5 Maximum Effective Thermal Impedance, Junction to Case

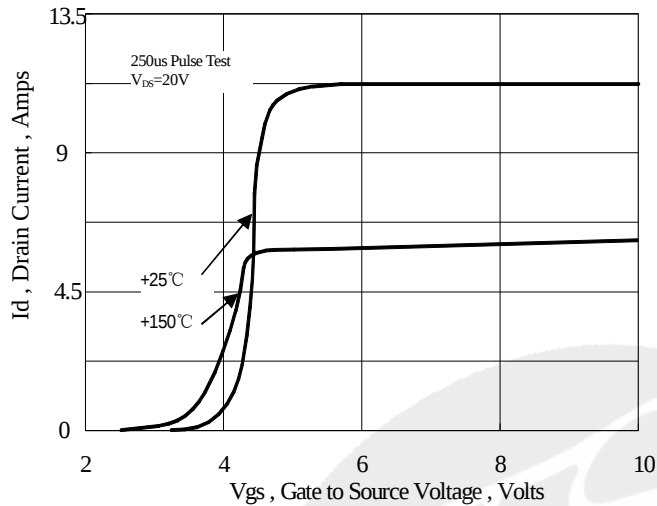


Figure 6 Typical Transfer Characteristics

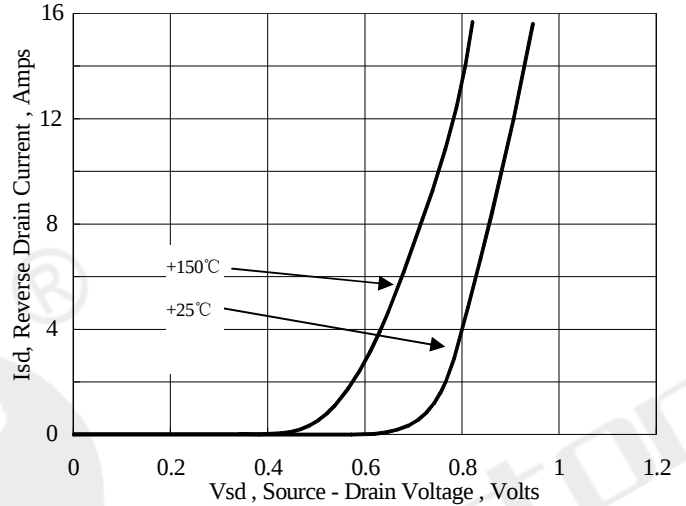


Figure 7 Typical Body Diode Transfer Characteristics

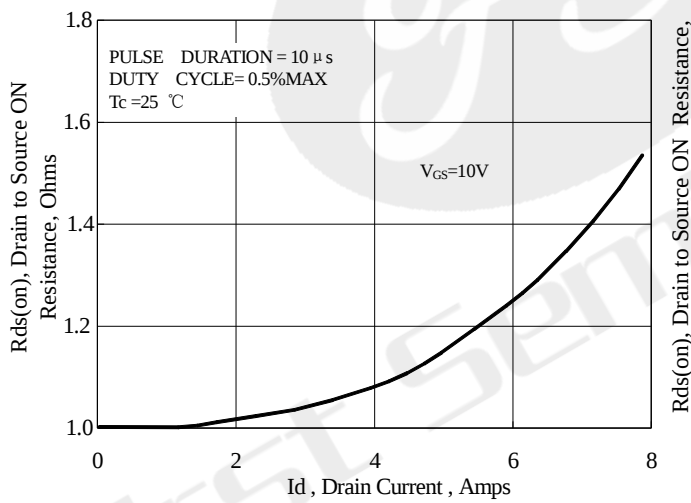


Figure 8 Typical Drain to Source ON Resistance vs Drain Current

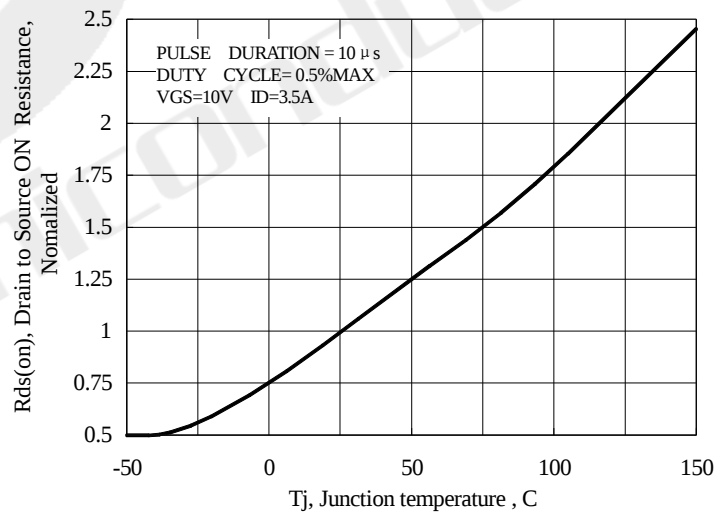


Figure 9 Typical Drain to Source on Resistance vs Junction Temperature

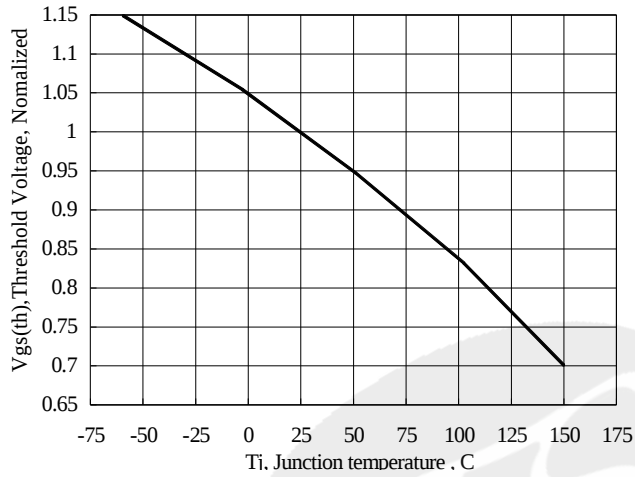


Figure 10 Typical Theshold Voltage vs Junction Temperature

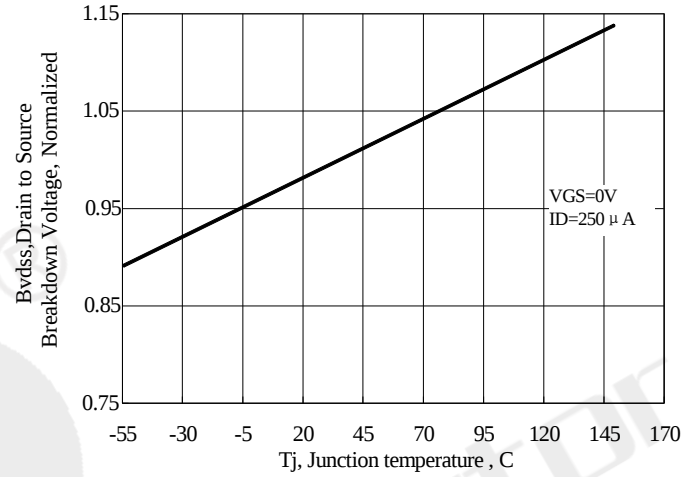


Figure 11 Typical Breakdown Voltage vs Junction Temperature

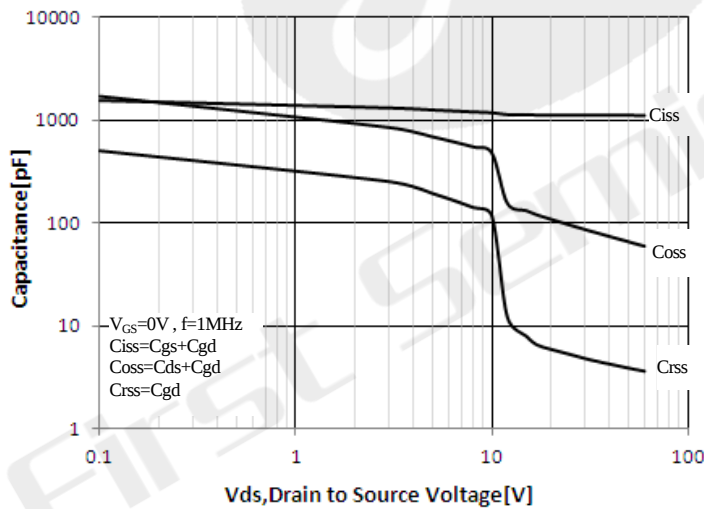


Figure 12 Typical Capacitance vs Drain to Source Voltage

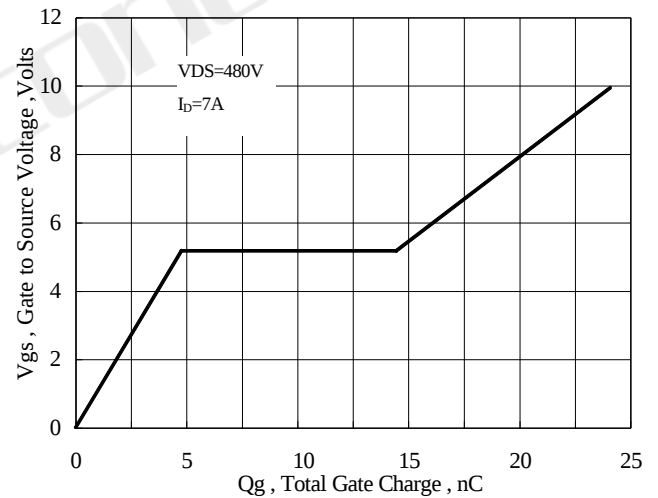


Figure 13 Typical Gate Charge vs Gate to Source Voltage

Test Circuit and Waveform

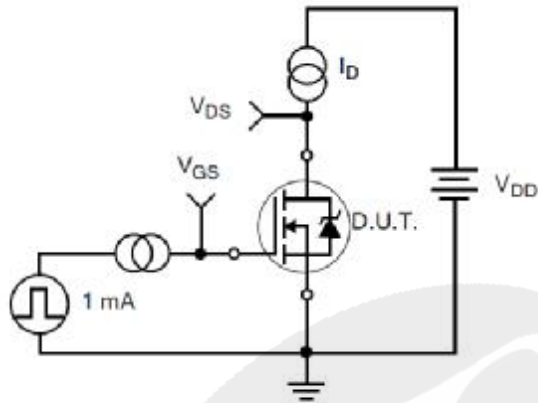


Figure 17. Gate Charge Test Circuit

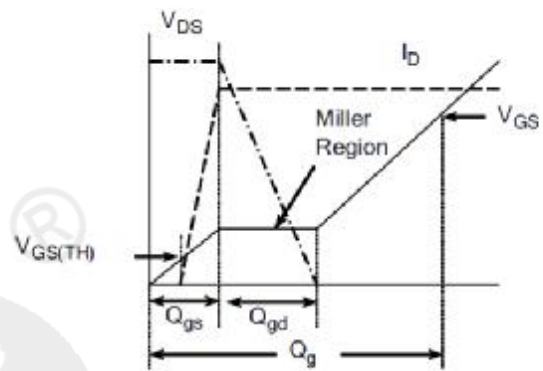


Figure 18. Gate Charge Waveform

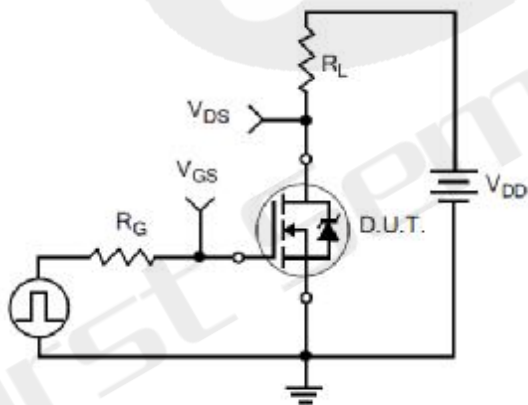


Figure 19. Resistive Switching Test Circuit

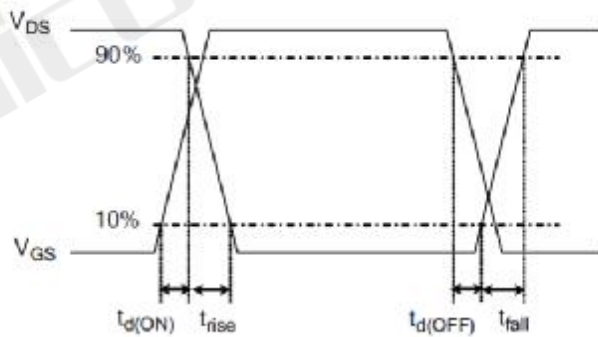


Figure 20. Resistive Switching Waveforms

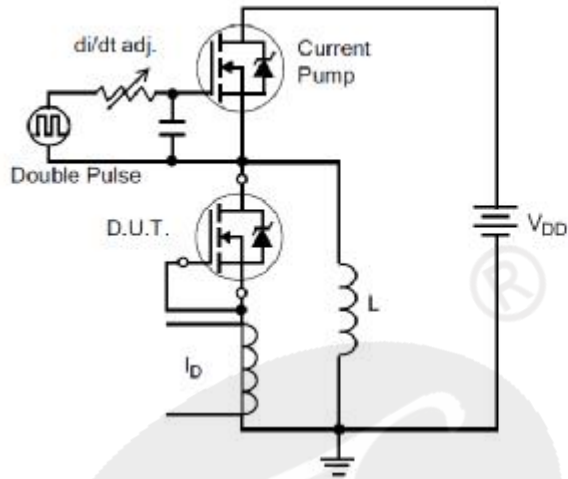


Figure 21. Diode Reverse Recovery Test Circuit

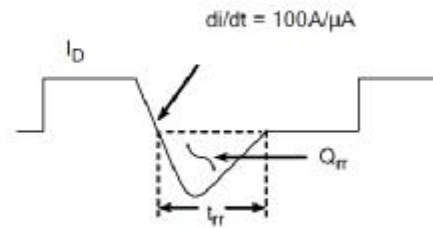


Figure 22. Diode Reverse Recovery Waveform

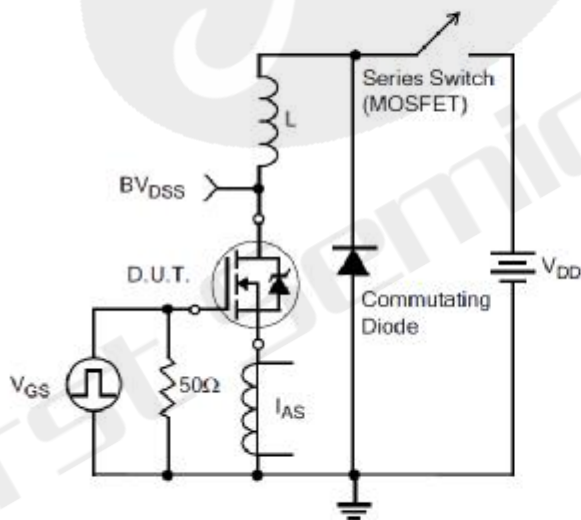


Figure 23. Unclamped Inductive Switching Test Circuit

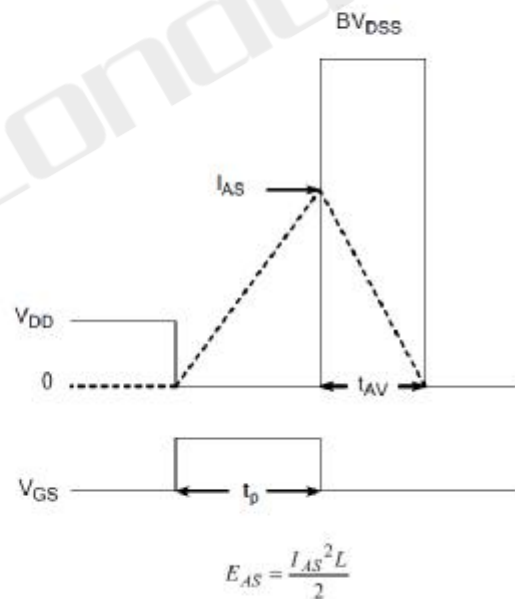
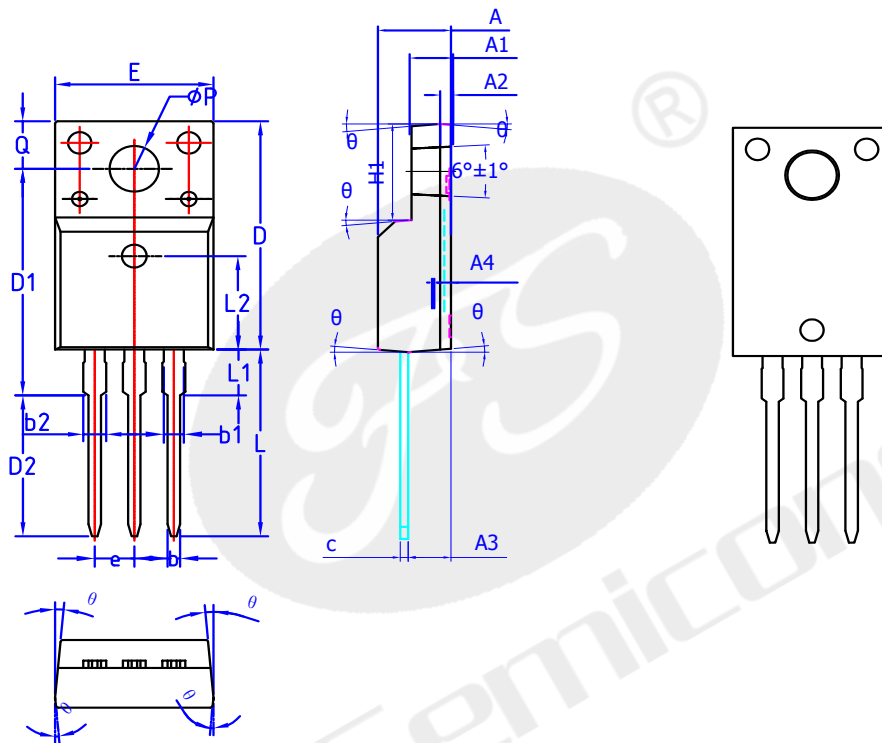


Figure 24. Unclamped Inductive Switching Waveforms

Package Dimension

TO-220F



Unit: mm			
COMMON DIMENSIONS			
(UNITS OF MEASURE= MILLIMETER)			
SYMBOL	MIN	NOM	MAX
A	4.50	4.70	4.90
A1	2.34	2.54	2.74
A2		0.70 REF	
A3	2.56	2.76	2.96
b	0.70	0.80	0.90
b1	1.17	1.2	1.25
b2	1.17	1.2	1.25
c	0.45	0.50	0.60
D	15.67	15.87	16.07
D1	15.55	15.75	15.95
D2	10.0	10.2	10.4
E	9.96	10.16	10.36
e		2.54BSC	
H1	6.48	6.68	6.88
L	12.68	12.98	13.28
L1	-	-	3.50
L2		6.50REF	
ØP	3.08	3.18	3.28
Q	3.20	3.30	3.40
Ø1	1"	3"	5"
A4	0.53	0.56	0.59



Declaration

- FIRST reserves the right to change the specifications, the same specifications of products due to different packaging line mold, the size of the appearance will be slightly different, shipped in kind, without notice! Customers should obtain the latest version information before ordering, and verify whether the relevant information is complete and up-to-date.
- Any semiconductor product under certain conditions has the possibility of failure or failure, The buyer has the responsibility to comply with safety standards and take safety measures when using FIRST products for system design and manufacturing, To avoid To avoid potential failure risks, which may cause personal injury or property damage!
- Product promotion endless, our company will wholeheartedly provide customers with better products!

ATTACHMENT

Revision History

Date	REV	Description	Page
2018.01.01	1.0	Initial release	