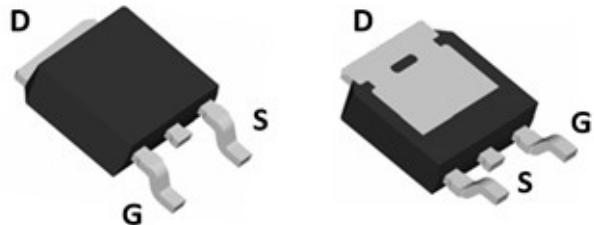


P-Channel Enhancement Mode Field Effect Transistor

RCD18P10

Product Summary

- V_{DS} -100V
- I_D -18A
- $R_{DS(ON)}$ at $V_{GS}=-10V$ <110 mohm
- $R_{DS(ON)}$ at $V_{GS}=-4.5V$ <120 mohm
- 100% UIS Tested
- 100% ∇V_{DS} Tested



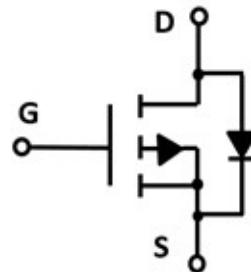
General Description

- Split gate trench MOSFET technology
- Low $R_{DS(on)}$ & FOM
- Extremely low switching loss
- Excellent stability and uniformity

Applications

- Power management
- Portable equipment

TO-252



■ Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	-100	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_c=25^\circ C$	I_D	-18	A
	$T_c=100^\circ C$		-12	
Pulsed Drain Current ^A		I_{DM}	-72	A
Avalanche energy ^B		E_{AS}	100	mJ
Total Power Dissipation	$T_c=25^\circ C$	P_D	72	W
	$T_c=100^\circ C$		28.8	
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	°C

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D		$R_{\theta JA}$	15	20	°C/W
Thermal Resistance Junction-to-Ambient ^D	Steady-State		40	50	
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	1.35	1.7	

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
RCD18P10	F1		2500	2500	250000	13" reel

P-Channel Enhancement Mode Field Effect Transistor

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■ Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=-250\mu\text{A}$	-100			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=-100\text{V}, V_{\text{GS}}=0\text{V}$	$T_J=25^\circ\text{C}$		-1	μA
			$T_J=55^\circ\text{C}$		-5	
			$T_J=125^\circ\text{C}$		-10	
Gate-Body Leakage Current	I_{GSS}	$V_{\text{GS}}= \pm 20\text{V}, V_{\text{DS}}=0\text{V}$			± 100	nA
Gate Threshold Voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=-250\mu\text{A}$	-1.0	-1.8	-2.5	V
Static Drain-Source On-Resistance	$R_{\text{DS(ON)}}$	$V_{\text{GS}}= -10\text{V}, I_{\text{D}}=-10\text{A}$		83	110	$\text{m}\Omega$
		$V_{\text{GS}}= -4.5\text{V}, I_{\text{D}}=-5\text{A}$		95	120	
Diode Forward Voltage	V_{SD}	$I_{\text{S}}=-10\text{A}, V_{\text{GS}}=0\text{V}$			-1.3	V
Maximum Body-Diode Continuous Current	I_{S}				-18	A
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{\text{DS}}=-50\text{V}, V_{\text{GS}}=0\text{V}, f=1\text{MHz}$		1051		pF
Output Capacitance	C_{oss}			119		
Reverse Transfer Capacitance	C_{rss}			25		
Switching Parameters						
Total Gate Charge	$Q_g(-10\text{V})$	$V_{\text{GS}}=-10\text{V}, V_{\text{DS}}=-50\text{V}, I_{\text{D}}=-5\text{A}$		20.1		nC
Total Gate Charge	$Q_g(-4.5\text{V})$			9.7		
Gate-Source Charge	Q_{gs}			3.9		
Gate-Drain Charge	Q_{gd}			4.3		
Reverse Recovery Charge	Q_{rr}	$I_F=-5\text{A}, dI/dt=100\text{A/us}$		140		ns
Reverse Recovery Time	t_{rr}			70		
Turn-on Delay Time	$t_{\text{D(on)}}$	$V_{\text{GS}}=-10\text{V}, V_{\text{DD}}=-50\text{V}, R_L=2.5\Omega$ $R_{\text{GEN}}=6\Omega$		10		ns
Turn-on Rise Time	t_r			30		
Turn-off Delay Time	$t_{\text{D(off)}}$			77		
Turn-off fall Time	t_f			81		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. $V_{\text{DD}}=50\text{V}$, $R_G=25\Omega$, $L=0.5\text{mH}$.

C. Pd is based on max. junction temperature, using junction-case thermal resistance.

D. The value of R_{QJA} is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with $TA = 25^\circ\text{C}$. The Power dissipation P_{DSM} is based on $R_{\text{QJA}} \leq 10\text{s}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design.

P-Channel Enhancement Mode Field Effect Transistor

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■ Typical Performance Characteristics

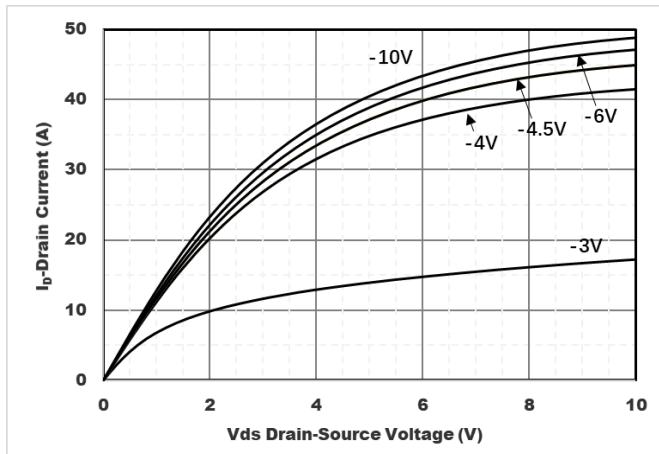


Figure1. Output Characteristics

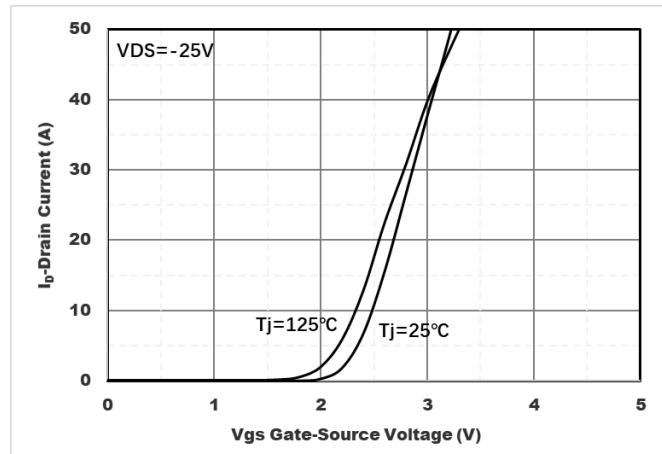


Figure2. Transfer Characteristics

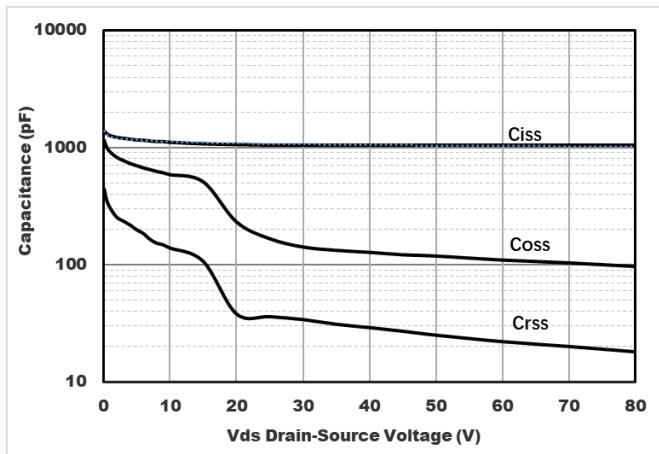


Figure3. Capacitance Characteristics

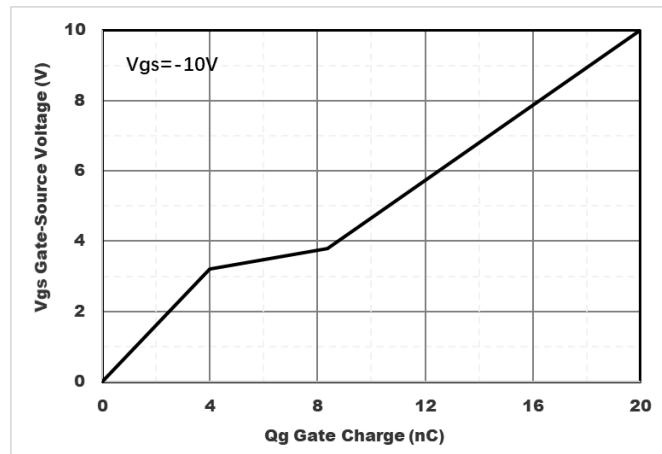


Figure4. Gate Charge

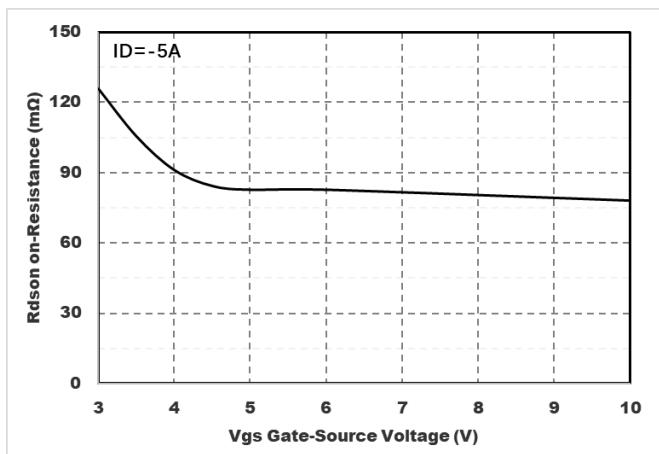


Figure5. : On-Resistance vs. Gate to Source Voltage

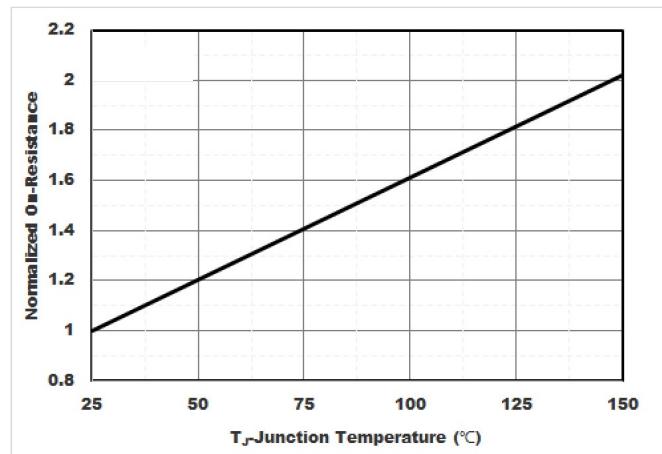


Figure6.Normalized On-Resistance

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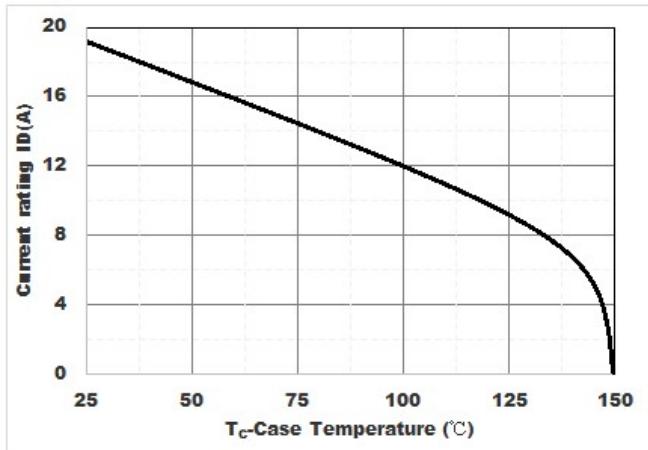


Figure7. Drain current

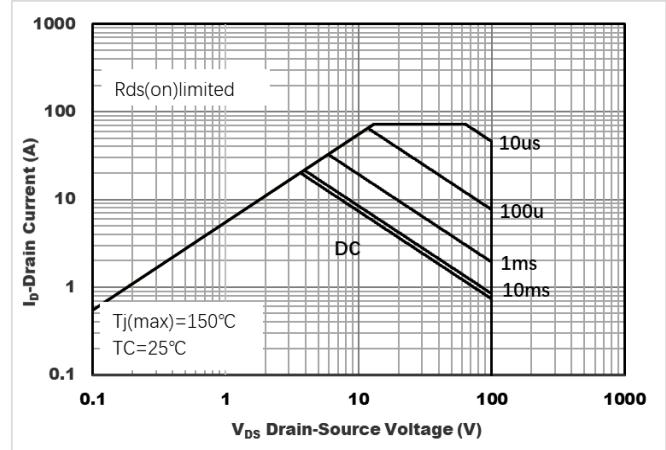


Figure8.Safe Operation Area

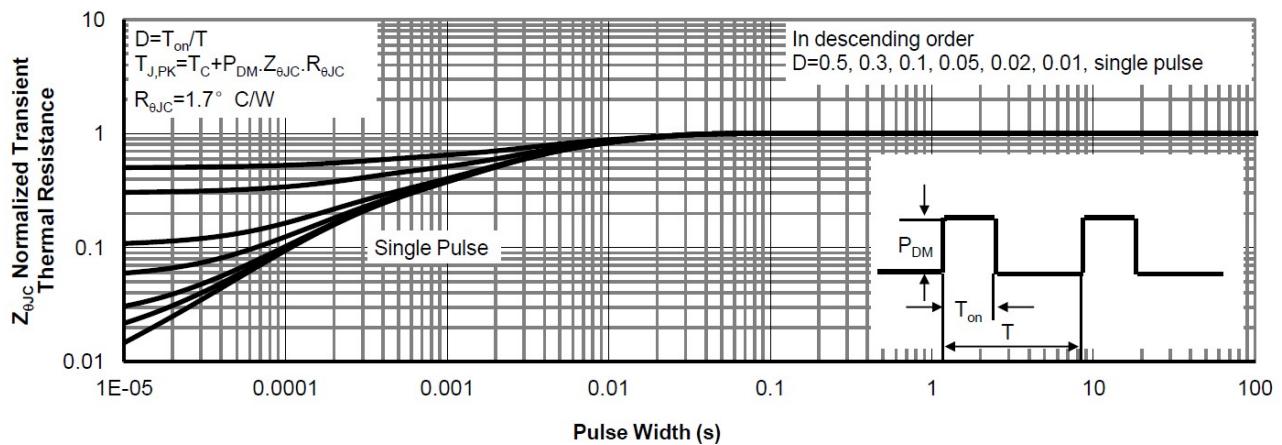
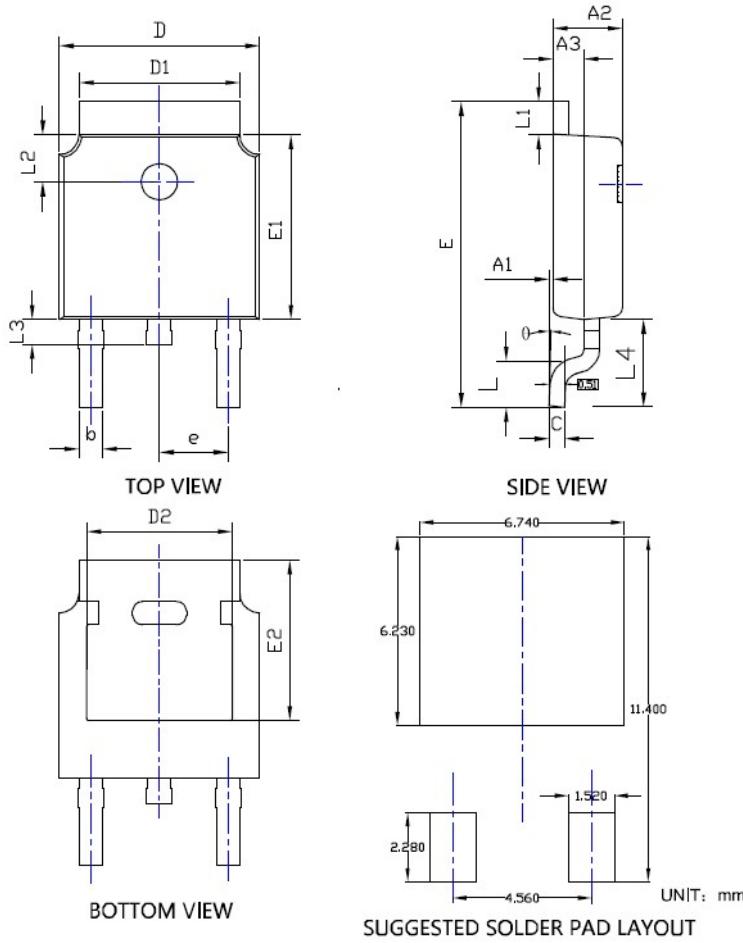


Figure9.Normalized Maximum Transient thermal impedance

P-Channel Enhancement Mode Field Effect Transistor

RCD18P10

■ TO-252 Package information



SYMBOL	INCHES			MILLIMETER		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A1	0.000	---	0.008	0.000	---	0.200
A2	0.087	0.091	0.094	2.200	2.300	2.400
A3	0.035	0.039	0.043	0.900	1.000	1.100
b	0.026	0.030	0.034	0.660	0.760	0.860
c	0.018	0.020	0.023	0.460	0.520	0.580
D	0.256	0.260	0.264	6.500	6.600	6.700
D1	0.203	0.209	0.215	5.150	5.300	5.450
D2	0.181	0.189	0.195	4.600	4.800	4.950
E	0.390	0.398	0.406	9.900	10.100	10.300
E1	0.236	0.240	0.244	6.000	6.100	6.200
E2	0.203	0.209	0.215	5.150	5.300	5.450
e	0.090BSC			2.286BSC		
L	0.049	0.059	0.069	1.250	1.500	1.750
L1	0.035	---	0.050	0.900	---	1.270
L2	0.055	---	0.075	1.400	---	1.900
L3	0.240	0.310	0.039	0.600	0.800	1.000
L4	0.114REF			2.900REF		
Ø	0°	---	10°	0°	---	10°