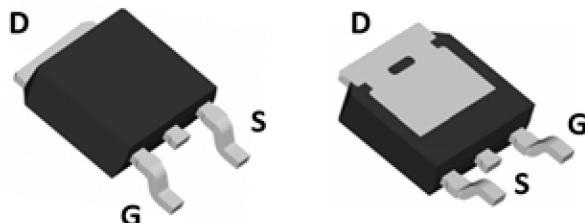


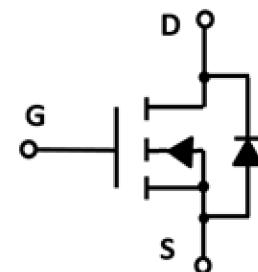
N-Channel Enhancement Mode Field Effect Transistor RC45N10K

Product Summary

• V_{DS}	100V
• I_D	45A
• $R_{DS(on)}$ (at $V_{GS}=10V$)	<17 mohm
• $R_{DS(on)}$ (at $V_{GS}=4.5V$)	<21.5 mohm
• 100% UIS Tested	
• 100% ∇V_{DS} Tested	



TO-252



General Description

- Low $R_{DS(on)}$ & FOM
- Extremely low switching loss
- Excellent stability and uniformity
- Fast switching and soft recovery

Applications

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	V_{DS}	100	V
Gate-source Voltage	V_{GS}	± 20	V
Drain Current	I_D	45	A
		28.5	
Pulsed Drain Current ^A	I_{DM}	180	A
Avalanche energy ^B	E_{AS}	81	mJ
Total Power Dissipation ^C	P_D	72	W
		28.8	
Junction and Storage Temperature Range	T_J, T_{STG}	-55~+150	°C

Thermal resistance

Parameter	Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	$R_{\theta JA}$	15	20	°C/W
Thermal Resistance Junction-to-Ambient ^D		40	50	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	1.35	1.7	

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
RC45N10	F1		2500	/	25000	13"Reel

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■ Electrical Characteristics ($T_j=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	100			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=100\text{V}, V_{\text{GS}}=0\text{V}$			1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{\text{GS}}= \pm 20\text{V}, V_{\text{DS}}=0\text{V}$			± 100	nA
Gate Threshold Voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	1	1.8	3	V
Static Drain-Source On-Resistance	$R_{\text{DS(ON)}}$	$V_{\text{GS}}= 10\text{V}, I_{\text{D}}=20\text{A}$		14	17	$\text{m}\Omega$
		$V_{\text{GS}}= 4.5\text{V}, I_{\text{D}}=20\text{A}$		17	21.5	$\text{m}\Omega$
Diode Forward Voltage	V_{SD}	$I_{\text{S}}=20\text{A}, V_{\text{GS}}=0\text{V}$			1.3	V
Maximum Body-Diode Continuous Current	I_{S}				45	A
Gate resistance	R_{G}	f= 1 MHz, Open drain		1		Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{\text{DS}}=50\text{V}, V_{\text{GS}}=0\text{V}, f=1\text{MHz}$		1135		pF
Output Capacitance	C_{oss}			399		
Reverse Transfer Capacitance	C_{rss}			18		
Switching Parameters						
Total Gate Charge	Q_{g}	$V_{\text{GS}}=10\text{V}, V_{\text{DS}}=50\text{V}, I_{\text{D}}=25\text{A}$		16		nC
Gate-Source Charge	Q_{gs}			5.6		
Gate-Drain Charge	Q_{gd}			2.4		
Reverse Recovery Charge	Q_{rr}	$I_{\text{F}}=20\text{A}, dI/dt=100\text{A/us}$		42		ns
Reverse Recovery Time	t_{rr}			39.8		
Turn-on Delay Time	$t_{\text{D(on)}}$			39.2		
Turn-on Rise Time	t_{r}	$V_{\text{GS}}=10\text{V}, V_{\text{DD}}=50\text{V}, I_{\text{D}}=25\text{A}$ $R_{\text{GEN}}=2.2\Omega$		11		ns
Turn-off Delay Time	$t_{\text{D(off)}}$			53.2		
Turn-off fall Time	t_{f}			15.8		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. $V_{\text{DD}}=50\text{V}$, $R_{\text{G}}=25\Omega$, $L=0.5\text{mH}$, $I_{\text{AS}}=25\text{A}$.

C. P_d is based on max. junction temperature, using junction-case thermal resistance.

D. The value of R_{qJA} is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with $TA = 25^\circ\text{C}$. The Power dissipation PDSM is based on $R_{\text{qJA}} t \leq 10\text{s}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design.

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■ Typical Performance Characteristics

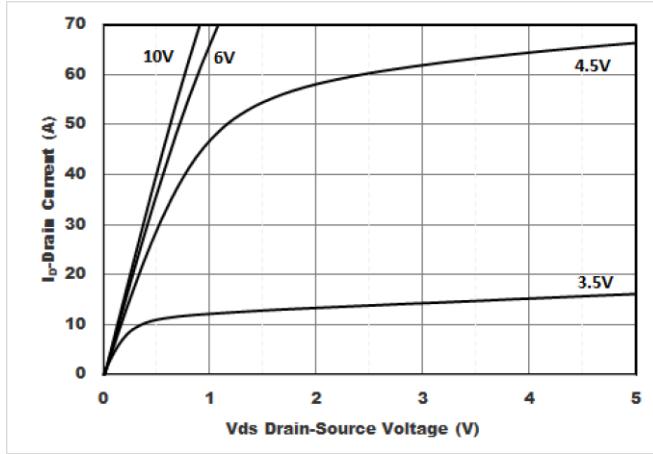


Figure1. Output Characteristics

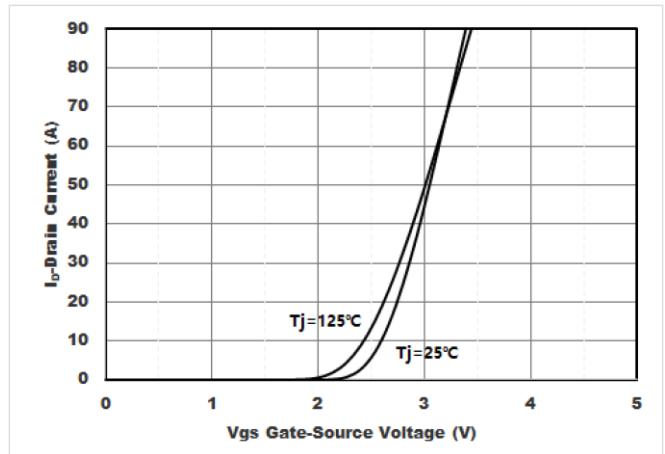


Figure2. Transfer Characteristics

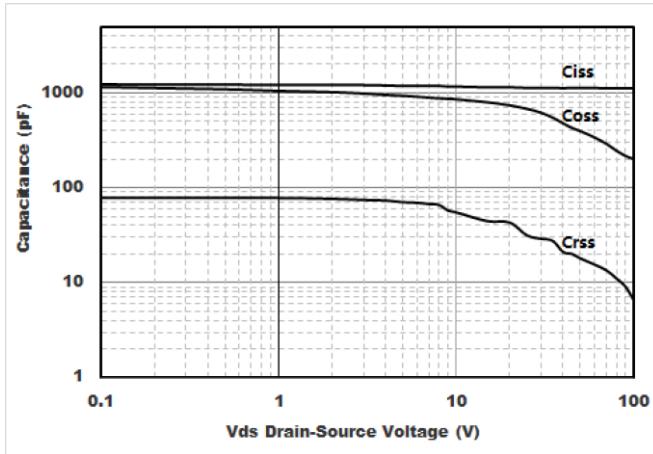


Figure3. Capacitance Characteristics

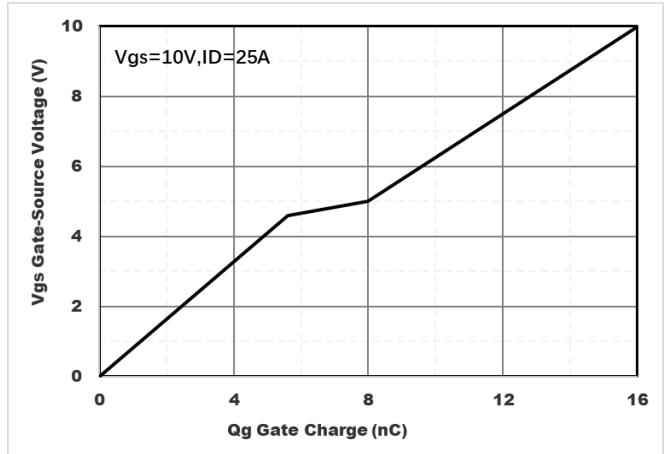


Figure4. Gate Charge

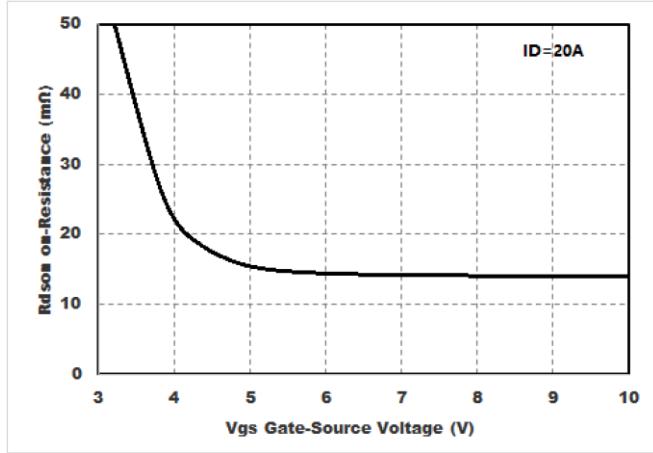


Figure5. : On-Resistance vs. Drain Current and Gate Voltage

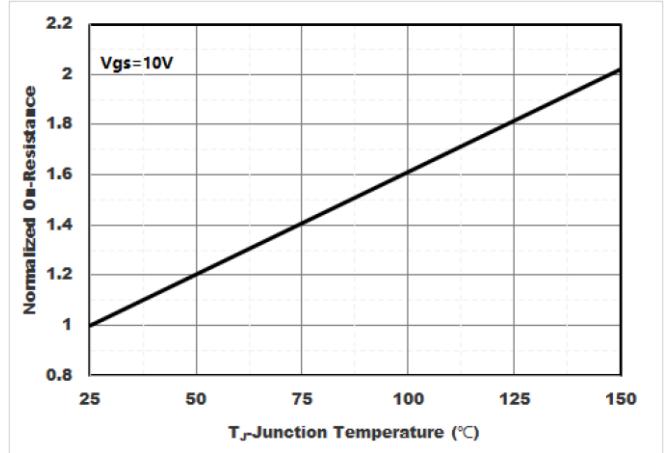


Figure6.Normalized On-Resistance

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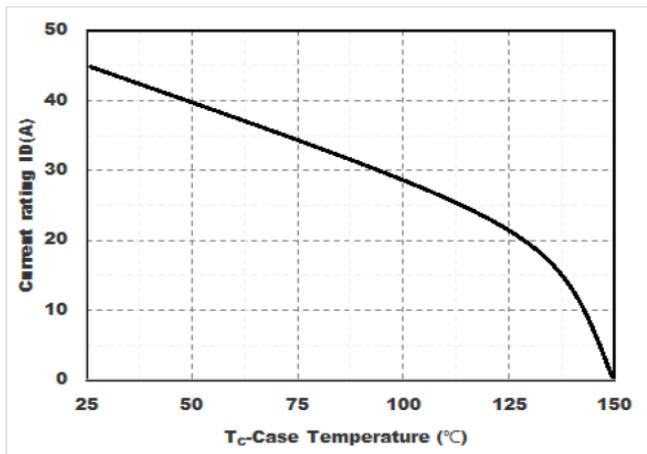


Figure 7. Drain current

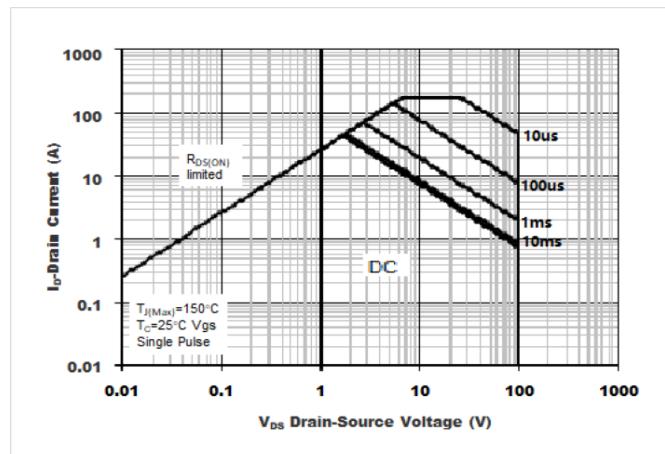


Figure 8. Safe Operation Area

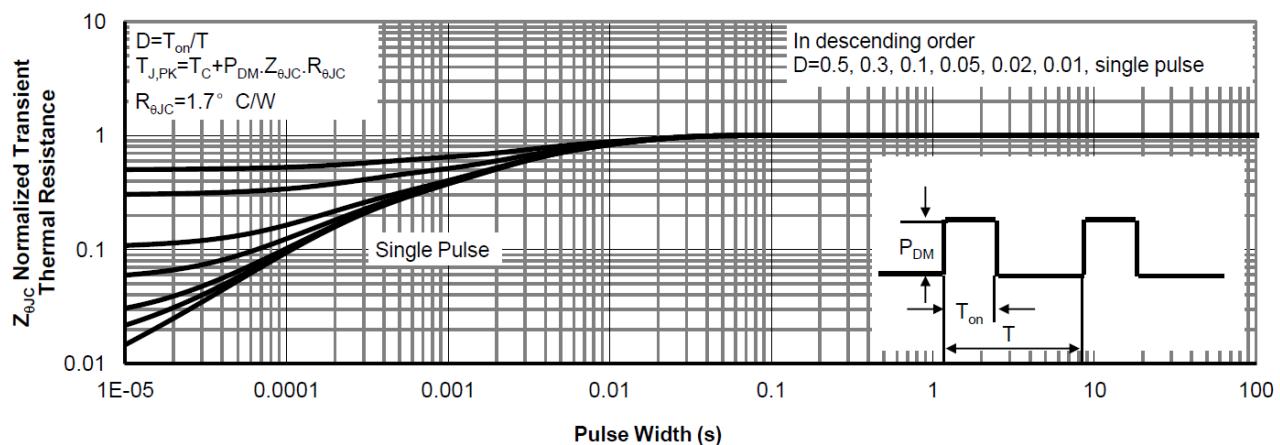
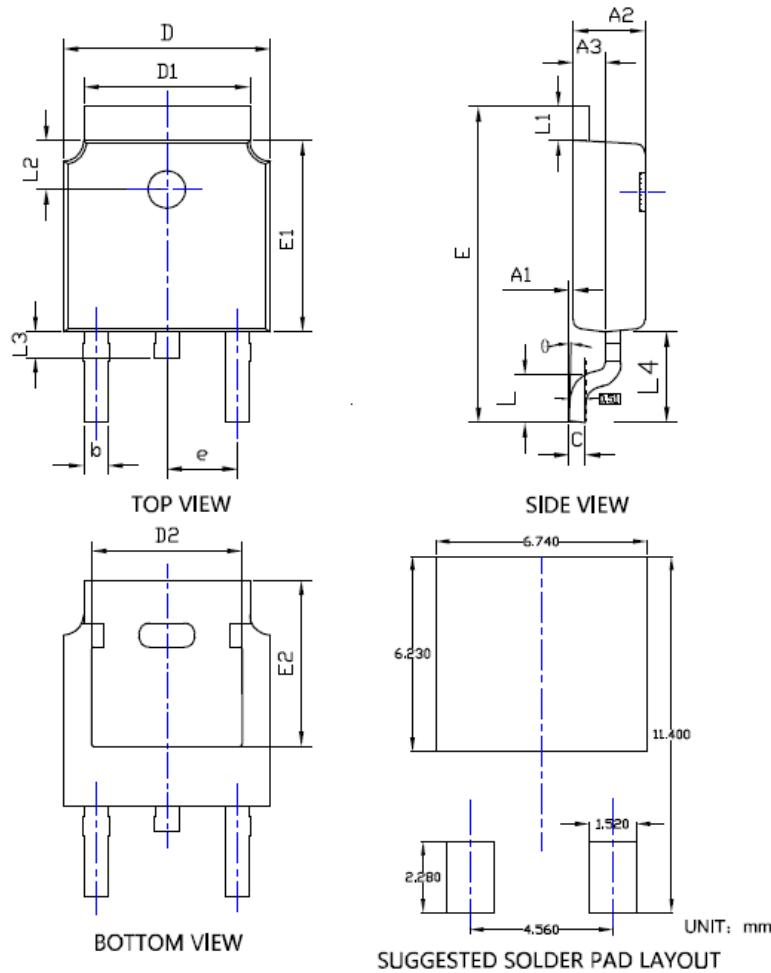


Figure 9. Normalized Maximum Transient thermal impedance

N-Channel Enhancement Mode Field Effect Transistor

RC45N10K

■ TO-252 Package information



SYMBOL	INCHES			MILLIMETER		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A1	0.000	---	0.008	0.000	---	0.200
A2	0.087	0.091	0.094	2.200	2.300	2.400
A3	0.035	0.039	0.043	0.900	1.000	1.100
b	0.026	0.030	0.034	0.660	0.760	0.860
c	0.018	0.020	0.023	0.460	0.520	0.580
D	0.256	0.260	0.264	6.500	6.600	6.700
D1	0.203	0.209	0.215	5.150	5.300	5.450
D2	0.181	0.189	0.195	4.600	4.800	4.950
E	0.390	0.398	0.406	9.900	10.100	10.300
E1	0.236	0.240	0.244	6.000	6.100	6.200
E2	0.203	0.209	0.215	5.150	5.300	5.450
e	0.090BSC			2.286BSC		
L	0.049	0.059	0.069	1.250	1.500	1.750
L1	0.035	---	0.050	0.900	---	1.270
L2	0.055	---	0.075	1.400	---	1.900
L3	0.240	0.310	0.039	0.600	0.800	1.000
L4	0.114REF			2.900REF		
Ø	0°	---	10°	0°	---	10°