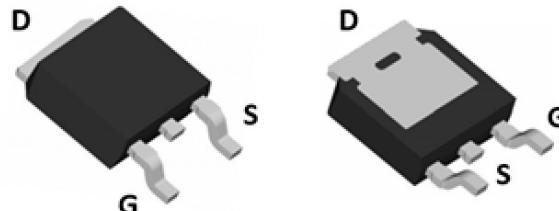


N-Channel Enhancement Mode Field Effect Transistor

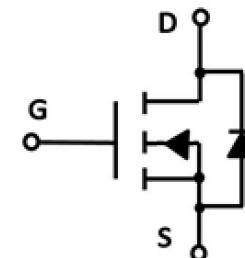
RC90N06

Product Summary

- V_{DS} 60V •
- I_D 90A •
- $R_{DS(ON)}$ (at $V_{GS}=10V$) <7.5 mohm •
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) <9.5 mohm •
- 100% UIS Tested
- 100% ∇V_{DS} Tested



TO-252



General Description

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation •
- High density cell design for low $R_{DS(ON)}$

Applications

- DC-DC Converters
- Power management functions
- Industrial and Motor Drive application

■ Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current (Silicon limited)	$T_c=25^\circ C$	I_D	90	A
	$T_c=100^\circ C$		50	
Pulsed Drain Current ^A		I_{DM}	300	A
Avalanche energy ^B		E_{AS}	150	mJ
Total Power Dissipation ^C	$T_c=25^\circ C$	P_D	78	W
	$T_c=100^\circ C$		31	
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	°C

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	$t \leq 10S$	$R_{\theta JA}$	15	20	°C/W
Thermal Resistance Junction-to-Ambient ^D	Steady-State		40	50	
Thermal Resistance Junction-to-Case	Steady-State		1.3	1.6	

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
RC90N06	F1	90N06	2500	2500	25000	13" reel

■ Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	60			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=60\text{V}, V_{\text{GS}}=0\text{V}$	$T_J=25^\circ\text{C}$		1	μA
			$T_J=55^\circ\text{C}$		5	
Gate-Body Leakage Current	I_{GSS}	$V_{\text{GS}}= \pm 20\text{V}, V_{\text{DS}}=0\text{V}$			± 100	nA
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	1.2	1.7	2.5	V
Static Drain-Source On-Resistance	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}}= 10\text{V}, I_{\text{D}}=20\text{A}$		5.5	7.5	$\text{m}\Omega$
		$V_{\text{GS}}= 4.5\text{V}, I_{\text{D}}=10\text{A}$		6.9	9.5	
Diode Forward Voltage	V_{SD}	$I_{\text{S}}=20\text{A}, V_{\text{GS}}=0\text{V}$		0.85	1.3	V
Maximum Body-Diode Continuous Current	I_{S}				80	A
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{\text{DS}}=35\text{V}, V_{\text{GS}}=0\text{V}, f=1\text{MHz}$		2000		pF
Output Capacitance	C_{oss}			390		
Reverse Transfer Capacitance	C_{rss}			13		
Gate Resistance	R_g	$f=1\text{MHz}, \text{Open drain}$		1.6		Ω
Switching Parameters						
Total Gate Charge	$Q_g(10\text{V})$	$V_{\text{DS}}=30\text{V}, I_{\text{D}}=20\text{A}$		34		nC
Total Gate Charge	$Q_g(4.5\text{V})$			15.8		
Gate-Source Charge	Q_{gs}			7.8		
Gate-Drain Charge	Q_{gd}			5.2		
Reverse Recovery Charge	Q_{rr}	$I_F=20\text{A}, dI/dt=200\text{A/us}$		36		ns
Reverse Recovery Time	t_{rr}			27		
Turn-on Delay Time	$t_{\text{D(on)}}$	$V_{\text{GS}}=10\text{V}, V_{\text{DD}}=30\text{V}, I_{\text{D}}=12\text{A}$ $R_{\text{GEN}}=3\Omega$		10		ns
Turn-on Rise Time	t_r			36		
Turn-off Delay Time	$t_{\text{D(off)}}$			30		
Turn-off fall Time	t_f			57		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. $V_{\text{DD}}=50\text{V}, R_G=25\Omega, L=0.5\text{mH}, I_{\text{AS}}=24.5\text{A},$

C. Pd is based on max. junction temperature, using junction-case thermal resistance.

D. The value of R_{GJA} is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The Power dissipation P_{DSM} is based on $R_{\text{GJA}} \leq 10\text{s}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design.

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■ Typical Performance Characteristics

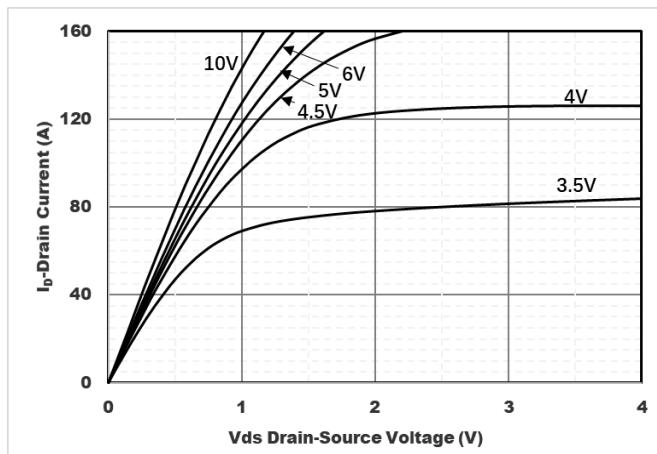


Figure1. Output Characteristics

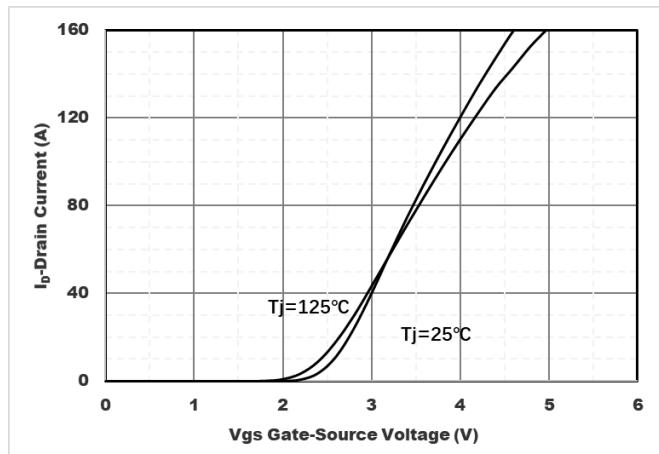


Figure2. Transfer Characteristics

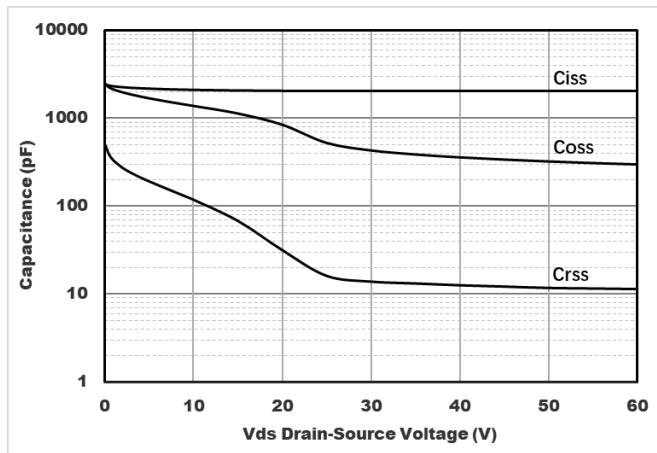


Figure3. Capacitance Characteristics

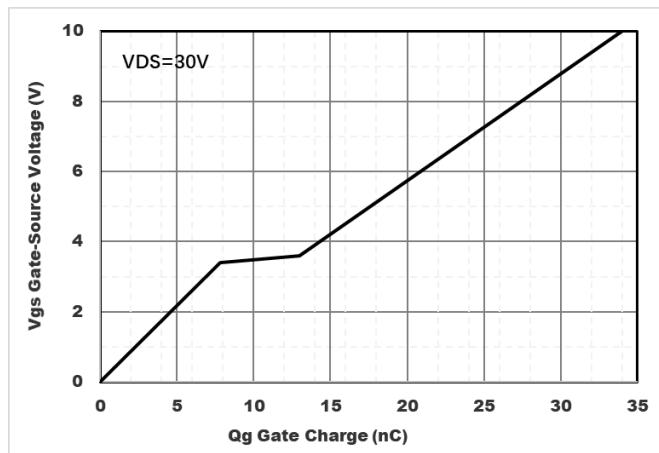


Figure4. Gate Charge

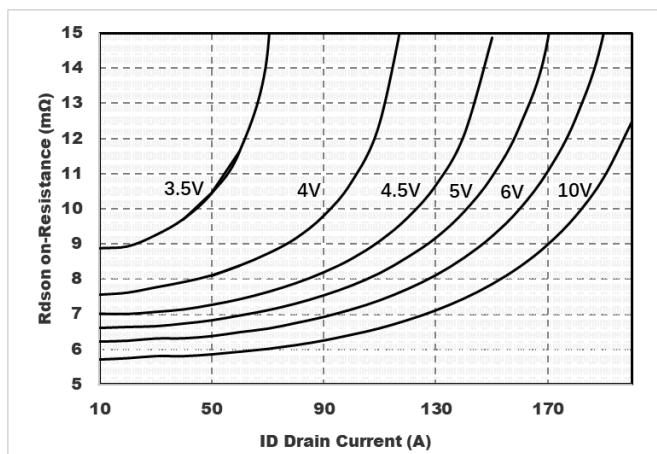


Figure5. Drain-Source on Resistance

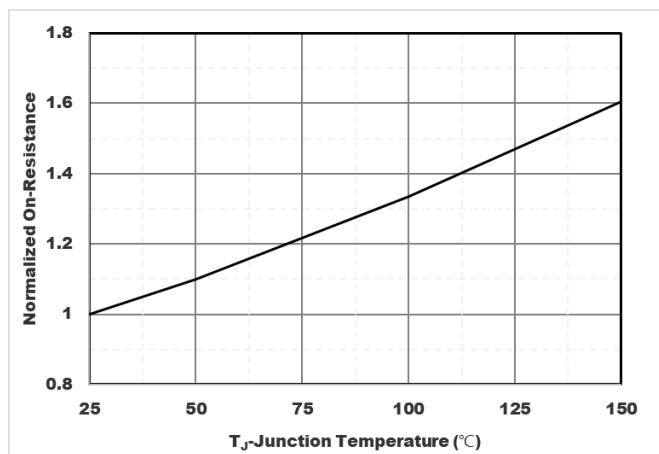


Figure6. Normalized On-Resistance

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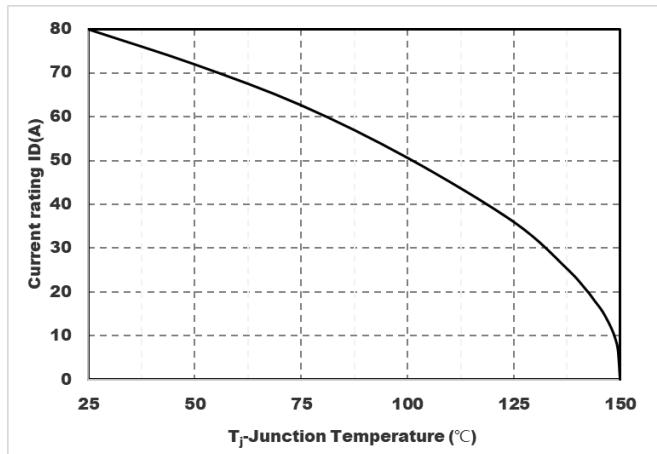


Figure7. Drain current

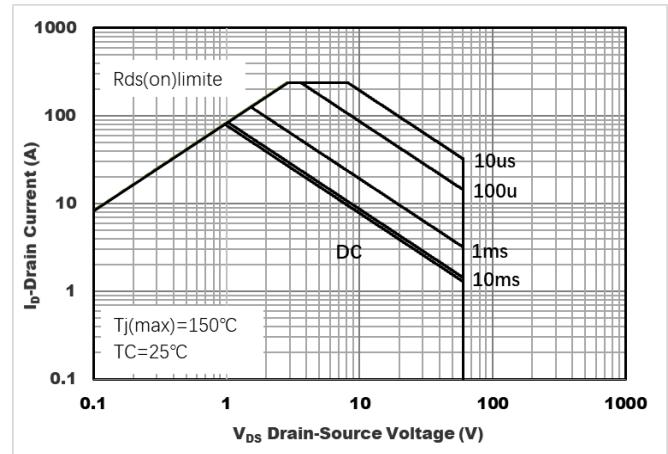


Figure8. Safe Operation Area

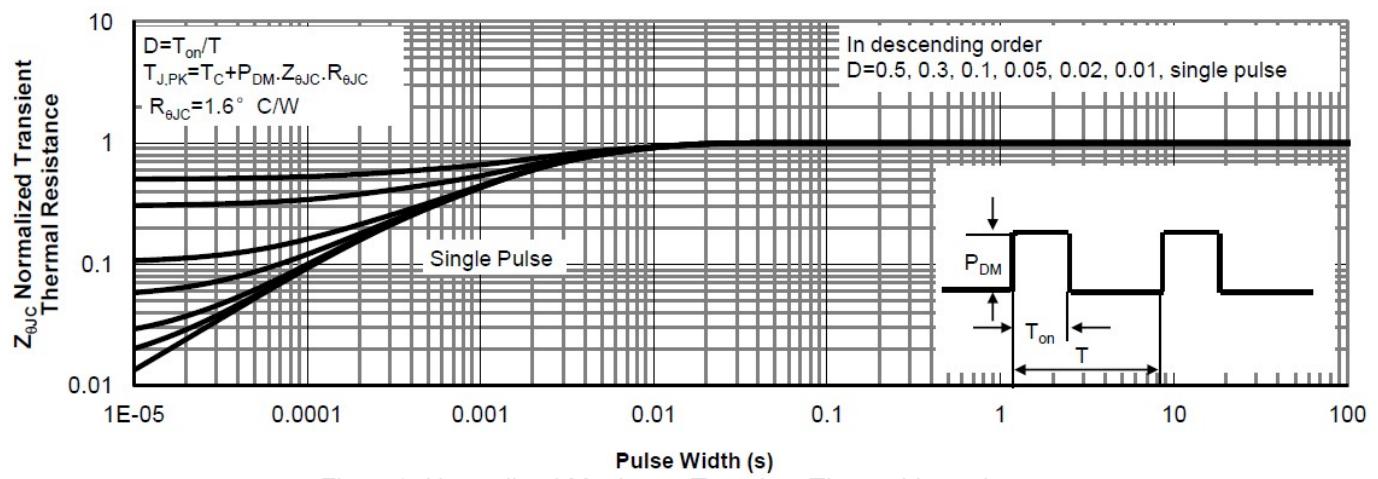
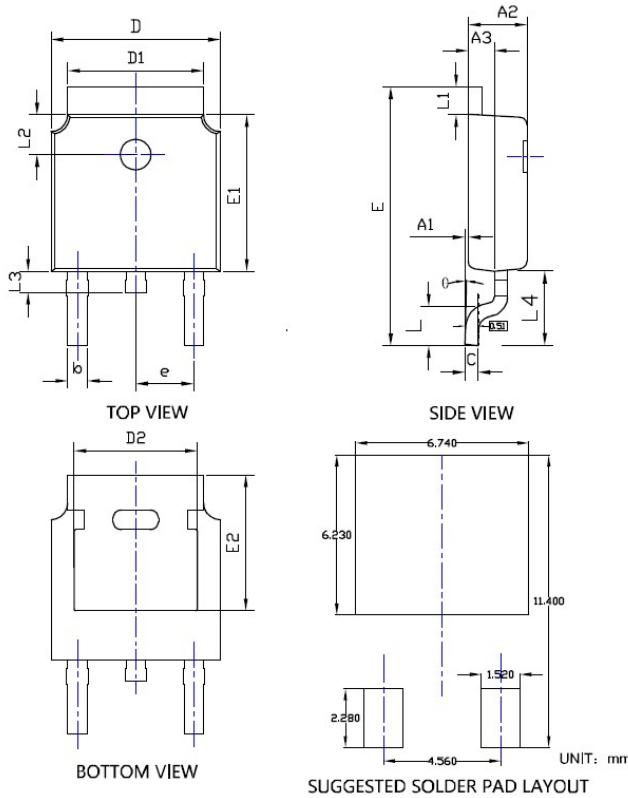


Figure8. Normalized Maximum Transient Thermal Impedance

N-Channel Enhancement Mode Field Effect Transistor

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■ TO-252 Package information



SYMBOL	DIMENSIONS			Millimeter		
	INCHES					
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A1	0.000	---	0.008	0.000	---	0.200
A2	0.087	0.091	0.094	2.200	2.300	2.400
A3	0.035	0.039	0.043	0.900	1.000	1.100
b	0.026	0.030	0.034	0.660	0.760	0.860
c	0.018	0.020	0.023	0.460	0.520	0.580
D	0.256	0.260	0.264	6.500	6.600	6.700
D1	0.203	0.209	0.215	5.150	5.300	5.450
D2	0.181	0.189	0.195	4.600	4.800	4.950
E	0.390	0.398	0.406	9.900	10.100	10.300
E1	0.236	0.240	0.244	6.000	6.100	6.200
E2	0.203	0.209	0.215	5.150	5.300	5.450
e	0.090BSC			2.286BSC		
L	0.049	0.059	0.069	1.250	1.500	1.750
L1	0.035	---	0.050	0.900	---	1.270
L2	0.055	---	0.075	1.400	---	1.900
L3	0.240	0.310	0.039	0.600	0.800	1.000
L4	0.114REF			2.900REF		
θ	0*	---	10*	0*	---	10*

NOTE:

- 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.