

N-Channel Enhancement Mode Field Effect Transistor

RC03N06B

Product Summary

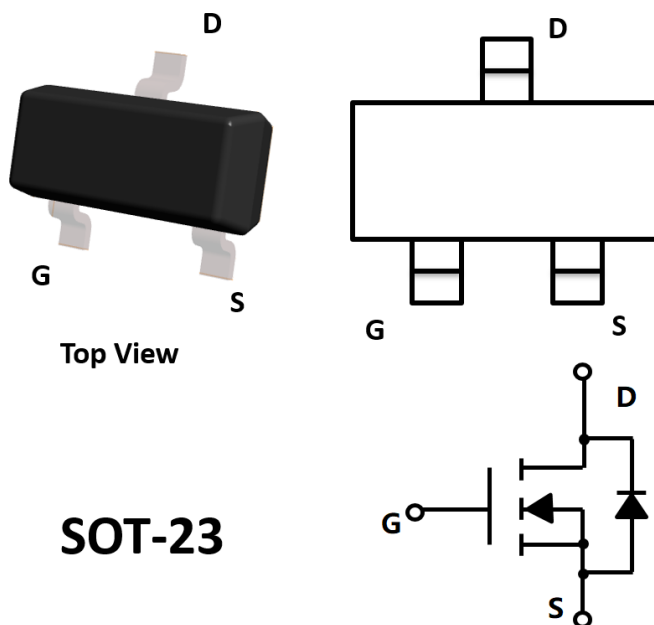
• V_{DS}	60V
• I_D	3.0A
• $R_{DS(ON)}$ (at $V_{GS}=10V$)	<100mohm
• $R_{DS(ON)}$ (at $V_{GS}=4.5V$)	<120mohm
• $R_{DS(ON)}$ (at $V_{GS}=2.5V$)	<200mohm

General Description

- Trench Power LV MOSFET technology
- High Density Cell Design for Low $R_{DS(ON)}$
- High Speed switching

Applications

- Battery protection
- Load switch
- Power management



■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	± 16	V
Drain Current	$T_A=25^\circ\text{C}$	I_D	3	A
	$T_A=70^\circ\text{C}$		2.4	
Pulsed Drain Current ^A		I_{DM}	12	A
Total Power Dissipation @ $T_A=25^\circ\text{C}$ Steady State		P_D	1.2	W
Thermal Resistance Junction-to-Ambient ^B		$R_{\theta JA}$	105	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
RC03N06B	F2		3000	30000	180000	7" reel

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■ Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	60			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60V, V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =± 16V, V _{DS} =0V			± 100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	0.65	0.95	1.55	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10V, I _D = 3A		65	100	mΩ
		V _{GS} = 4.5V, I _D = 2A		75	120	
		V _{GS} = 2.5V, I _D = 1A		100	200	
Diode Forward Voltage	V _{SD}	I _S = 3.0A, V _{GS} =0V		0.8	1.2	V
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =30V, V _{GS} =0V, f=1MHZ		451		pF
Output Capacitance	C _{oss}			38		
Reverse Transfer Capacitance	C _{rss}			31		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} = 10V, V _{DS} = 30V, I _D = 3.0A		13.8		nC
Gate-Source Charge	Q _{gs}			2.2		
Gate-Drain Charge	Q _{gd}			1.9		
Reverse Recovery Chrage	Q _{rr}	I _F = 3A, di/dt=100A/us		7.6		ns
Reverse Recovery Time	t _{rr}			30		
Turn-on Delay Time	t _{D(on)}	V _{GS} = 10V, V _{DS} = 30V, I _D = 1.5A R _{GEN} = 3Ω		3		
Turn-on Rise Time	t _r			18		
Turn-off Delay Time	t _{D(off)}			17		
Turn-off fall Time	t _f			22		

A. Pulse Test: Pulse Width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

B. $R_{\theta JA}$ is the sum of the junction-to-lead and lead-to-ambient thermal resistance, where the lead thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JL}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

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■ Typical Performance Characteristics

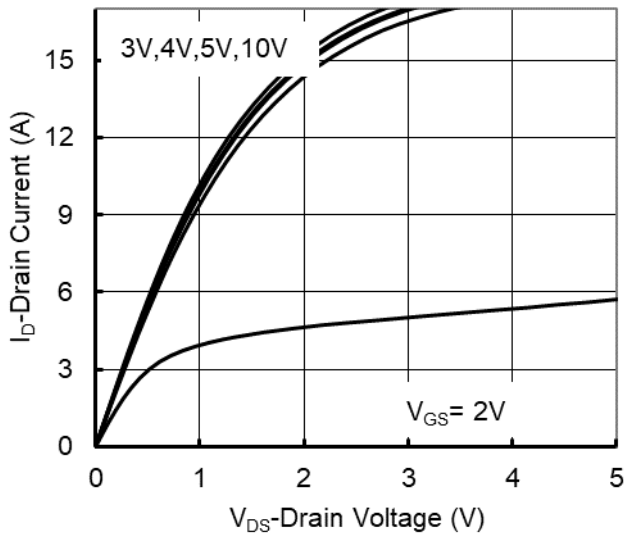


Figure1. Output Characteristics

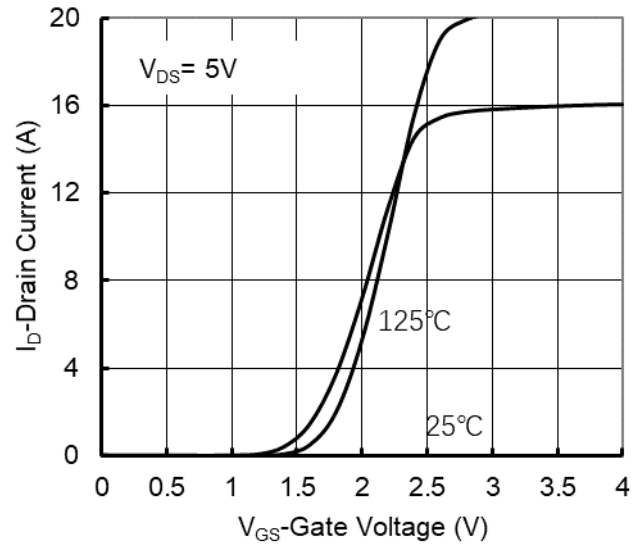


Figure2. Transfer Characteristics

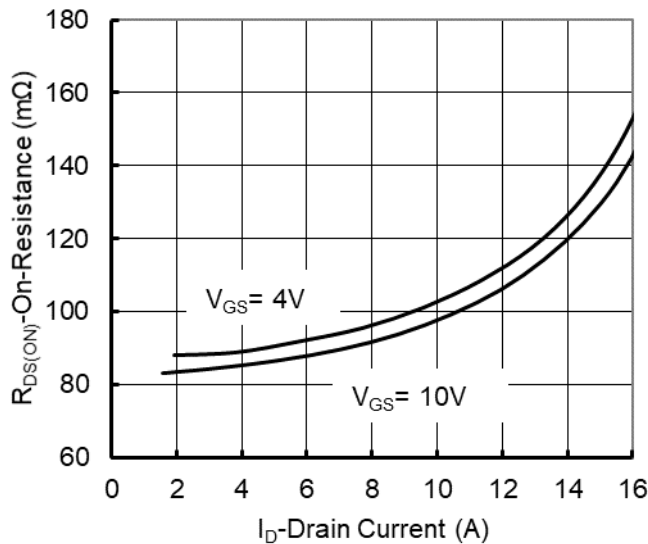


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

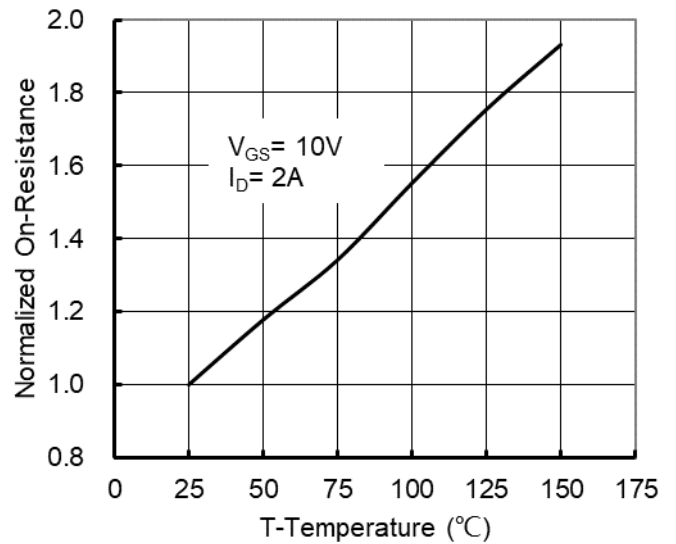


Figure 4: On-Resistance vs. Junction Temperature

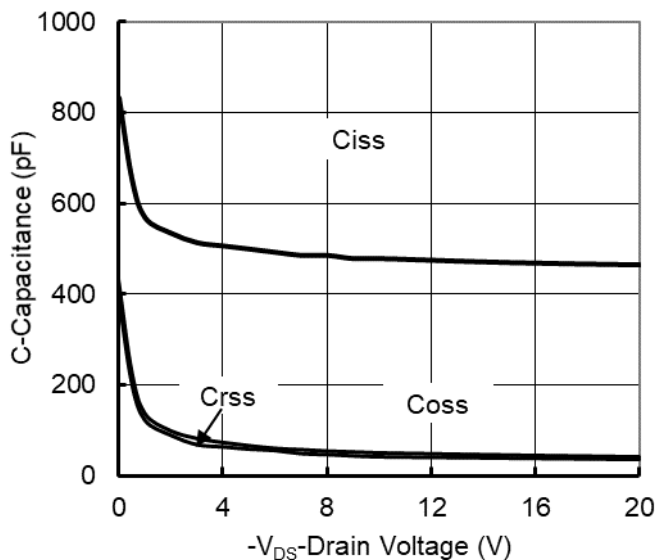


Figure5. Capacitance Characteristics

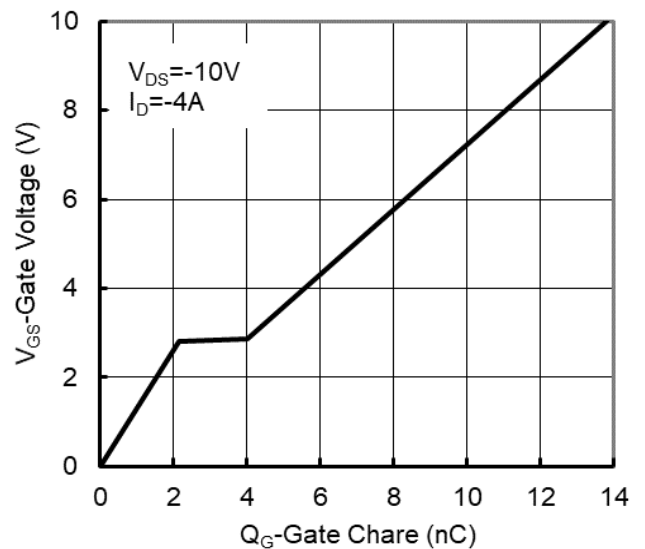


Figure6. Gate Charge

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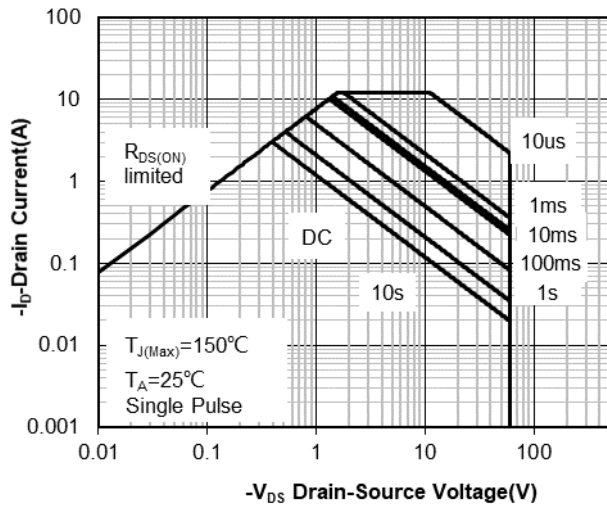


Figure7. Safe Operation Area

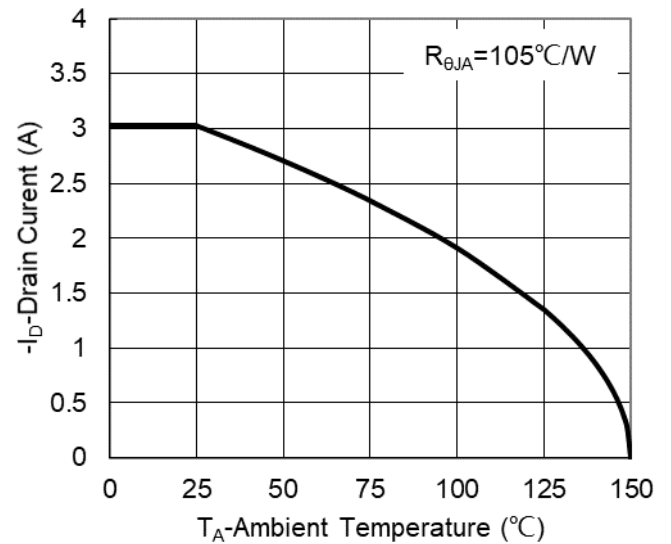


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

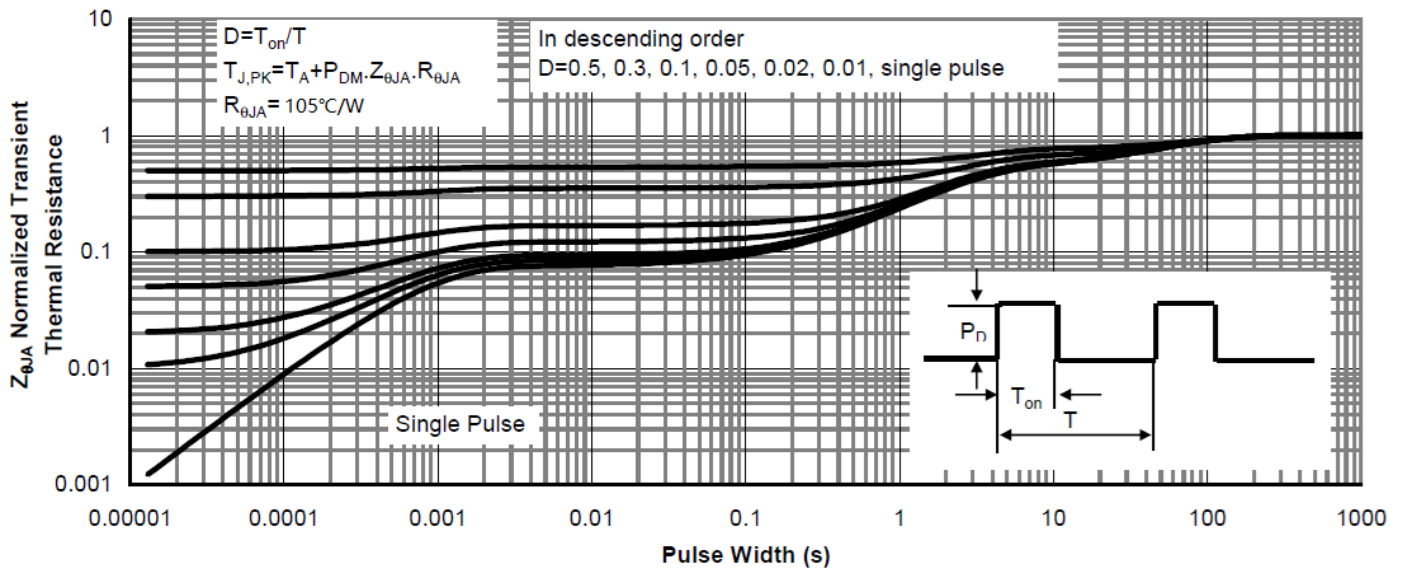
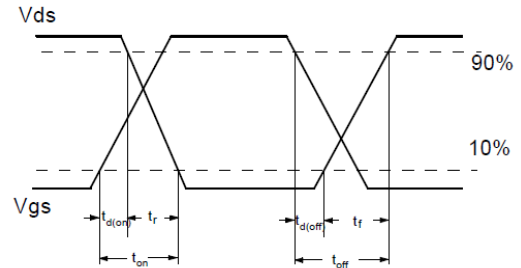
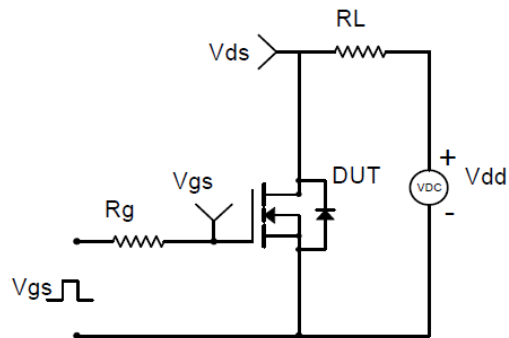


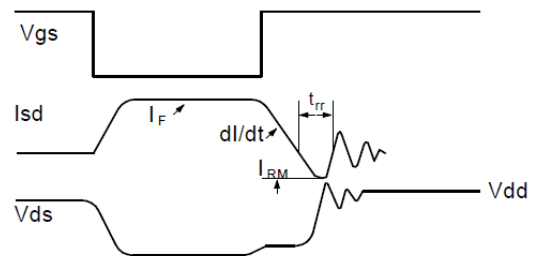
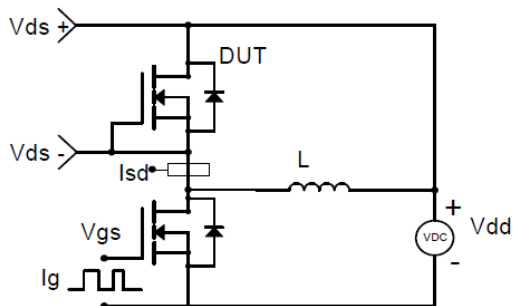
Figure9. Normalized Maximum Transient Thermal Impedance

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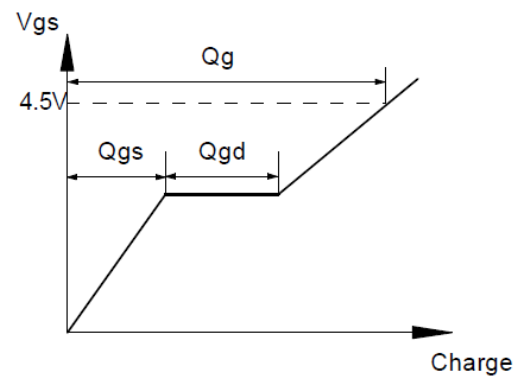
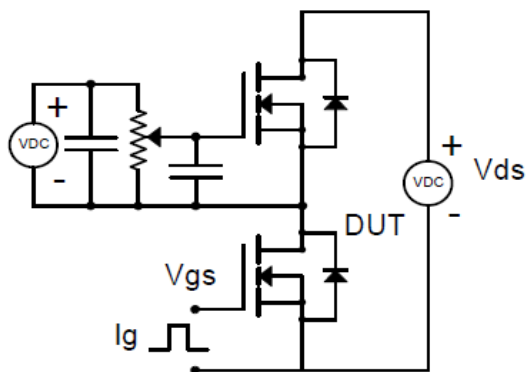
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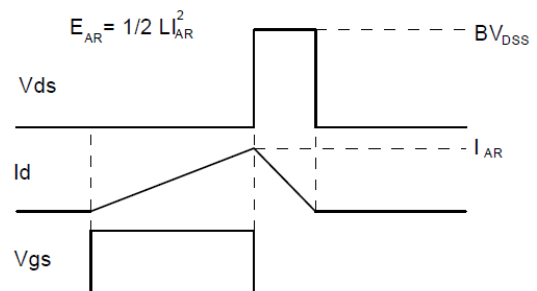
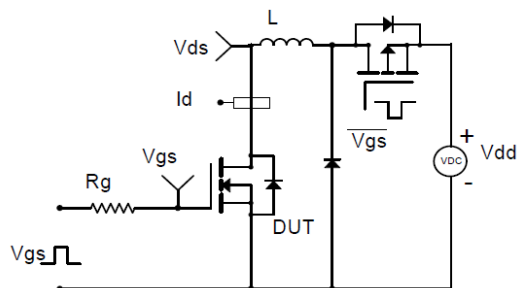
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform

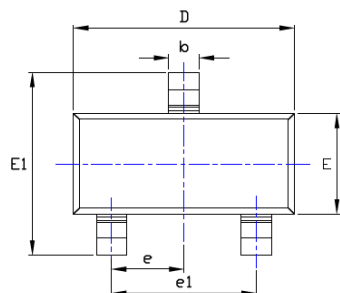


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

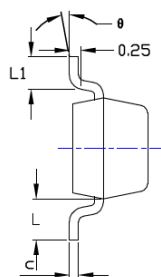
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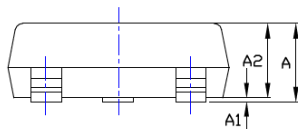
■ SOT-23 Package Information



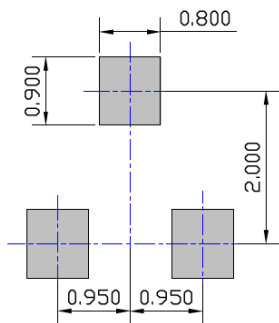
TOP VIEW



SIDE VIEW



SIDE VIEW



UNIT: mm

SUGGESTED SOLDER PAD LAYOUT

SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.035	0.045	0.900	1.150
A1	0.000	0.004	0.000	0.100
A2	0.035	0.041	0.900	1.050
b	0.012	0.020	0.300	0.500
c	0.004	0.008	0.100	0.200
D	0.110	0.118	2.800	3.000
E	0.047	0.055	1.200	1.400
E1	0.089	0.100	2.250	2.550
e	0.037TYP		0.950TYP	
e1	0.071	0.079	1.800	2.000
L	0.022REF		0.550REF	
L1	0.012	0.200	0.300	0.500
θ	0°	8°	0°	8°

NOTE:

- 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.