Rochester Electronics

*Datasheet*

# PART NUMBER

# 2147-70BYA

## Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

## Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

*The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.*

# M2147H
# HIGH SPEED 4096 x 1-BIT STATIC RAM

*Military*

| | M2147H-2 | M2147H-3 | M2147H |
|---|---|---|---|
| Max. Access Time (ns) | 45 | 55 | 70 |
| Max. Active Current (mA) | 180 | 180 | 180 |
| Max. Standby Current (mA) | 30 | 30 | 30 |

- **Pinout, Function, and Power Compatible to Industry Standard M2147**
- **HMOS* II Technology**
- **Completely Static Memory—No Clock or Timing Strobe Required**
- **Equal Access and Cycle Times**
- **Single +5V Supply**
- **Direct Performance Upgrade for M2147**
- **Power-Down**
- **High Density 18-Pin Package**
- **Separate Data Input and Output**
- **Three-State Output**
- **Military Temperature Range: −55°C to +125°C ($T_C$)**

The Intel M2147H is a 4096-bit static Random Access Memory organized as 4096 words by 1-bit using HMOS II, Intel's next generation high-performance MOS technology. It uses a uniquely innovative design approach which provides the ease-of-use features associated with non-clocked static memories and the reduced standby power dissipation associated with clocked static memories. To the user this means low standby power dissipation without the need for clocks, address setup and hold times, nor reduced data rates due to cycle times that are longer than access times.

$\overline{CS}$ controls the power-down feature. In less than a cycle time after $\overline{CS}$ goes high—deselecting the M2147H—the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ remains high. This device feature results in system power savings as great as 85% in larger systems, where the majority of devices are deselected.

The M2147H is placed in an 18-pin package configured with the industry standard pinout. It is directly TTL compatible in all respects: inputs, output, and a single +5V supply. The data is read out nondestructively and has the same polarity as the input data. A data input and a separate three-state output are used.

*HMOS is a patented process of Intel Corporation.

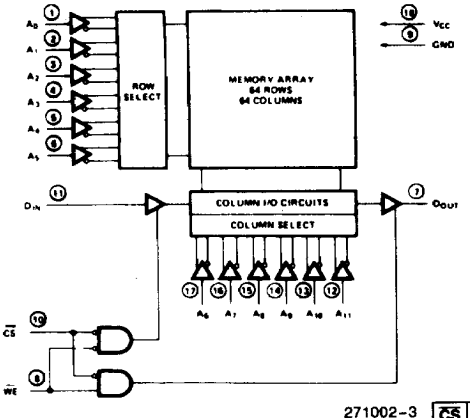


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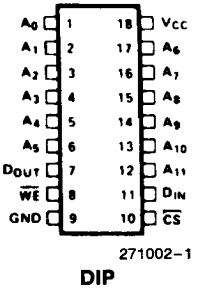
**Figure 1. Block Diagram**




271002-1

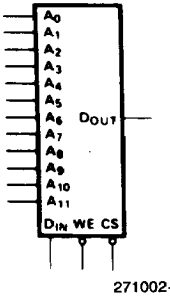
**DIP**

Diagrams are for pin reference only. Package sizes are not to scale.

**Figure 2. Pin Configuration**

**Truth Table**

| $\overline{CS}$ | $\overline{WE}$ | Mode | Output | Power |
|---|---|---|---|---|
| H | X | Not Selected | High Z | Standby |
| L | L | Write | High Z | Active |
| L | H | Read | $D_{OUT}$ | Active |




271002-2

**Figure 3. Logic Symbol**

**Pin Names**

| | |
|---|---|
| $A_0$–$A_{11}$ | Address Inputs |
| $\overline{WE}$ | Write Enable |
| $\overline{CS}$ | Chip Select |
| $D_{IN}$ | Data Input |
| $D_{OUT}$ | Data Output |
| $V_{CC}$ | Power (+5V) |
| GND | Ground |



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## ABSOLUTE MAXIMUM RATINGS*

Case Temperature Under Bias . . . −65°C to +135°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin
with Respect to Ground . . . . . −3.5V to +7V
Power Dissipation . . . . . 1.2W
D.C. Output Current . . . . . 20 mA

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

## Operating Conditions

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_C$ | Case Temperature (Instant On) | −55 | +125 | °C |
| $V_{CC}$ | Digital Supply Voltage | 4.50 | 5.50 | V |

## D.C. CHARACTERISTICS (Over Specified Operating Conditions)

| Symbol | Parameter | M2147H-2 M2147H-3, M2147H | | | Unit | Test Conditions | |
|---|---|---|---|---|---|---|---|
| | | Min | Typ(1) | Max | | | |
| $I_{LI}$ | Input Load Current (All Input Pins) | | 0.01 | 10 | µA | $V_{CC}$ = Max., $V_{IN}$ = GND to $V_{CC}$ | |
| $\|I_{LO}\|$ | Output Leakage Current | | 0.1 | 50 | µA | $\overline{CS}$ = $V_{IH}$, $V_{CC}$ = Max., $V_{OUT}$ = GND to 4.5V | |
| $I_{CC}$ | Operating Current | | 120 | 170 | mA | $T_C$ = 25°C | $V_{CC}$ = Max., $\overline{CS}$ = $V_{IL}$ Outputs Open |
| | | | | 180 | mA | $T_C$ = −55°C | |
| $I_{SB}$ | Standby Current | | 18 | 30 | mA | $V_{CC}$ = Min. to Max., $\overline{CS}$ = $V_{IH}$ | |
| $I_{PO}$(2) | Peak Power-On Current | | 35 | 70 | mA | $V_{CC}$ = GND to $V_{CC}$ Min. $\overline{CS}$ = Lower of $V_{CC}$ of $V_{IH}$ Min. | |
| $V_{IL}$ | Input Low Voltage | −3.0 | | 0.8 | V | | |
| $V_{IH}$ | Input High Voltage | 2.0 | | 6.0 | V | | |
| $V_{OL}$ | Output Low Voltage | | | 0.4 | V | $I_{OL}$ = 8 mA | |
| $V_{OH}$ | Output High Voltage | 2.4 | | | V | $I_{OH}$ = −4.0 mA | |
| $I_{OS}$ | Output Short Circuit Current | −275 | | +275 | mA | $V_{OUT}$ = GND to $V_{CC}$, $T_C$ = 0°C | |

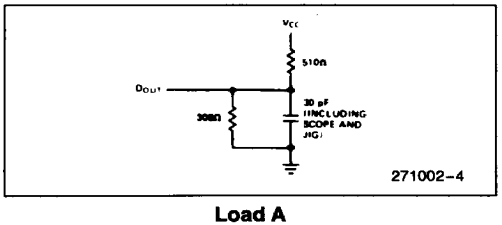
**NOTES:**
1. Typical limits at $V_{CC}$ = 5V, $T_C$ = +25°C, and Load A.
2. A pull-up resistor to $V_{CC}$ on the $\overline{CS}$ input is required to keep the device deselected; otherwise, power-on current approaches $I_{CC}$ active.

## CAPACITANCE $T_C$ = 25°C, F = 1.0 MHz

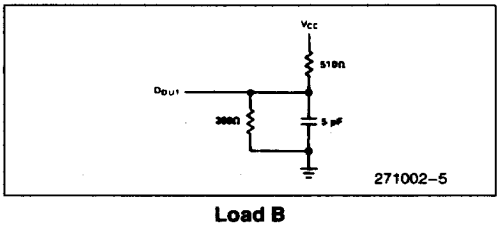
| Symbol | Parameter | Max | Unit | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 5 | pF | $V_{IN}$ = 0V |
| $C_{OUT}$ | Output Capacitance | 6 | pF | $V_{OUT}$ = 0V |

## A.C. TEST CONDITIONS

Input Pulse Levels . . . . . GND to 3.0V
Input Rise and Fall Times . . . . . 5 ns
Input Timing Reference Levels . . . . . 1.5V
Output Timing Reference Levels . . . . . 0.8V–2.0V
Output Load . . . . . See Load A




**Load A**




**Load B**

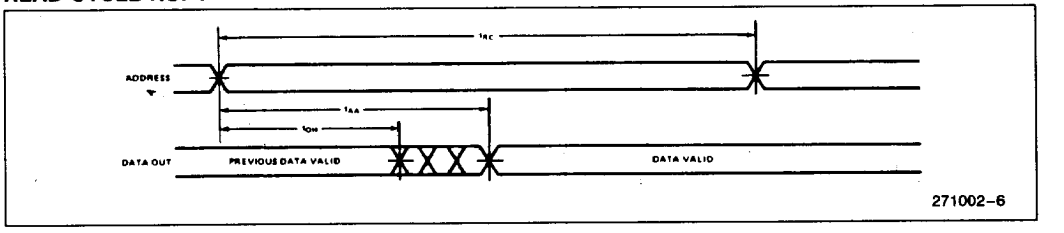
## A.C. CHARACTERISTICS (Over Specified Operating Conditions)

### READ CYCLE

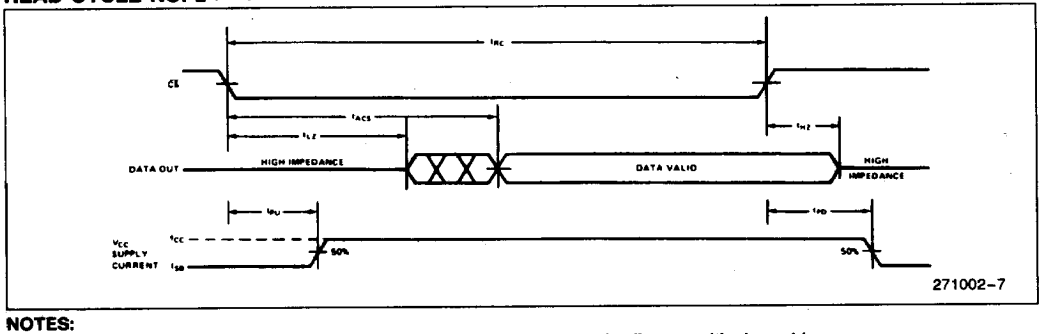
| Symbol | Parameter | M2147H-2 | | M2147H-3 | | M2147H | | Unit | Comments |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{RC}$(1) | Read Cycle Time | 45 | | 55 | | 70 | | ns | |
| $t_{AA}$ | Address Access Time | | 45 | | 55 | | 70 | ns | |
| $t_{ACS1}$ | Chip Select Access Time | | 45 | | 55 | | 70 | ns | (Note 7) |
| $t_{ACS2}$ | Chip Select Access Time | | 45 | | 65 | | 80 | ns | (Note 8) |
| $t_{OH}$ | Output Hold from Address Change | 5 | | 5 | | 5 | | ns | |
| $t_{LZ}$(2) | Chip Selection to Output in Low Z | 5 | | 10 | | 10 | | ns | (Note 3) |
| $t_{HZ}$(2) | Chip Deselection to Output in High Z | 0 | 30 | 0 | 30 | 0 | 40 | ns | (Note 3) |
| $t_{PU}$ | Chip Selection to Power Up Time | 0 | | 0 | | 0 | | ns | |
| $t_{PD}$ | Chip Deselection to Power Down Time | | 20 | | 20 | | 30 | ns | |

## WAVEFORMS

### READ CYCLE NO. 1(4, 5)




### READ CYCLE NO. 2 (4, 6)




**NOTES:**
1. All Read Cycle timings are referenced from the last valid address to the first transitioning address.
2. At any given temperature and voltage condition, $t_{HZ}$ max. is less than $t_{LZ}$ min. both for a given device and from device to device.
3. Transition is measured ±500 mV from steady state voltage with Load B.
4. $\overline{WE}$ is high for Read Cycles.
5. Device is continuously selected, $\overline{CS} = V_{IL}$.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
7. Chip deselected for greater than 55 ns prior to selection.
8. Chip deselected for a finite time that is less than 55 ns prior to selection. (If the deselect time is 0 ns, the chip is by definition selected and access occurs according to Read Cycle No. 1.)

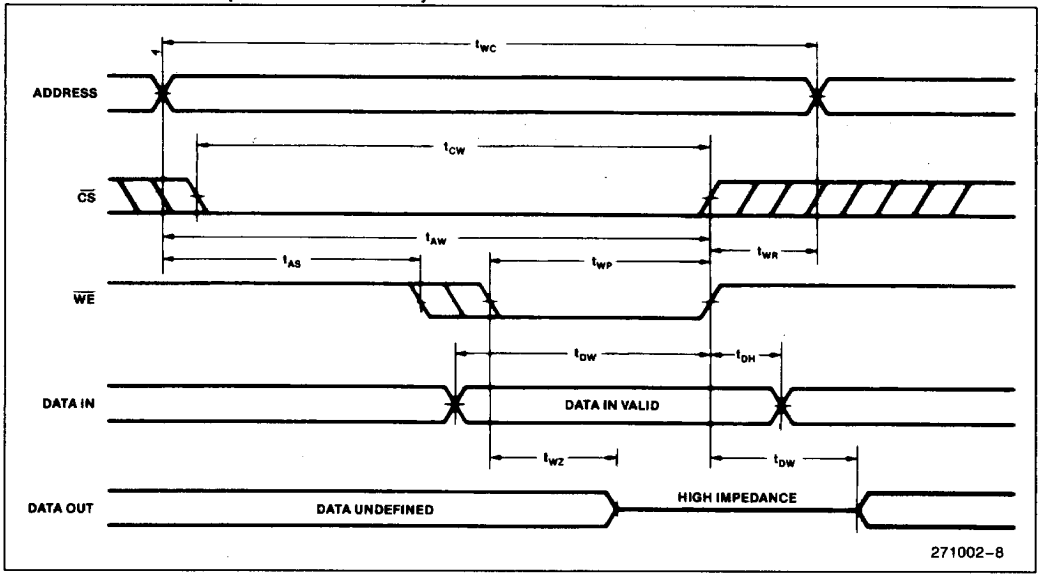
## A.C. CHARACTERISTICS (Continued)

### WRITE CYCLE

| Symbol | Parameter | M2147H-2 | | M2147H-3 | | M2147H | | Unit | Comments |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{WC}$[2] | Write Cycle Time | 45 | | 55 | | 70 | | ns | |
| $t_{CW}$ | Chip Selection to End of Write | 45 | | 45 | | 55 | | ns | |
| $t_{AW}$ | Address Valid to End of Write | 45 | | 45 | | 55 | | ns | |
| $t_{AS}$ | Address Setup Time | 0 | | 0 | | 0 | | ns | |
| $t_{WP}$ | Write Pulse Width | 25 | | 25 | | 40 | | ns | |
| $t_{WR}$ | Write Recovery Time | 0 | | 10 | | 15 | | ns | |
| $t_{DW}$ | Data Valid to End of Write | 25 | | 25 | | 30 | | ns | |
| $t_{DH}$ | Data Hold Time | 10 | | 10 | | 10 | | ns | |
| $t_{WZ}$ | Write Enable to Output in High Z | 0 | 25 | 0 | 25 | 0 | 35 | ns | (Note 3) |
| $t_{OW}$ | Ouput Active from End of Write | 0 | | 0 | | 0 | | ns | (Note 3) |

## WAVEFORMS

### WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED) [4]

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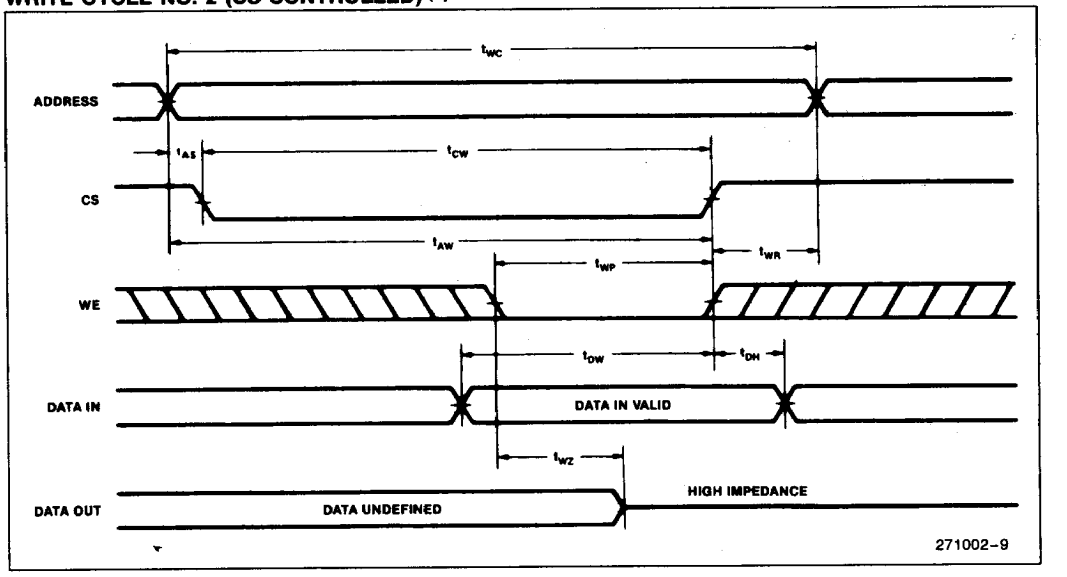
## WAVEFORMS (Continued)

### WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED) (4)




**NOTES:**
1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady state voltage with Load B.
4. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.