

Quad 2-port register w/true & complimentary outputs
Quad 2-port register

54F398
54F399

FEATURES

- Select inputs from two data sources
- Fully positive edge-triggered operation
- Both True and Complementary outputs – 54F398

DESCRIPTION

The 54F398 and 54F399 are the logical equivalent of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of the two 4-bit words is accepted. The selected data enters the flip-flops on the rising edge of the clock. The 54F399 is the 16-pin version of the 54F398, with only the Q outputs of the flip-flops available.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
20-Pin Ceramic DIP 16-Pin Ceramic DIP	54F398/BRA 54F399/BEA	GDIP1-T20 GDIP1-T16
20-Pin Ceramic Flat Pack 16-Pin Ceramic Flat Pack	54F398/BSA 54F399/BFA	GDFP2-F20 GDFP2-F16
20-Pin Ceramic LLCC	54F398/B2A 54F399/B2A	CQCC2-N20

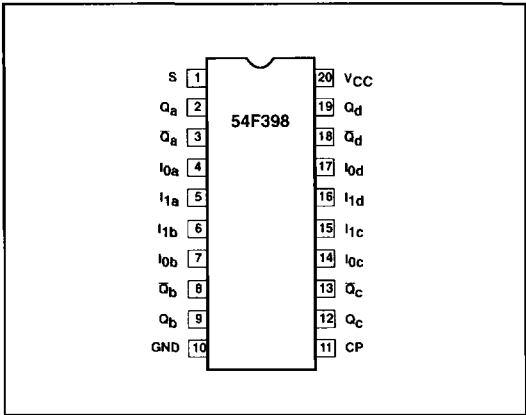
* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

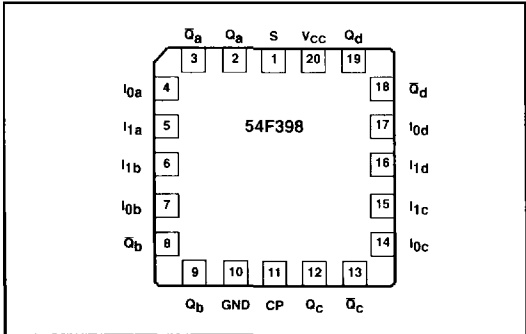
PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I _{0a} - I _{0d}	Data inputs from source 0	1.0/1.0	20μA/0.6mA
I _{1a} - I _{1d}	Data inputs from source 1	1.0/1.0	20μA/0.6mA
S	Common select input	1.0/1.0	20μA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
Q _a - Q _d	Register true outputs	50/33	1.0mA/20mA
$\bar{Q}_a$ - $\bar{Q}_d$	Register complementary outputs (54F398)	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

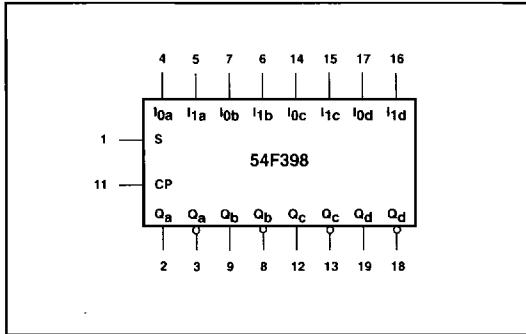
PIN CONFIGURATION



LLCC LEAD CONFIGURATION



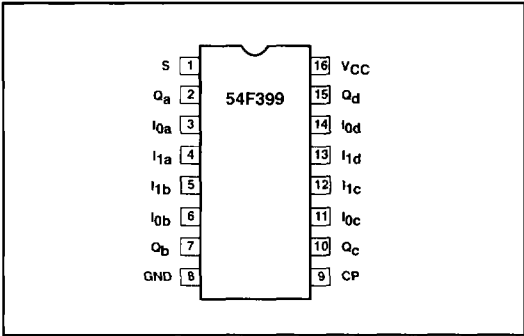
LOGIC SYMBOL



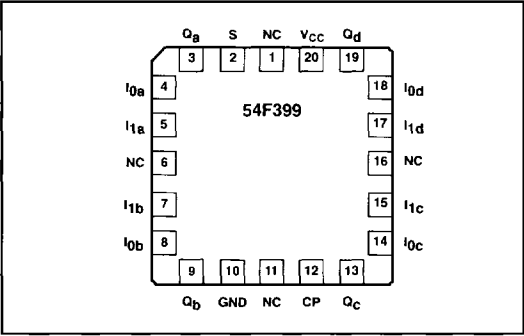
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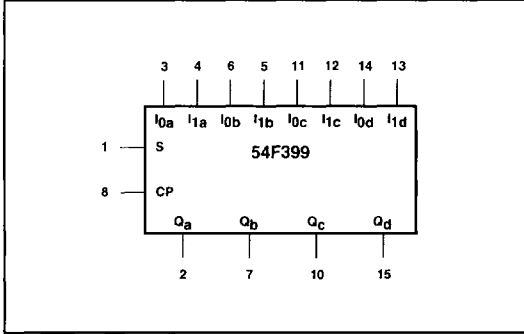
PIN CONFIGURATION



LLCC LEAD CONFIGURATION



LOGIC SYMBOL



The 54F398 and 54F399 are high-speed quad 2-port registers. They select 4 bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the Low-to-High transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I_{0x} , I_{1x}) and Select input (S) must be stable only a set-up time prior to and hold time after the Low-to-High transition of the Clock input for predictable operation. The 54F398 has both Q and $\bar{Q}$ outputs.

FUNCTION TABLE

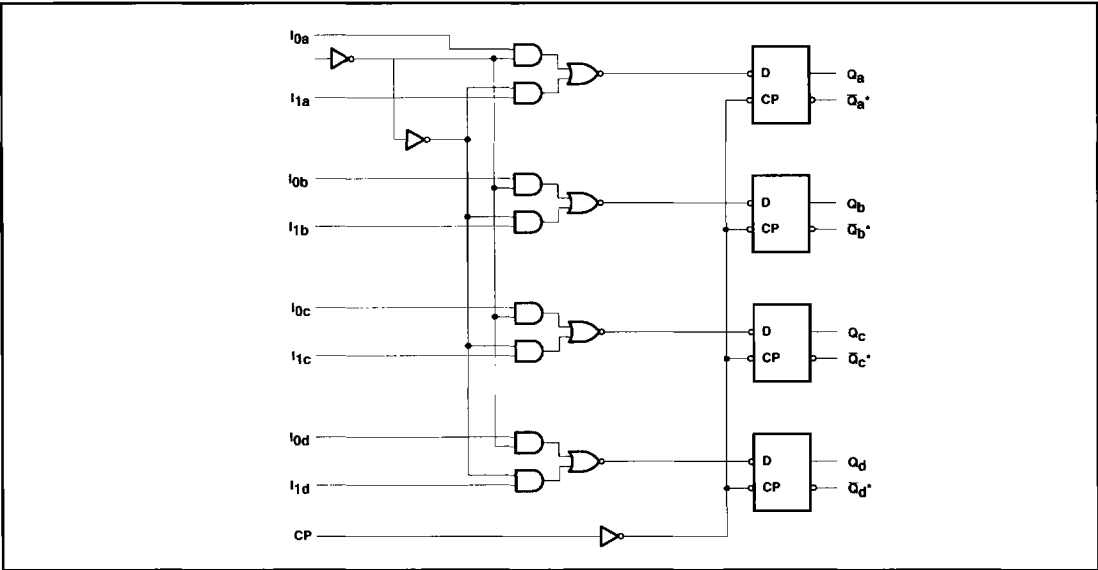
INPUTS			OUTPUTS	
S	I_0	I_1	Q	$\bar{Q}^*$
l	l	X	L	H
l	h	X	H	L
h	X	l	L	H
h	X	h	H	L

*54F398 only

- l = Low voltage level one setup time prior to Low-to-High clock transition
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level
H = High voltage level
X = Don't care

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LOGIC DIAGRAM (54F398 only)



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage range	-0.5 to +7.0	V
V _I	Input voltage range	-0.5 to +7.0	V
I _I	Input current range	-30 to +5	mA
V _O	Voltage applied to output in High output state range	-0.5 to +V _{CC}	V
I _O	Current applied to output in Low output state	40	mA
T _{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{IH}	High-level input voltage	2.0			V
V _{IL}	Low-level input voltage			0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	High-level output current			-1	mA
I _{OL}	Low-level output current			20	mA
T _A	Operating free-air temperature range	-55		+125	°C

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DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT
			Min	Typ ²	Max	
V _{OH}	High-level output voltage	V _{CC} = Min, V _{IL} = Max, I _{OH} = Max, V _{IH} = Min	2.5			V
V _{OL}	Low-level output voltage	V _{CC} = Min, V _{IL} = Max, I _{OL} = Max, V _{IH} = Min		0.35	0.50	V
V _{IK}	Input clamp voltage	V _{CC} = Min, I _I = I _{IK}		-0.73	-1.2	V
I _{IH2}	Input current at maximum input voltage	V _{CC} = Max, V _I = 7.0V			100	μA
I _{IH1}	High-level input current	V _{CC} = Max, V _I = 2.7V		1	20	μA
I _{IL}	Low-level input current	V _{CC} = Max, V _I = 0.5V		-0.4	-0.6	mA
I _{OS}	Short-circuit output current ³	V _{CC} = Max	-60		-150	mA
I _{CC}	Supply current ⁴ (total)	V _{CC} = Max		25	38	mA
				22	34	mA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			T _A = +25°C			T _A = -55°C to +125°C			
			V _{CC} = +5.0V			V _{CC} = +5.0V ± 10%			
			C _L = 50pF, R _L = 500Ω			C _L = 50pF, R _L = 500Ω			
			Min	Typ	Max	Min	Max		
t _{MAX}	Maximum clock frequency	Waveform 1	100	120		80 ⁵		MHz	
t _{PLH}	Propagation delay CP to Q or Q̄	Waveform 1	3.0	5.7	7.5	3.0	9.5	ns	
t _{PHL}			3.0	6.5	8.5	3.0	10.5	ns	

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			T _A = +25°C			T _A = -55°C to +125°C			
			V _{CC} = +5.0V			V _{CC} = +5.0V ± 10%			
			C _L = 50pF, R _L = 500Ω			C _L = 50pF, R _L = 500Ω			
			Min	Typ	Max	Min	Max		
t _s (H)	Set-up time, High or Low I _n to CP	Waveform 2	3.0			4.5		ns	
t _s (L)			3.0			4.5		ns	
t _h (H)	Hold time, High or Low I _n to CP	Waveform 2	1..0			1.5		ns	
t _h (L)			1.0			1.5		ns	
t _s (H)	Set-up time, High or Low S to CP	Waveform 2	7.5			10.5		ns	
t _s (L)			7.5			10.5		ns	
t _h (H)	Hold time, High or Low S to CP	Waveform 2	0			0		ns	
t _h (L)			0			0		ns	
t _w (H)	CP pulse width, High or Low	Waveform 1	4.0			4.0		ns	
t _w (L)			6.0			7.0		ns	

NOTES:

- For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS} the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests I_{OS} tests should be performed last.
- V_{IN} = High; apply 3V, 0V, 3V to CP then make measurement.
- These parameters are guaranteed, but not tested.

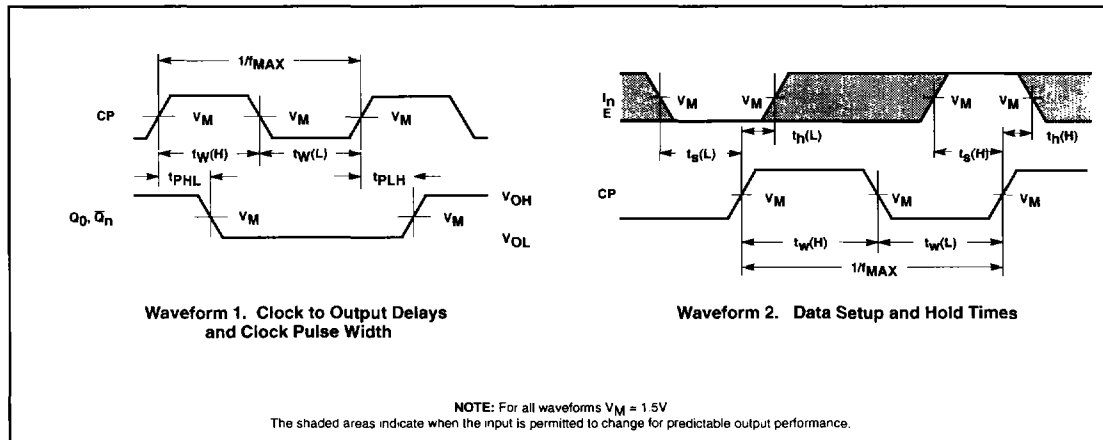
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AC WAVEFORMS



TEST CIRCUIT AND WAVEFORM

