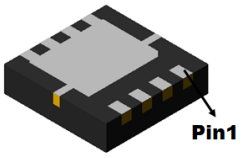
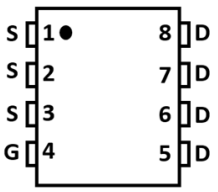
N-Channel Enhancement Mode Field Effect Transistor

RC50N03D3

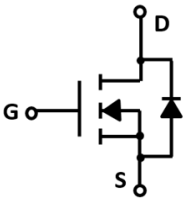
Product Summary

- V_{DS} 30V
- I_D 50A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜8．5 mΩ
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜1 3 mΩ





DFN3.3X3.3



General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation ● High density cell design for low $R_{DS(ON)}$

Applications

- High current load applications
- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	30	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_C=25℃	I_D	50	A
	T_C=100℃		35	
Pulsed Drain Current [A]		I_{DM}	190	A
Total Power Dissipation	T_C=25℃	P_D	42	W
	T_C=100℃		21	W
Single Pulse Avalanche Energy [B]		E_{AS}	225	mJ
Thermal Resistance Junction-to-Case [C]		$R_{\theta JC}$	3.6	℃/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+175	℃

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
RC50N03D3	F1	RC50N03	5000	10000	100000	13“ reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 10V, I_D=15A		7	8.5	mΩ
		V_{GS}= 4.5V, I_D=15A		10	13	
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V			1.2	V
Maximum Body-Diode Continuous Current	I_S				50	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=15V,V_{GS}=0V,f=1MHZ		2504		pF
Output Capacitance	C_{oss}			323		
Reverse Transfer Capacitance	C_{rss}			283		
Gate resistance	R_g	F= 1MHZ			3	Ω
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=15V,I_D=20A		54		nC
Gate-Source Charge	Q_{gs}			26		
Gate-Drain Charge	Q_{gd}			8.5		
Reverse Recovery Chrage	Q_{rr}	I_F=15A, di/dt=100A/us		10.2		
Reverse Recovery Time	t_{rr}			15		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DD}=20V, I_D=2A R_{GEN}=3Ω		11		
Turn-on Rise Time	t_r			20		
Turn-off Delay Time	$t_{D(off)}$			41		
Turn-off fall Time	t_f			25		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. $R_{\theta JA}$ is the sum of the junction-to-Case and Case-to-ambient thermal resistance, where the Case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ Typical Performance Characteristics

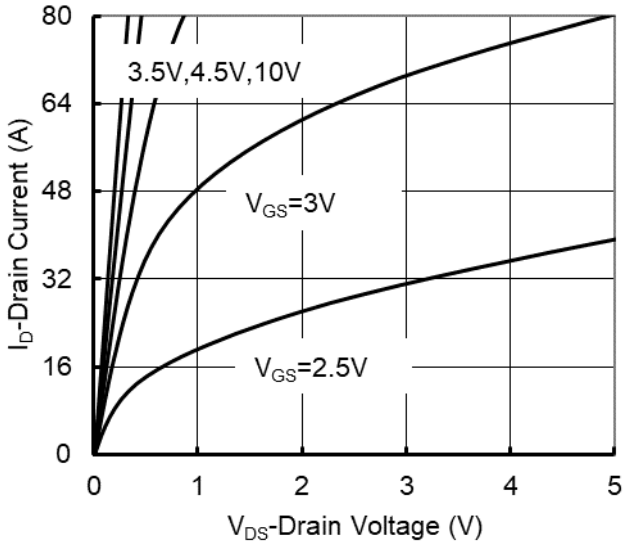


Figure1. Output Characteristics

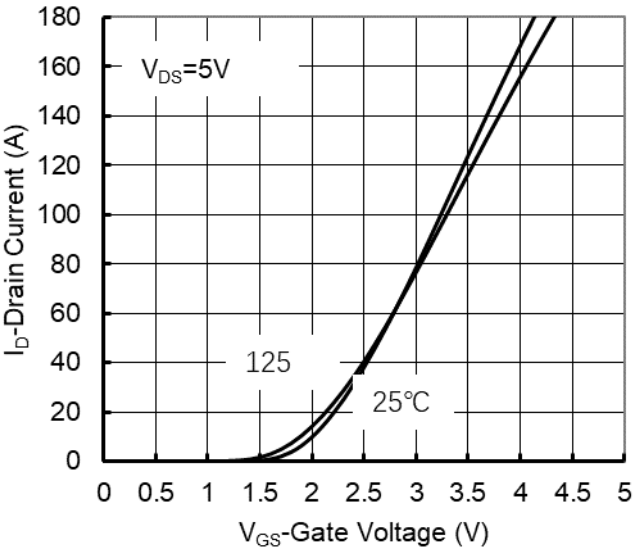


Figure2. Transfer Characteristics

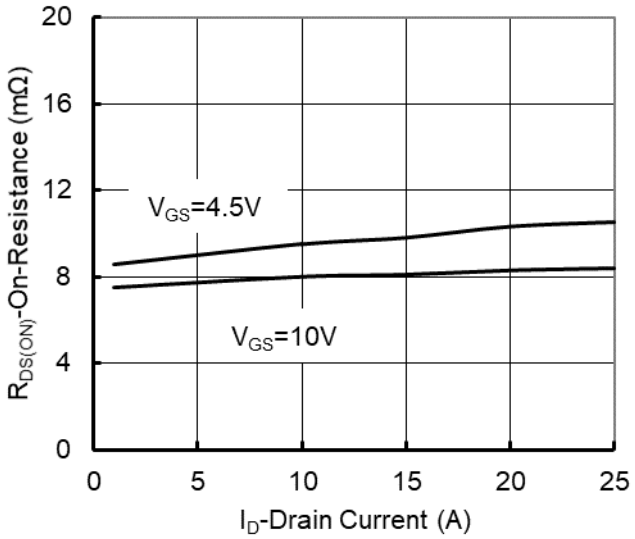


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

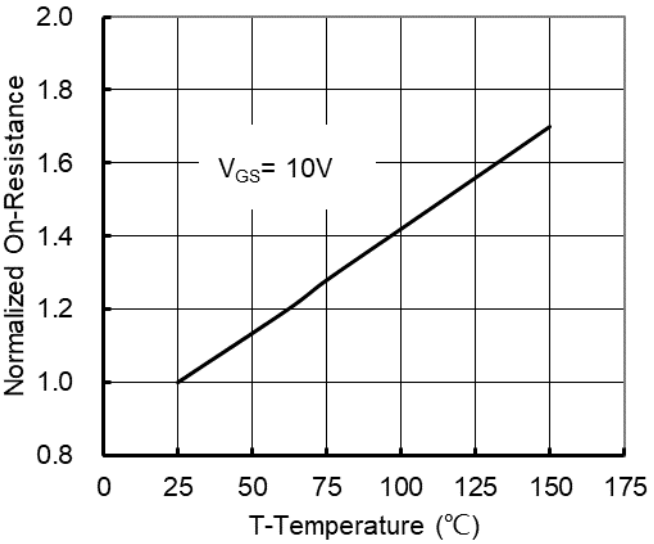


Figure 4: On-Resistance vs. Junction Temperature

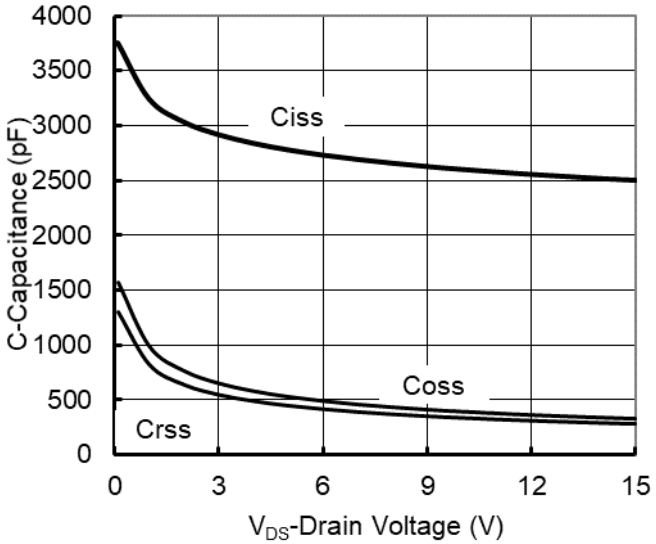


Figure5. Capacitance Characteristics

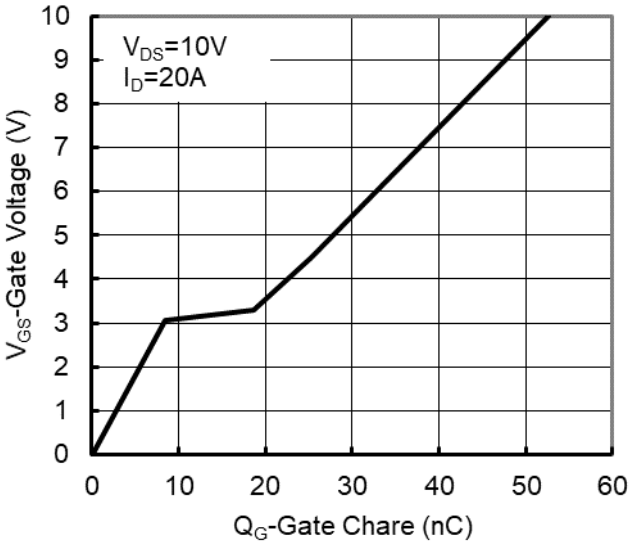


Figure6. Gate Charge

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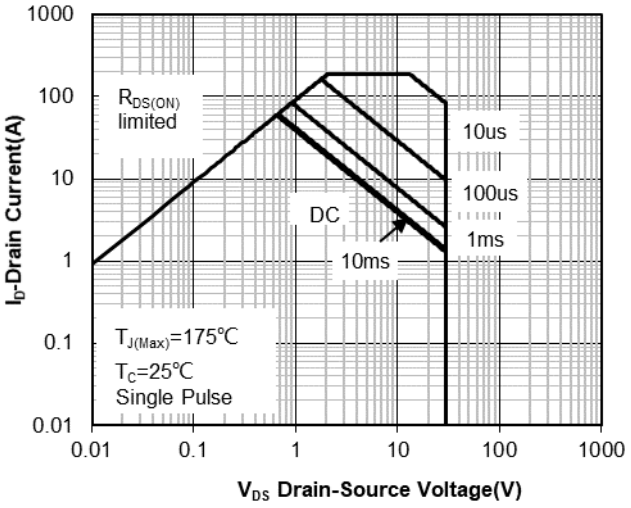

Figure7. Safe Operation Area

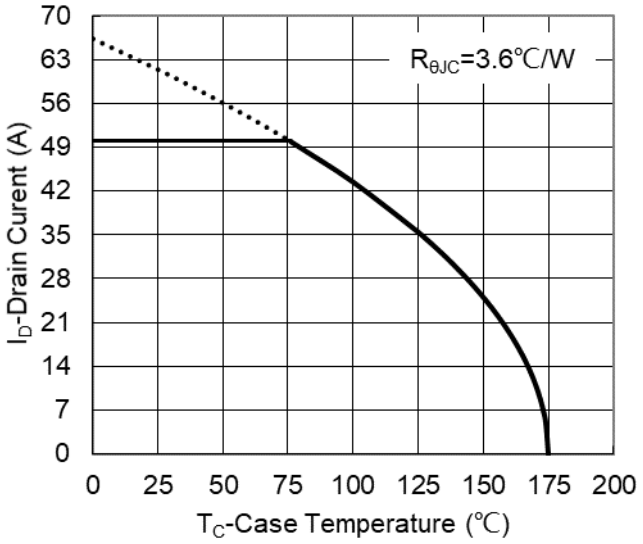

Figure8. Maximum Continuous Drain Current vs Case Temperature

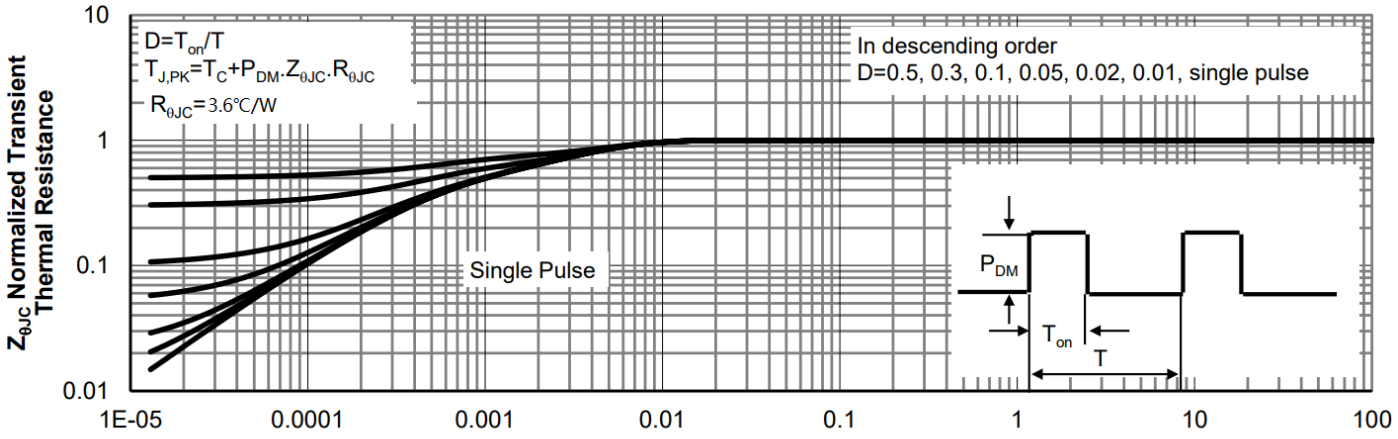

Figure9.Normalized Maximum Transient Thermal Impedance

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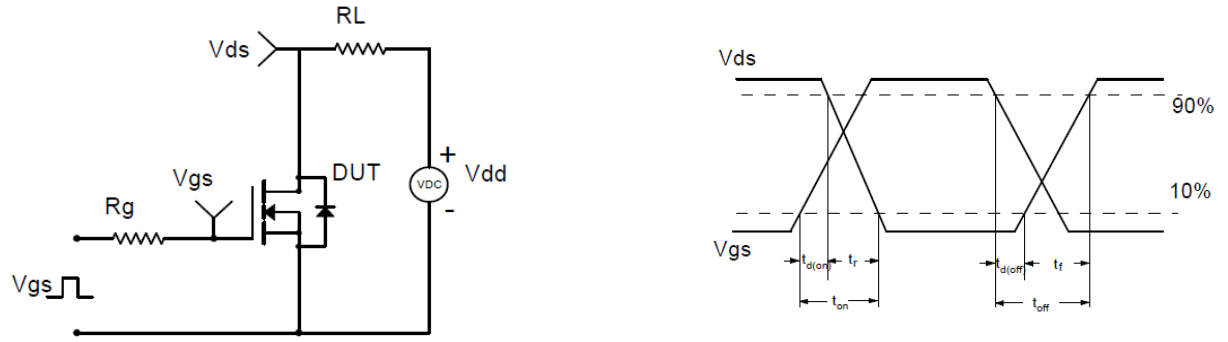
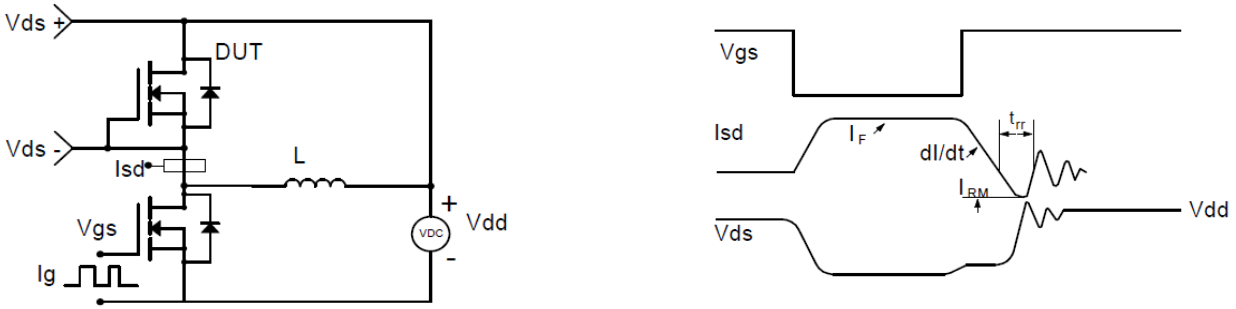
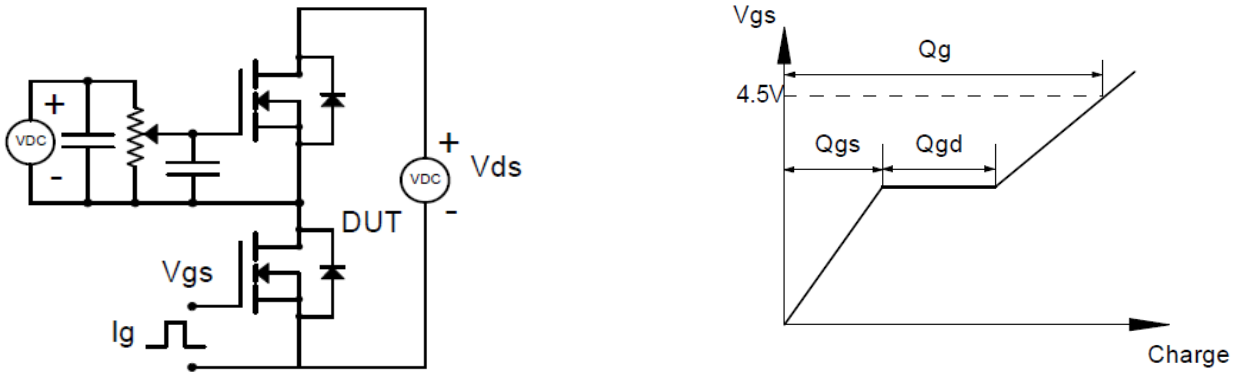


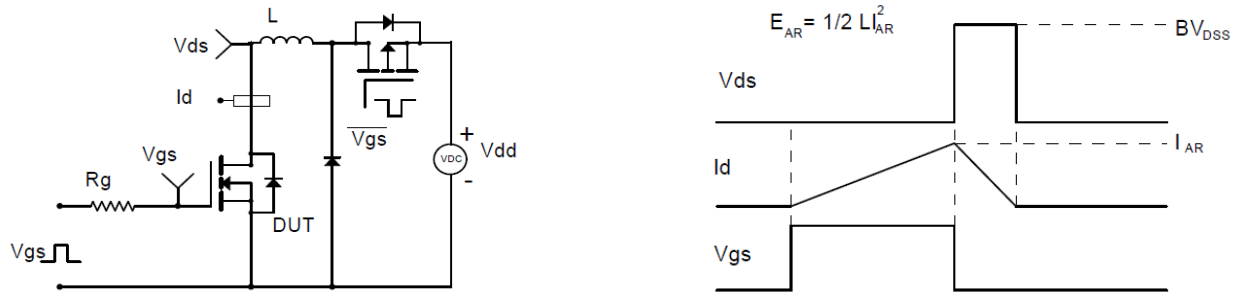
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

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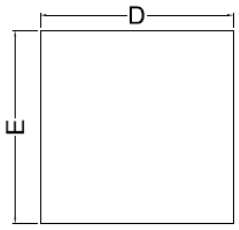
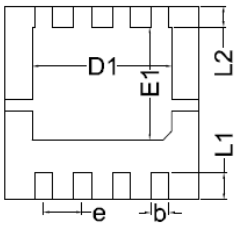
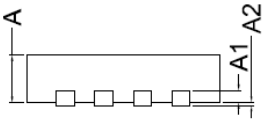
■DFN3.3X3.3 Package information



Top View
正面视图

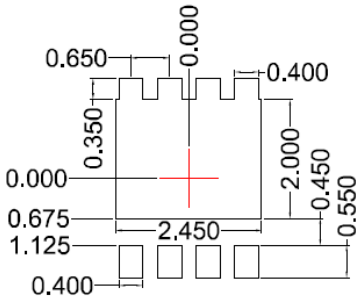


Bottom View
背面视图



Side View
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1		0.20 BSC	
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2		0.35 BSC	
b	0.20	0.30	0.40
e		0.65 BSC	



Suggested Solder Pad Layout
Top View

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.