1-MSPS/800-KSPS, 3.3V-5.25V, ULTRA LOW POWER, 12-/10-/8-BIT SAR ANALOG-TO-DIGITAL CONVERTER

FEATURES

- Single 3.3V to 4.8V Supply Operation for CI7476E/77E/78E
  Single 4V to 5.25V Supply Operation for CI 7476/77/78
- Fast Throughput Rate:
  1 MSPS for CI7476E/77E/78E
  800 KSPS for CI 7476/77/78
- ±1.25LSB INL, ±1.25LSB DNL (CI 7476)
- No Pipeline Delays
- SPI/DSP/MICROWIRE™/QSPI™ Compatible Serial Interface
- Variable Power Management
- Low Power (CI7476 Typical):
  3.4mW (4V, 800 KSPS)
  6.1mW (5V, 800 KSPS)
- Second-Source for ADCS7476/77/78
- 6-Pin SOT-23 Package

APPLICATIONS

- Battery Powered Systems
- Portable Systems
- Medical Instruments
- Mobile Communications
- Factory Automation and ATM Equipment
- Instrumentation and Control Systems

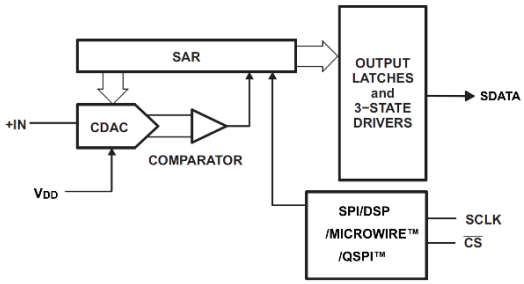


Figure 1. Functional Block Diagram

SPECIFICATIONS

At-40℃ to 85℃, f_{SAMPLE} = 1 MSPS and f_{SCLK} = 20 MHz if 3.3 V ≤ V_{DD} ≤ 4.8 V ; f_{SAMPLE} = 800 KSPS and f_{SCLK} = 16 MHz if 4 V ≤ V_{DD} ≤ 5.25 V . (unless otherwise noted)

PARAMETER	TEST CONDITIONS	CI7476/76E			CI7477/77E			CI7478/78E			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SYSTEM PERFORMANCE											
Resolution			**12**			**10**			**8**		Bits
No missing codes		**12**			**10**			**8**			Bits
Integral linearity		**-1.25**		**1.25**	**-1**		**1**	**-0.5**		**0.5**	LSB
Differential linearity		**-1.25**		**1.25**	**-1**		**1**	**-0.5**		**0.5**	LSB
f_{SAMPLE} Throughput rate	f_{SCLK} = 16 MHz, 4 V ≤ V_{DD} ≤ 5.25 V			**800**			**800**			**800**	KSPS
	f_{SCLK} = 20 MHz, 3.3 V ≤ V_{DD} ≤ 4.8 V			**1**			**1**			**1**	MSPS
SNR	f_{IN} = 100 kHz		**71.5**			**61**			**49**		dB
THD	f_{IN} = 100 kHz		**-84**			**-74**			**-68**		dB

CI7476

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{DD} Supply current, normal operation	Digital inputs = 0 V or V_{DD}	f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 4 V		**0.85**	**0.97**	mA
		f_{SAMPLE} =800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 5 V		**1.22**	**1.34**	
		f_{SAMPLE} = 500 KSPS, f_{SCLK} = 10 MHz, V_{DD} = 4 V		**0.48**	**0.58**	
		f_{SAMPLE} = 500 KSPS, f_{SCLK} = 10 MHz, V_{DD} = 5 V		**0.80**	**0.90**	
POWER DISSIPATION, CI7476						
Normal operation		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 4 V		**3.4**	**3.9**	mW
		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 5 V		**6.1**	**6.7**	mW

CI7477

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{DD} Supply current, normal operation	Digital inputs = 0 V or V_{DD}	f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 4 V		**0.75**	**0.87**	mA
		f_{SAMPLE} =800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 5 V		**1.04**	**1.18**	
		f_{SAMPLE} = 500 KSPS, f_{SCLK} = 10 MHz, V_{DD} = 4 V		**0.45**	**0.55**	
		f_{SAMPLE} = 500 KSPS, f_{SCLK} = 10 MHz, V_{DD} = 5 V		**0.75**	**0.80**	
POWER DISSIPATION, CI7477						
Normal operation		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 4 V		**3.00**	**3.50**	mW
		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 5 V		**5.20**	**5.90**	mW

CI7478

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{DD} Supply current, normal operation	Digital inputs = 0 V or V_{DD}	f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 4 V		**0.70**	**0.80**	mA
		f_{SAMPLE} =800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 5 V		**0.96**	**1.08**	
		f_{SAMPLE} = 500 KSPS, f_{SCLK} = 10 MHz, V_{DD} = 4 V		**0.40**	**0.50**	
		f_{SAMPLE} = 500 KSPS, f_{SCLK} = 10 MHz, V_{DD} = 5 V		**0.68**	**0.78**	
POWER DISSIPATION, CI7477						
Normal operation		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 4 V		**2.80**	**3.20**	mW
		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 5 V		**4.80**	**5.40**	mW

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

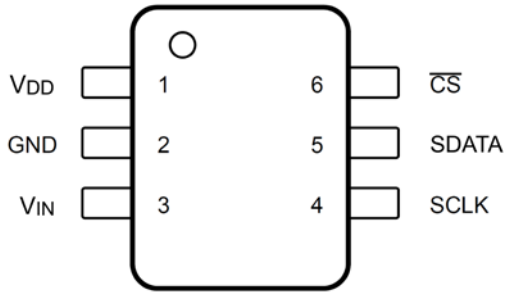


Figure 2. Pin Configuration

TERMINAL		DESCRIPTION
NAME	NO.	
V_{DD}	1	Power Supply Input.
GND	2	The ground return for the supply and signals.
V_{IN}	3	Analog Input. This signal can range from 0 V to V_{DD}.
SCLK	4	Digital clock input. This clock directly controls the conversion and readout processes.
SDATA	5	Digital data output. The output samples are clocked out of this pin on falling edges of the SCLK pin.
$\overline{CS}$	6	Chip Select. On the falling edge of $\overline{CS}$, a conversion process begins.

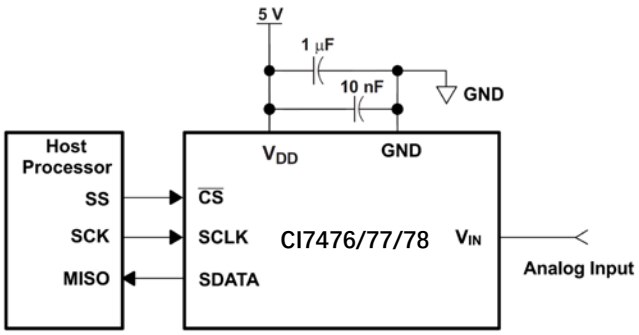


Figure 3. Typical Circuit Configuration

TIMING DIAGRAM

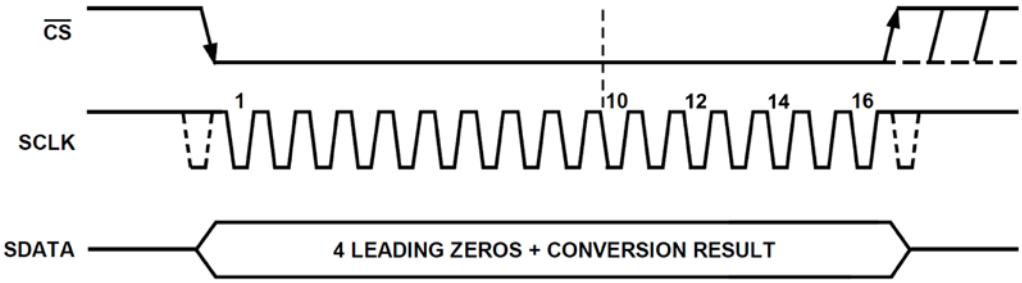
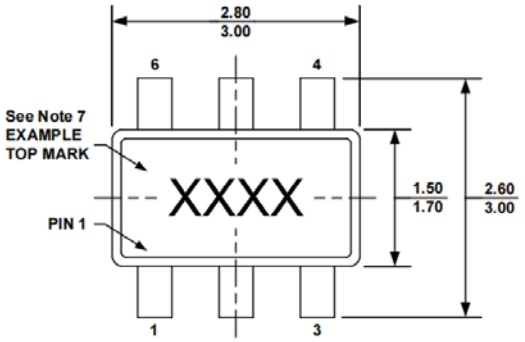
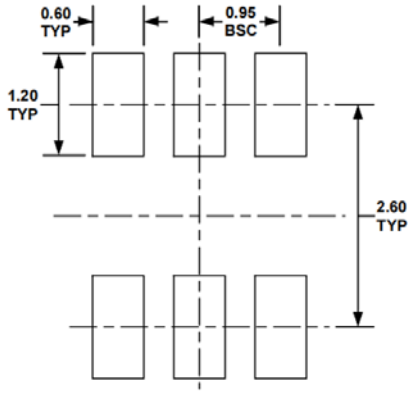


Figure 4. Timing Diagram

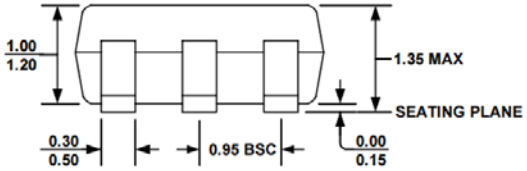
OUTLINE DIMENTIONS



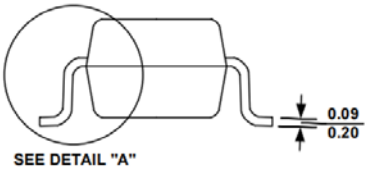
TOP VIEW



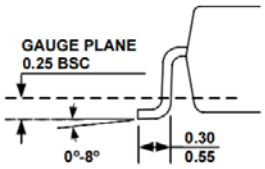
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-178, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)