Enhanced ESD, 1.5 kV rms 200Mbps Dual-Channel Digital Isolators

Data Sheet

π120E1/π122E1

FEATURES

- **Ultra-low power consumption (1Mbps): 0.58mA/Channel**
- **High data rate: 200Mbps**
- **High common-mode transient immunity: 75 kV/μs typical**
- **High robustness to radiated and conducted noise**
- **Low propagation delay:**
  - **8 ns typical for 5 V operation**
  - **9 ns typical for 3.3 V operation**
- **Isolation voltages:**
  - **π12xM1x: AC 1500Vrms**
- **High ESD rating:**
  - **ESDA/JEDEC JS-001-2017**
  - **Human body model (HBM) ±8kV**
- **CQC certification per GB4943.1-2011（CQC20001260210）**
- **3 V to 5.5 V level translation**
- **Wide temperature range: -40°C to 125°C**
- **8-PIN, RoHS-compliant, DFN Package(3mm*2mm)**

APPLICATIONS

- **General-purpose multichannel isolation**
- **Industrial field bus**
- **Isolation Industrial automation systems**
- **Isolated switch mode supplies**
- **Isolated ADC, DAC**
- **Motor control**

GENERAL DESCRIPTION

The π1xxxxx is a 2PaiSemi digital isolators product family that includes over hundreds of digital isolator products. By using maturated standard semiconductor CMOS technology and 2PaiSEMI ***iDivider®*** technology, these isolation components provide outstanding performance characteristics and reliability superior to alternatives such as optocoupler devices and other integrated isolators.

Intelligent voltage divider technology (***iDivider®*** technology) is a new generation digital isolator technology invented by 2PaiSEMI. It uses the principle of capacitor voltage divider to transmit voltage signal directly cross the isolator capacitor without signal modulation and demodulation.

The π1xxxxx isolator data channels are independent and are available in a variety of configurations with a withstand voltage rating of 1.5 kV rms to 6.0 kV rms and the data rate from DC up to 600Mbps (see the Ordering Guide). The devices operate with the supply voltage on either side ranging from 3.0 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier. The fail-safe state is available in which the outputs transition to a preset state when the input power supply is not applied.

FUNCTIONAL BLOCK DIAGRAMS

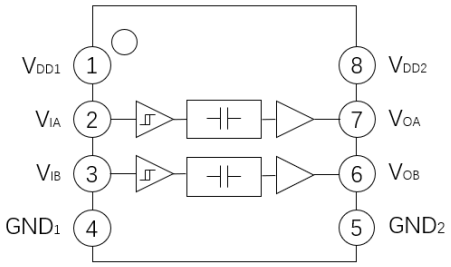

Figure 1.π120E1x functional Block Diagram

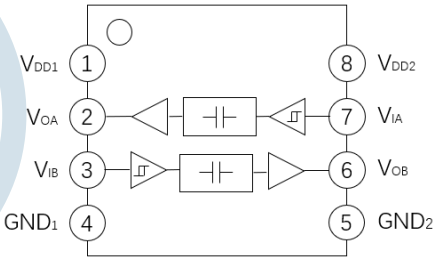

Figure 2.π122E1x functional Block Diagram

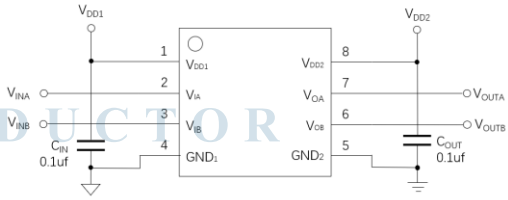

Figure 3.π120E1x Typical Application Circuit

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http://www.rpsemi.com/

PIN CONFIGURATIONS AND FUNCTIONS

Table 1.π120E1x Pin Function Descriptions

Pin No.	Name	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_{IA}	Logic Input A.
3	V_{IB}	Logic Input B.
4	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
5	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
6	V_{OB}	Logic Output B.
7	V_{OA}	Logic Output A.
8	V_{DD2}	Supply Voltage for Isolator Side 2.

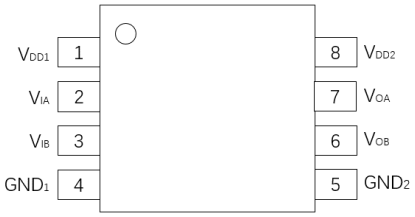


Figure 4.π120E1x Pin Configuration

Table 2.π122E1x Pin Function Descriptions

Pin No.	Name	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_{OA}	Logic Output A.
3	V_{IB}	Logic Input B.
4	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
5	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
6	V_{OB}	Logic Output B.
7	V_{IA}	Logic Input A.
8	V_{DD2}	Supply Voltage for Isolator Side 2.

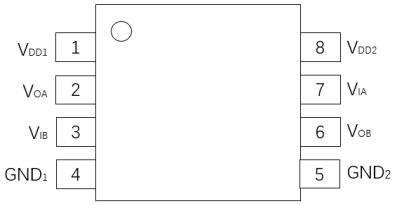


Figure 5.π122E1x Pin Configuration

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.Absolute Maximum Ratings[3]

Parameter	Rating
Supply Voltages (V_{DD1}-GND_1, V_{DD2}-GND_2)	−0.5 V ~ +7.0 V
Input Voltages (V_{IA}, V_{IB})[1]	−0.5 V ~ V_{DDx} + 0.5 V
Output Voltages (V_{OA}, V_{OB})[1]	−0.5 V ~ V_{DDx} + 0.5 V
Average Output Current per Pin Side 1 Output Current (I_{O1})	−10 mA ~ +10 mA
Average Output Current per Pin Side 2 Output Current (I_{O2})	−10 mA ~ +10 mA
Common-Mode Transients Immunity [2]	−200 kV/μs ~ +200 kV/μs
Storage Temperature (T_{ST}) Range	−65°C ~ +150°C
Ambient Operating Temperature (T_A) Range	−40°C ~ +125°C

Notes:

[1] V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.

[2]See Figure 12 for Common-mode transient immunity (CMTI) measurement.

[3] Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

RECOMMENDED OPERATING CONDITIONS

Table 4.Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DDx} [1]	3		5.5	V
High Level Input Signal Voltage	V_{IH}	0.7*V_{DDx}[1]		V_{DDx}[1]	V
Low Level Input Signal Voltage	V_{IL}	0		0.3*V_{DDx}[1]	V
High Level Output Current	I_{OH}	-6			mA
Low Level Output Current	I_{OL}			6	mA
Data Rate		0		200	Mbps
Junction Temperature	T_J	-40		150	°C
Ambient Operating Temperature	T_A	-40		125	°C

Notes:
[1] V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.

Truth Tables

Table 5.π120E1x/π122E1x Truth Table

V_{Ix} Input[1]	V_{DDI} State[1]	V_{DDO} State[1]	Default Low V_{Ox} Output[1]	Default High V_{Ox} Output[1]	Test Conditions /Comments
Low	Powered[2]	Powered[2]	Low	Low	Normal operation
High	Powered[2]	Powered[2]	High	High	Normal operation
Open	Powered[2]	Powered[2]	Low	High	Default output
Don't Care[4]	Unpowered[3]	Powered[2]	Low	High	Default output[5]
Don't Care[4]	Powered[2]	Unpowered[3]	High Impedance	High Impedance	

Notes:
[1] V_{Ix}/V_{Ox} are the input/output signals of a given channel (A or B). V_{DDI}/V_{DDO} are the supply voltages on the input/output signal sides of this given channel.
[2] Powered means V_{DDx}≥ 2.95 V
[3] Unpowered means V_{DDx} < 2.30V
[4] Input signal (V_{Ix}) must be in a low state to avoid powering the given V_{DDI}[1] through its ESD protection circuitry.
[5] If the V_{DDI} goes into unpowered status, the channel outputs the default logic signal after around 1us. If the V_{DDI} goes into powered status, the channel outputs the input status logic signal after around 1us.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Table 6.Switching Specifications

V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC}±10% or 5V_{DC}±10%, T_A=25°C, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Minimum Pulse Width	PW			5	ns	Within pulse width distortion (PWD) limit
Maximum Data Rate		200			Mbps	Within PWD limit
Propagation Delay Time[1]	t_{pHL}, t_{pLH}	5.5	8	12.5	ns	5V_{DC} supply
		6.5	9	13.5	ns	3.3V_{DC} supply
Pulse Width Distortion	PWD	0	0.3	3.0	ns	The max different time between t_{pHL} and t_{pLH}@ 5V_{DC} supply. And The value is | t_{pHL} - t_{pLH} |
		0	0.3	3.0	ns	@ 3.3V_{DC} supply
Channel to Channel Propagation Delay Skew	t_{CSK}		0	1.8	ns	The max amount propagation delay time differs between any two output channels in the single device @ 5V_{DC} supply.
			0	2	ns	@ 3.3V_{DC} supply

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Output Signal Rise/Fall Time [4]	t_r/t_f		1.5		ns	See Figure 8.
Rated Dielectric Insulation Voltage	V_{ISO}	1.5			kV rms	1-minute duration
Common-Mode Transient Immunity[3]	CMTI		75		kV/μs	V_{IN} = V_{DDx}[2] or 0V, V_{CM} = 1000 V.
ESD（HBM - Human body model）	ESD		±8		kV	

Notes:

[1] t_{pLH} = low-to-high propagation delay time, t_{pHL} = high-to-low propagation delay time. See Figure 9.

[2] V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.

[3] See Figure 12 for Common-mode transient immunity (CMTI) measurement.

[4] t_r means is the time from 10% amplitude to 90% amplitude of the rising edge of the signal， t_f means is the time from 90% amplitude to 10% amplitude of the falling edge of the signal.

Table 7.DC Specifications

V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC}±10% or 5V_{DC}±10%, T_A=25°C, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Rising Input Signal Voltage Threshold	V_{IT+}		0.6*V_{DDx}[1]	0.7*V_{DDx}[1]	V	
Falling Input Signal Voltage Threshold	V_{IT-}	0.3* V_{DDX}[1]	0.4* V_{DDX}[1]		V	
High Level Output Voltage	V_{OH} [1]	V_{DDx} – 0.1	V_{DDx}		V	−20 μA output current
		V_{DDx} – 0.2	V_{DDx} – 0.1		V	−2 mA output current
Low Level Output Voltage	V_{OL}		0	0.1	V	20 μA output current
			0.1	0.2	V	2 mA output current
Input Current per Signal Channel	I_{IN}	−10	0.5	10	μA	0 V ≤ Signal voltage ≤ V_{DDx}[1]
V_{DDx}[1] Undervoltage Rising Threshold	V_{DDxUV+}	2.45	2.75	2.95	V	
V_{DDx}[1] Undervoltage Falling Threshold	V_{DDxUV-}	2.30	2.60	2.75	V	
V_{DDx}[1] Hysteresis	V_{DDxUVH}		0.15		V	

Notes:

[1] V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.

Table 8.Quiescent Supply Current

V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC}±10% or 5V_{DC}±10%, T_A=25°C, C_L = 0 pF, unless otherwise noted.

Part	Symbol	Min	Typ	Max	Unit	Test Conditions	
						Supply voltage	Input signal
π120E1x	$I_{DD1 (Q)}$	0.06	0.08	0.10	mA	5V_{DC}	VI=0V for π12xEx0
	$I_{DD2 (Q)}$	0.78	0.98	1.27	mA		VI=5V for π12xEx1
	$I_{DD1 (Q)}$	0.16	0.20	0.26	mA		VI=5V for π12xEx0
	$I_{DD2 (Q)}$	0.74	0.92	1.20	mA		VI=0V for π12xEx1
	$I_{DD1 (Q)}$	0.06	0.08	0.10	mA	3.3V_{DC}	VI=0V for π12xEx0
	$I_{DD2 (Q)}$	0.77	0.97	1.26	mA		VI=3.3V for π12xEx1
	$I_{DD1 (Q)}$	0.12	0.15	0.19	mA		VI=3.3V for π12xEx0
	$I_{DD2 (Q)}$	0.71	0.89	1.15	mA		VI=0V for π12xEx1
π122E1x	$I_{DD1 (Q)}$	0.42	0.52	0.68	mA	5V_{DC}	VI=0V for π12xEx0

Part	Symbol	Min	Typ	Max	Unit	Test Conditions	
						Supply voltage	Input signal
	$I_{DD2\,(Q)}$	0.42	0.52	0.68	mA		VI=5V for π12xEx1
	$I_{DD1\,(Q)}$	0.44	0.55	0.71	mA		VI=5V for π12xEx0
	$I_{DD2\,(Q)}$	0.44	0.55	0.71	mA		VI=0V for π12xEx1
	$I_{DD1\,(Q)}$	0.41	0.52	0.67	mA	3.3V_{DC}	VI=0V for π12xEx0
	$I_{DD2\,(Q)}$	0.41	0.52	0.67	mA		VI=3.3V for π12xEx1
	$I_{DD1\,(Q)}$	0.41	0.51	0.66	mA		VI=3.3V for π12xEx0
	$I_{DD2\,(Q)}$	0.41	0.51	0.66	mA		VI=0V for π12xEx1

Table 9.Total Supply Current vs. Data Throughput (CL = 0 pF)

V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC}±10% or 5V_{DC}±10%, T_A=25°C, C_L = 0 pF, unless otherwise noted.

Part	Symbol	2 Mbps			20 Mbps			200 Mbps			Unit	Supply voltage
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
π120E1x	I_{DD1}		0.23	0.36		0.48	0.77		3.72	5.95	mA	5V_{DC}
	I_{DD2}		1.12	1.80		2.64	4.22		17.20	27.52		
	I_{DD1}		0.16	0.25		0.36	0.58		2.16	3.46	mA	3.3V_{DC}
	I_{DD2}		1.07	1.71		2.15	3.43		11.14	17.82		
π122E1x	I_{DD1}		0.64	1.02		1.94	3.10		10.40	16.64	mA	5V_{DC}
	I_{DD2}		0.64	1.02		1.94	3.10		10.40	16.64		
	I_{DD1}		0.59	0.95		1.54	2.46		6.58	10.53	mA	3.3V_{DC}
	I_{DD2}		0.59	0.95		1.54	2.46		6.58	10.53		

PACKAGE CHARACTERISTICS

Table 10.Package Characteristics

Parameter	Symbol	Typical Value	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{IO}	10^{11}	Ω	
Capacitance (Input to Output)[1]	C_{IO}	0.6	pF	@1MHz
Input Capacitance[2]	C_I	3	pF	@1MHz
IC Junction to Ambient Thermal Resistance	θ_{JA}	100	°C/W	Thermocouple located at center of package underside

Notes:

[1]The device is considered a 2-terminal device; DFN Pin 1 - Pin 4 are shorted together as the one terminal, and DFN Pin 5 - Pin 8 are shorted together as the other terminal.

[2]Testing from the input signal pin to ground.

Typical Thermal Characteristic

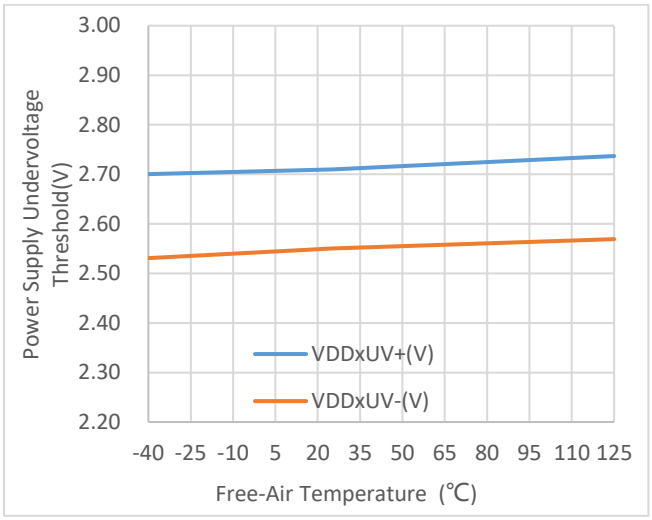


Figure 6.UVLO vs. Free-Air Temperature

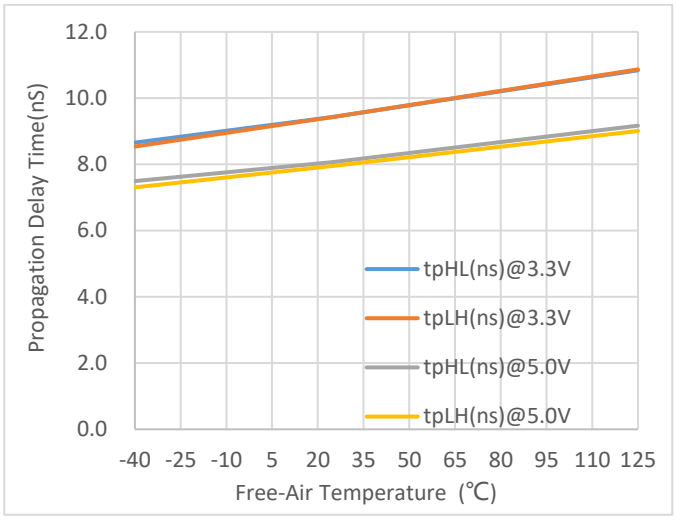


Figure 7.Propagation Delay Time vs. Free-Air Temperature

Timing test information

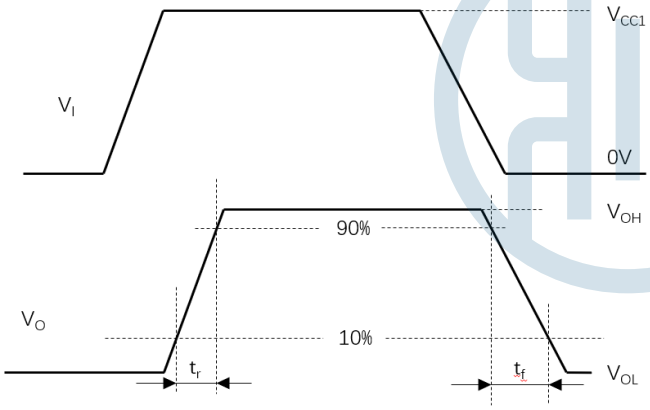


Figure 8.Transition time waveform measurement

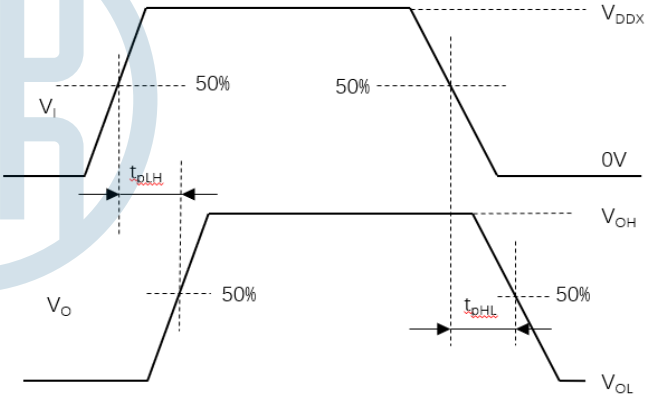


Figure 9.Propagation delay time waveform measurement

APPLICATIONS INFORMATION

OVERVIEW

The π1xxxxx are 2PaiSemi digital isolators product family based on 2PaiSEMI unique ***iDivider®*** technology. Intelligent voltage **Divider** technology (***iDivider®*** technology) is a new generation digital isolator technology invented by 2PaiSEMI. It uses the principle of capacitor voltage divider to transmit signal directly cross the isolator capacitor without signal modulation and demodulation. Compare to the traditional Opto-couple technology, icoupler technology, OOK technology, ***iDivider®*** is a more essential and concise isolation signal transmit technology which leads to greatly simplification on circuit design and therefore significantly improves device performance, such as lower power consumption, faster speed, enhanced anti-interference ability, lower noise.

By using maturated standard semiconductor CMOS technology and the innovative ***iDivider®*** design, these isolation components provide outstanding performance characteristics and reliability superior to alternatives such as optocoupler devices and other integrated isolators. The π1xxxxx isolator data channels are independent and are available in a variety of configurations with a withstand voltage rating of 1.5 kV rms to 6.0 kV rms and the data rate from DC up to 600Mbps (see the Ordering Guide).

The π120E1x/π122E1x are the outstanding 200 Mbps dual-channel digital isolators with the enhanced ESD capability. the devices transmit data across an isolation barrier by layers of silicon dioxide isolation.

The devices operate with the supply voltage on either side ranging from 3.0 V to 5.5 V, offering voltage translation of 3.3 V and 5 V logic. The π120E1x/π122E1x have very low propagation delay and high speed. The input/output design techniques allow logic and supply voltages over a wide range from 3.0 V to 5.5 V, offering voltage translation of 3.3 V and 5 V logic. The architecture is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference.

See the Ordering Guide for the model numbers that have the fail-safe output state of low or high.

PCB LAYOUT

The low-ESR ceramic bypass capacitors must be connected between V_{DD1} and GND_1 and between V_{DD2} and GND_2. The bypass capacitors are placed on the PCB as close to the isolator device as possible. The recommended bypass capacitor value is between 0.1 µF and 10 µF. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy.

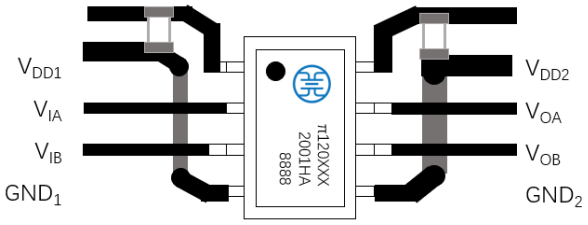


Figure 10.Recommended Printed Circuit Board Layout

Avoid reducing the isolation capability, Keep the space underneath the isolator device free from metal such as planes, pads, traces and vias.

To minimize the impedance of the signal return loop, keep the solid ground plane directly underneath the high-speed signal path, the closer the better. The return path will couple between the nearest ground plane to the signal path. Keep suitable trace width for controlled impedance transmission lines interconnect.

To reduce the rise time degradation, keep the length of input/output signal traces as short as possible, and route low inductance loop for the signal path and It's return path.

JITTER MEASUREMENT

The eye diagram shown in the figure below provides the jitter measurement result for the π120E1/π122E1. The Keysight 81160A pulse function arbitrary generator works as the data source for the π120E1/π122E1, which generates 100Mbps pseudo random bit sequence (PRBS). The Keysight DSOS104A digital storage oscilloscope captures the π120E1/π122E1 output waveform and recoveries the eye diagram with the SDA jitter tools and eye diagram analysis tools. The result shows a typical measurement jitter data.

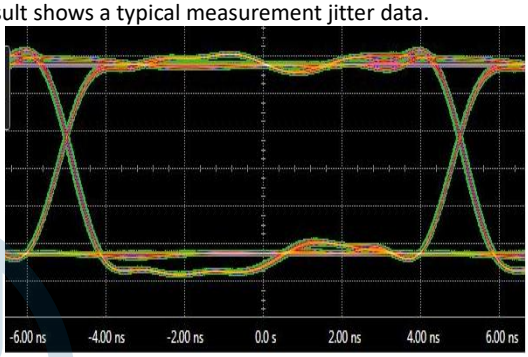


Figure 11.π120Exx/π122Exx Eye Diagram

CMTI MEASUREMENT

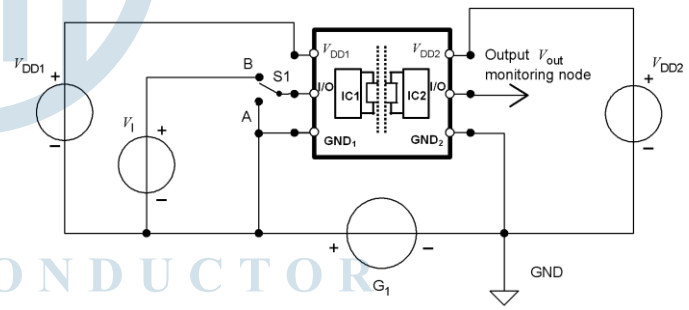
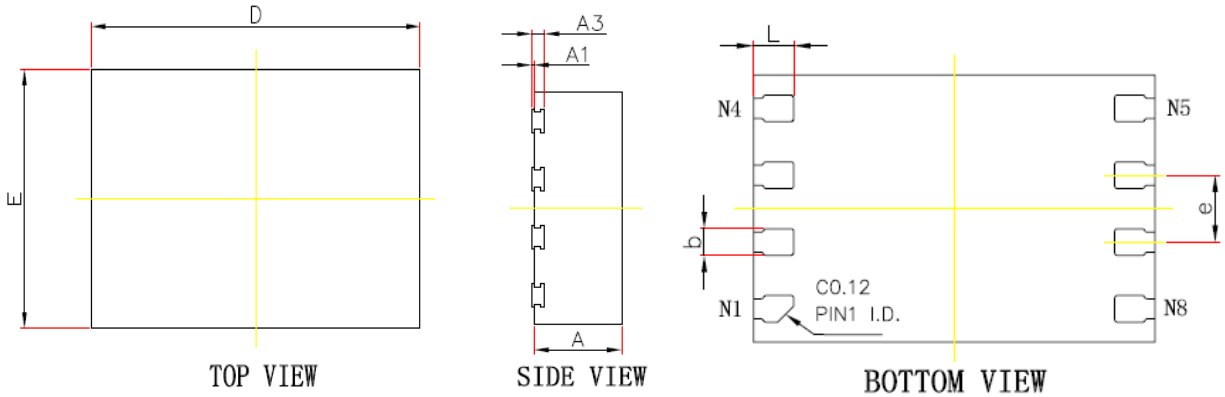


Figure 12.Common-mode transient immunity (CMTI) measurement

To measure the Common-Mode Transient Immunity (CMTI) of π1xxxxx isolator under specified common-mode pulse magnitude (VCM) and specified slew rate of the common-mode pulse (dVCM/dt) and other specified test or ambient conditions, The common-mode pulse generator (G1) will be capable of providing fast rise and fall pulses of specified magnitude and duration of the common-mode pulse (VCM),such that the maximum common-mode slew rates (dVCM/dt) can be applied to π1xxxxx isolator coupler under measurement. The common-mode pulse is applied between one side ground GND1 and the other side ground GND2 of π1xxxxx isolator, and shall be capable of providing positive transients as well as negative transients.

OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	-0.004	0.046	0.000	0.002
A3	0.110REF.		0.004REF.	
D	2.900	3.100	0.114	0.122
E	1.900	2.100	0.075	0.083
b	0.150	0.250	0.006	0.010
e	0.500BSC.		0.020BSC.	
L	0.250	0.350	0.010	0.014

*Figure 13.8-PIN DFN Outline Package（3mm*2mm）*

Land Patterns

8-P DFN

The figure below illustrates the recommended land pattern details for the π16xxxx in a 16-pin narrow-body SOIC. The table below lists the values for the dimensions shown in the illustration.

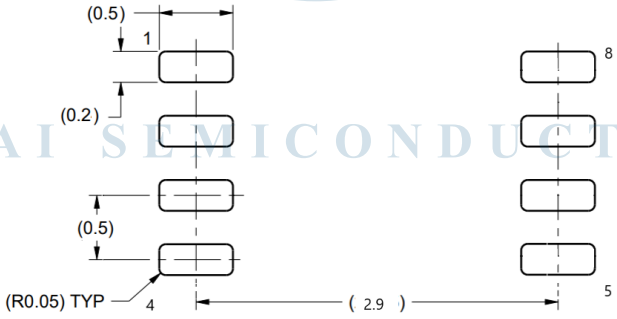


Figure 14.8-P DFN Land Pattern–dimension unit(mm)

Note：

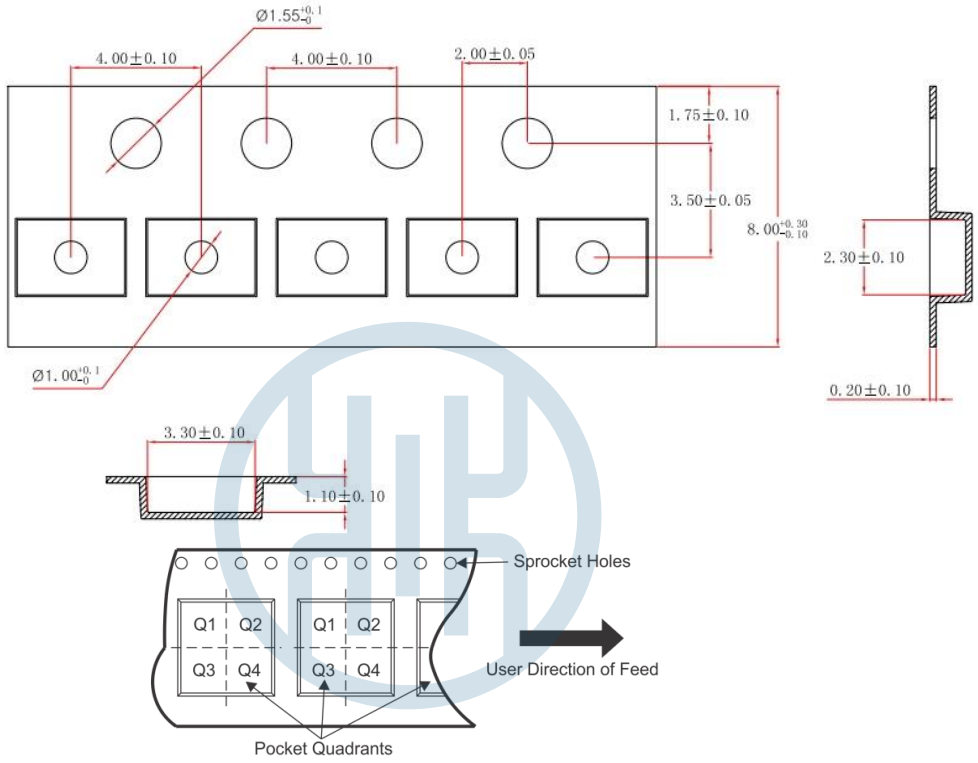
1.This land pattern design is based on IPC -7351

2.All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.

Top Marking

Line 1	Product name. Example:122E11, equals to π122E11
Line 2	YY = Work Year. WW = Work Week AB = no special meaning.

REEL INFORMATION



Note：The Pin 1of the chip is in the quadrant Q1

Figure 15. 8-P DFN Reel Information–dimension unit(mm)

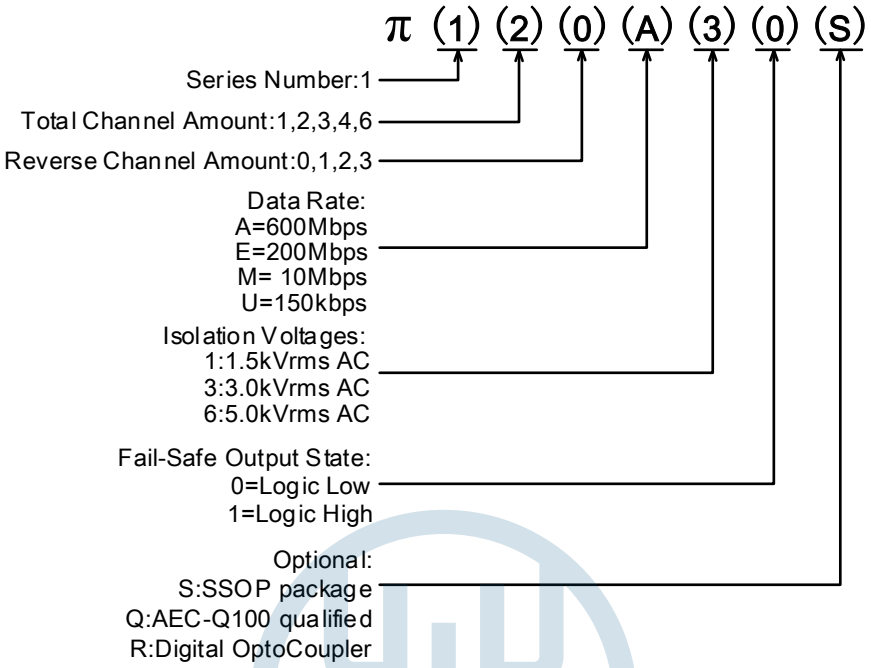
ORDERING GUIDE

Model Name [1]	Temperature Range	No. of Inputs, V_{DD1} Side	No. of Inputs, V_{DD2} Side	Withstand Voltage Rating (kV rms)	Fail-Safe Output State	Package Description	MSL Peak Temp [2]	Quantity per reel
π120E11	−40 to 125°C	2	0	1.5	High	8-P DFN 2mm*3mm	Level-1-260C-Unlimited	4000
π120E10	−40 to 125°C	2	0	1.5	Low	8-P DFN 2mm*3mm	Level-1-260C-Unlimited	4000
π122E11	−40 to 125°C	1	1	1.5	High	8-P DFN 2mm*3mm	Level-1-260C-Unlimited	4000
π122E10	−40 to 125°C	1	1	1.5	Low	8-P DFN 2mm*3mm	Level-1-260C-Unlimited	4000

Note：

1. Pai1xxxxx is equals to π1xxxxx in the customer BOM
2. MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
3. MOQ, minimum ordering quantity.

PART NUMBER NAMED RULE



Notes:
Pai1xxxxx is equals to π1xxxxx in the customer BOM

Figure 16. Part Number Named Rule

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REVISION HISTORY

Revision	Date	Page	Change Record
1.0	2018/09/17	All	Initial version
1.1	2018/11/28	P11	Changed the recommended bypass capacitor value.
1.2	2019/09/08	Page1	Changed the contact address. Add *iDivider* technology description in General Description. Changed propagation delay time, CMTI and HBM ESD. Added WB SOIC-16 Lead information.
1.3	2019/12/20	Page1,11,14	Changed description of π1xxx6x.
1.4	2020/02/16	Page1	Changed propagation delay time.
1.5	2020/02/25	Page5	Changed Pulse Width Distortion.
1.6	2020/03/16	Page6	Changed VDDx Undervoltage Threshold and Regulatory Information. Added information of Land Patterns and Top Marking
1.7	2020/04/16	Page12	Optimize description and format to make it consistent with the Chinese version.
1.8	2021/05/17	Page 10	Changed part number named rule
1.9	2021/12/06	Page5	Updated Data Throughput Range.